

Reliability Monitoring For Highly Leaky Devices

J.T. Ryan, J.P. Campbell, K.P. Cheung*, and J.S. Suehle

National Institute of Standards and Technology
Semiconductor and Dimensional Metrology Division
Gaithersburg, MD USA

*Phone: 301-975-3093, email:kpckpc@ieee.org

R.G. Southwick

Now at IBM Research
Albany, NY USA

A.S. Oates

Taiwan Semiconductor Manufacturing Company
Hsin-Chu 30844, Taiwan

Abstract— We demonstrate a new charge pumping (CP) methodology, frequency modulated CP (FMCP), that robustly treats metrology challenges associated with high gate leakage current. By moving to an AC coupled measurement, we are able to easily resolve small CP signals despite excessively high gate leakage current backgrounds. We demonstrate the utility of FMCP as a reliability monitoring tool in highly scaled and highly leaky devices.

Keywords; charge pumping, leakage current, frequency modulation

I. INTRODUCTION

It seems like a universal truth that advanced development routinely challenges the validity of conventional reliability measurements. This situation has, in some ways, been beneficial as this requires us to better understand our measurement limits and conceive workarounds. Charge pumping (CP) has been utilized and relied upon as a defect monitoring tool for several decades [1, 2]. However, this technique has an Achilles heel common to many other measurement techniques: gate leakage currents. Excessive leakage current associated with advanced and early development devices stymie its effectiveness and renders the CP signal virtually un-resolvable. Even for high-k devices, with sub-nm equivalent oxide thickness scaling goals, gate leakage is a major metrology limiting factor being exacerbated with each new device generation.

The effect of increasing gate leakage on the CP measurement is schematically illustrated in fig. 1. For the case of devices with relatively thick gate dielectrics (fig. 1a), the leakage current is small compared to the recombination current and I_{CP} can be easily measured. However, when the gate oxide is relatively thin (fig. 1b) the gate leakage can become much larger than I_{CP} . The major obstacle in this scenario lies in the precision in which the substrate current, which is composed of CP recombination current (I_{CP}) and gate leakage current (I_G), can be measured. Once I_{CP} becomes a small fraction of the total current, I_{CP} becomes very difficult to precisely resolve and the technique fails. Simply speaking, it is very difficult to resolve a small signal (I_{CP}) residing on a much larger background (I_G).

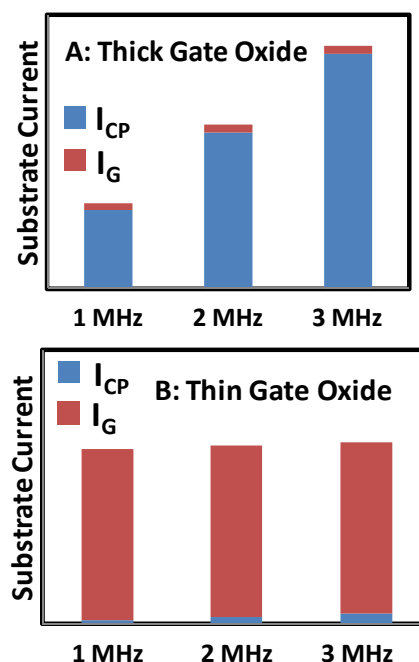


Fig. 1. Schematic scenario of I_{CP} and I_G for the case of (a) relatively thick gate oxides and (b) relatively thin gate oxides. When the substrate current is completely dominated by I_G , the small CP signal becomes extremely difficult to precisely detect.

Fig. 2 illustrates such a case of excessively high leakage where we attempt to use conventional CP to obtain constant amplitude (V_{AMP}), swept base voltage (V_{BASE}) CP curves, commonly called Elliot curves [3]. The device used is a highly leaky $10\ \mu\text{m} \times 0.055\ \mu\text{m}$ 1.4 nm SiON n-channel MOSFET. As can be seen, the CP conditions result in very high leakage current in the range of 10 to 100's of nA, depending on the gate bias. Typically, this scenario is treated via a high-low frequency subtraction where a low frequency CP curve is subtracted from a high frequency CP curve. Since leakage should be frequency independent (more on this later), the subtraction yields I_{CP} . As mentioned before, the precision of extracting I_{CP} with this method is lacking and, as expected, the anticipated pA levels of I_{CP} are completely un-resolvable in fig. 2.

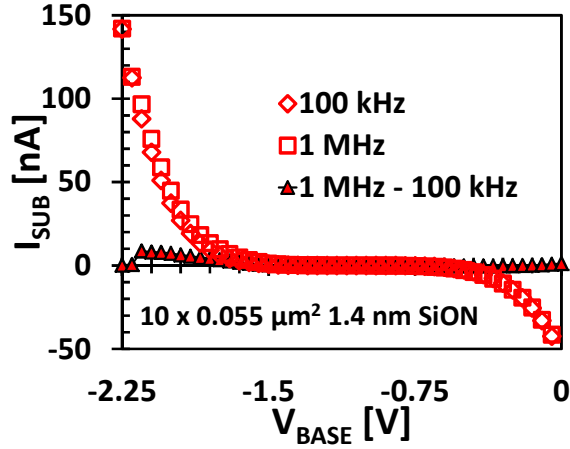


Fig. 2. Conventional CP approaches fail when I_G becomes large compared to I_{CP} . Shown are high and low frequency Elliot curves for a highly leaky device. The high-low subtraction yields little CP data.

Herein, we outline a new CP measurement technique called frequency modulated CP (FMCP) in which we robustly treat the leakage issue illustrated in the previous figures. Fig. 3 illustrates FMCP Elliot curve measurements on a production quality $10 \mu\text{m} \times 0.035 \mu\text{m}$ 1.8 nm capacitance equivalent thickness (CET) SiON n-channel MOSFET. Despite extremely high I_G , we obtain clear CP signals on this small, high quality device (pre stress D_{it} about $4 \times 10^{10} \text{ cm}^{-2}$).

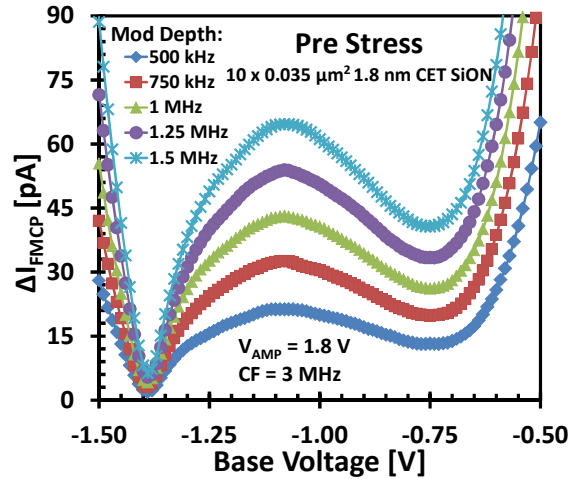


Fig. 3. The FMCP technique is easily able to resolve small CP signals in highly scaled and highly leaky devices.

The FMCP technique presented below and demonstrated for reliability monitoring overcomes the leakage issue by transforming a traditionally DC CP measurement into an AC coupled measurement. In doing so, the precision of measuring the I_{CP} component of the substrate current is substantially less troubling.

II. EXPERIMENTAL

A schematic illustration of the FMCP measurement is shown in fig. 4. In FMCP, the conventional single-frequency CP square wave gate voltage (V_G) pulse is replaced with a frequency modulated V_G pulse. The AC coupled substrate

current can then be measured with a lock-in amplifier. For demonstration purposes, we can also detect the AC coupled substrate current using a current pre-amplifier and digital storage oscilloscope. Again, for the purposes of this paper, we demonstrate a digital storage oscilloscope detection method; however, the lock-in detection is the better choice as it treats the leakage/precision issues much more robustly.

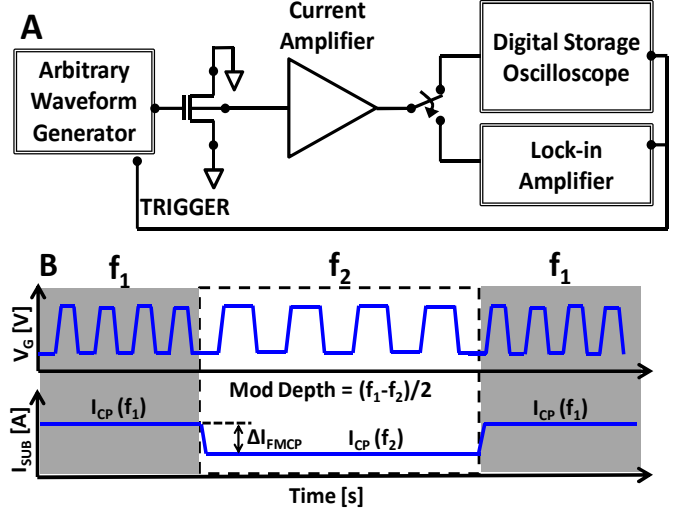


Fig. 4. (a) Schematic of the FMCP measurement. An arbitrary waveform generator applies a frequency modulated square wave voltage pulse to the gate. The AC-coupled substrate current is measured with a current amplifier and a digital storage oscilloscope or lock-in amplifier. (b) The substrate current oscillates between two values (I_{CP1} and I_{CP2}) corresponding to the two different CP frequencies (f_1 and f_2). In FMCP, the lock-in amplifier detects the difference between these two levels of I_{CP} , defined as ΔI_{FMCP} .

In this approach, the measured lock-in output is the difference in substrate current between the two modulated V_G frequencies (ΔI_{FMCP}), as shown in fig. 4b. The two frequencies, f_1 and f_2 , are defined by a center frequency (CF) and modulation depth. Assuming I_G is independent of the V_G pulse frequency, the lock-in eliminates the leakage current background allowing for a very precise measure of the difference in I_{CP} at the two frequencies (ΔI_{FMCP}). In this approach, there is no need to measure the quasi-DC I_G component and thus does not mask the CP response.

It should be obvious at this point that FMCP is significantly more immune to gate leakage currents and can serve to be an accurate measure of defect density, even in highly leaky devices. Additionally, uncertainties in conventional CP (such as amplifier offset or gain calibration) are eliminated.

It's important to discuss our assumption of frequency independent gate leakage current. This assumption relies heavily on the ability of a given pulse generator to maintain identical voltage levels at different frequencies. Additionally, this assumption is influenced by the time spent in a rising or falling edge of the V_G square wave pulse train. If the rise/fall times are held constant, more time is spent in a rising or falling edge when the V_G frequency is increased, leading to differences in overall leakage response.

For all FMCP data shown, the modulation frequency (rate at which we switch between f_1 and f_2) is 103.3 Hz while the rise

and fall times are 5 ns. With the exception of fig. 2, all data was taken on the same $10\text{ }\mu\text{m} \times 0.035\text{ }\mu\text{m}$ 1.8 nm CET SiON n-channel MOSFET.

III. RESULTS AND DISCUSSION

The robustness and utility of FMCP has already been demonstrated in fig. 3 where Elliot curves, taken at various modulation depths, were obtained on a particularly leaky device. Note that since these measurements involve a difference in I_{CP} between two CP frequencies, we plot these measurements as ΔI_{FMCP} . Also note that increasing the modulation depth is identical to increasing the frequency in a conventional CP measurement. Focusing on the peaks in the Elliot curves at V_{BASE} about -1.1 V (representing full accumulation to full inversion biasing) seen in fig. 3, fig. 5 plots ΔI_{FMCP} as a function of frequency. Note this is plotted as Δ Frequency due to the nature of the modulation scheme. Here we observe a nearly perfect linear relationship, attesting to the high quality of the device (negligible bulk dielectric defects) and complete trap filling [4]. From this data, we extract from the slope an interface state density (D_{it}) of about $3.9 \times 10^{10}\text{ cm}^{-2}$ corresponding to about 136 defects in the device.

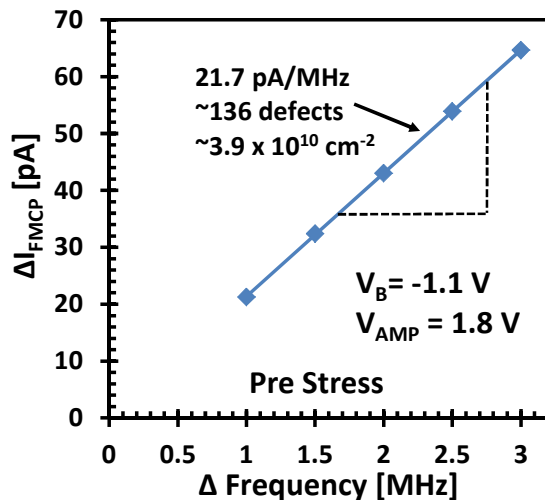


Fig. 5. (a) A nearly perfect linear relationship is observed in the ΔI_{FMCP} vs. Δ Frequency plot corresponding to $D_{it} = 3.9 \times 10^{10}\text{ cm}^{-2}$. This data was extracted from the I_{CP} peaks in fig. 3 ($V_{BASE} = -1.1\text{ V}$)

For completeness we have also measured ΔI_{FMCP} as a function of center frequency for various modulation depths (fig. 6) at the Elliot curve peaks of fig. 3 ($V_{BASE} = -1.1\text{ V}$). The observed flat response further “proves” the technique and is a good indicator of complete trap filling [4] and negligible bulk trapping.

We also note that a two-frequency FMCP measurement is easy to implement and well suited for lock-in amplifier detection. However, in principle, more exotic frequency modulation schemes could be applied. For example, fig. 7 illustrates a “staircase” FMCP plot in which I_{CP} was measured in response to a staircase modulation waveform in which the CP frequency was varied between f_1 (1.5 MHz) and f_2 , f_3 , f_4 , f_5 , and f_6 (2.1 MHz, 2.7 MHz, 3.3 MHz, 3.9 MHz, and 4.5

MHz). Not as robust as the lock-in detection, this waveform required the use of the current pre-amplifier/digital storage oscilloscope detection method.

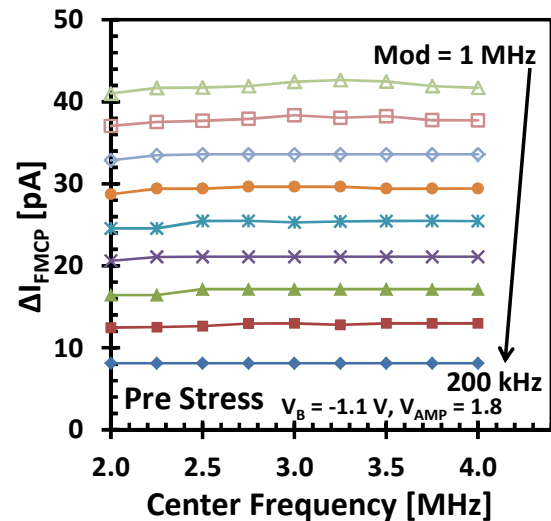


Fig. 6. ΔI_{FMCP} vs. center frequency at various modulation depths displays a flat response. This measurement further proves the concept of FMCP and is indicative of negligible bulk trapping and complete trap filling.

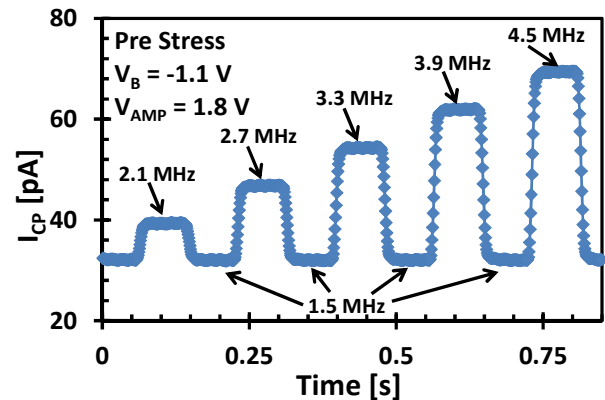


Fig. 7. “Staircase” I_{CP} response due to a more complex six frequency modulation scheme. Although not as robust as a two frequency lock-in detected measurement, it clearly demonstrates the utility of the FMCP.

Thus far, we have detailed a powerful CP method which robustly treats leakage current errors and is well suited to examine advanced device structures. However, we also note that this measurement is quite sensitive (easily measure 10’s of defects with a noise floor well below 1 pA) making it a good candidate to monitor reliability in highly scaled devices. We demonstrate this by subjecting our device to a series of constant voltage (accumulation) room temperature stress sequences with the intent to generate relatively small increases in interface state density. For stress 1, V_G was held at -2 V for 3600 s while V_G was held at -2.5 V for 600 s for stress 2.

The pre-stress/post-stress I_D - V_G and I_G - V_G (normalized to current density J_G) characteristics are shown in figs. 8a and 8b, respectively. Note that after stress 1, there is no noticeable threshold voltage shift, I_D degradation, or change in I_G characteristics. Only the harshest stress (stress 1 & 2)

introduces a small threshold voltage shift and small increase in leakage current

However, when we track the defect generation in these devices using FMCP we note a very distinct increase in defect density. After obtaining Elliot curves similar to fig. 3 (not shown) on the device after the stress sequences and converting ΔI_{FMCP} into charge per cycle (dividing I_{CP} by electronic charge and CP frequency), fig. 9 clearly illustrates the degradation. Note that each grouping of curves (pre stress, stress 1, and stress 1 & 2) contains five separate curves with different modulation depths (again, similar to fig. 3).

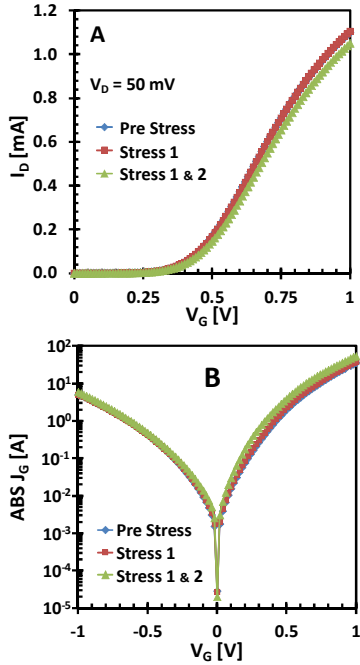


Fig. 8. Following stress, little degradation is observed via (a) I_D - V_G and (b) J_G - V_G .

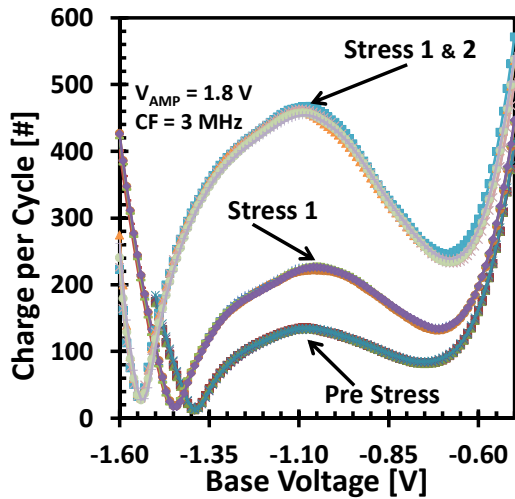


Fig. 9. After converting to charge per cycle (procedure discussed in the text), the degradation is clearly visible via FMCP.

Similar to fig. 5, we can also extract defect densities from the data of fig. 9 via the slope of the ΔI_{FMCP} vs. Δ Frequency

plot. This is shown in fig. 10 for the pre-stress, stress 1, and stress 1 & 2 data.

After stress 1, we generated about 69 defects ($D_{it} = 5.9 \times 10^{10} \text{ cm}^{-2}$) and an additional 231 defects ($D_{it} = 1.3 \times 10^{11} \text{ cm}^{-2}$) after the more harsh stress 2. Again, we note an extremely good linear relationship of this data as well as a robust method to track small changes in defect density even in devices with high gate leakage.

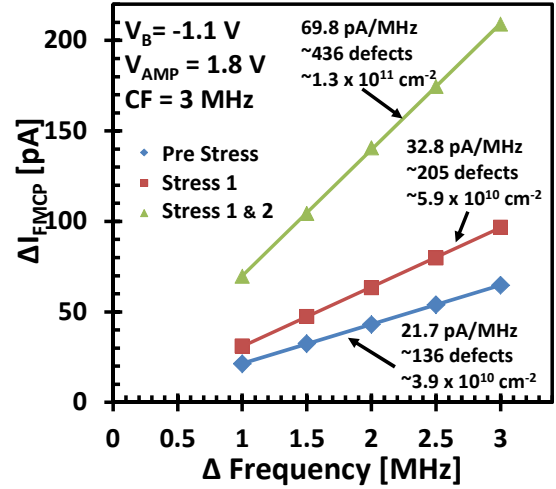


Fig. 10. Slope changes in ΔI_{FMCP} vs. Δ Frequency due to stress. We observe relatively small changes in defect density following stress, even in these highly leaky devices.

A particularly interesting observation is that the clear stress-induced defect generation observable via FMCP (fig. 10) is barely apparent using conventional DC characterizations like I_D - V_G and I_G - V_G (figs. 8a and 8b). This further demonstrates the sensitivity and utility of this technique as a reliability monitoring tool for nano-scale devices.

IV. CONCLUSIONS

We have outlined the inherent difficulty in measuring small changes in I_{CP} in the presence of extremely high levels of gate leakage current. Our solution is FMCP which robustly treats the leakage issue by transforming a traditionally DC measuring into an AC detected scheme. We have highlighted its ability to robustly treat leakage current and demonstrated its power and sensitivity as a reliability monitoring tool in highly scaled and highly leaky devices.

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