

Method of Deciding Burn-in Stress Voltage in Conceptual Design Phase

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INTRODUCTION

Randomly unintended process defects or process variations are the major contributor to semiconductor component reliability failures. DRAM manufacturers rely on burn-in (BI) to achieve required field failure rates as shown in fig.1. [1] For the voltage acceleration an exponential relation between time and voltage is used [2] (In addition, there is acceleration factors for applying stress pattern[3] & frequency that is not considered here.) Typically, voltage acceleration parameters with multi defects are experimentally determined for each product and technology. [4] However, The decision of BI voltage in conceptual design level (such as a planning phase to develop the new product using new process as shown in fig 2) without evaluating product has not been discussed yet. In this paper, we propose new ratio method that could be used in the conceptual design, because designer has not known defect characterizations, when the BI voltage should be decided without acceleration factors to develop the next generation's DRAM in fig.3. First, to establish this method, the history of BI stress voltage and early life failure rate (ELFR) data was reviewed over past ten years. Second, based on the existing trend data, we will find the individual increasing ratio between internal stress voltage (V_{stress}) and nominal use-voltage (V_{use})[1] compared to etch design rule product. Finally, we will show that both bit line (storage node cell cap.) and word line stress voltage (V_{pp}) ratio with single BI condition for screening multi defect are investigated and discuss the design guide by considering BI strategy in planning phase.

BURN-IN MODELING AND V_{STRESS}

In the case of BI, wherein it uses both stress voltage and temperature (85~140°C) stresses, the effects of both should be taken into consideration. For BI modeling, similar equations as for gate oxide are used as shown in fig.4. For temperature acceleration, the well-known Arrhenius equation is applied, and for the voltage acceleration an exponential relation between time and voltage is used. The acceleration parameters are experimentally determined for each product and technology. The weibull distribution (fig.7) is accepted as probability distribution. Typical BI voltage is usually 1.1 to 1.7 times higher than the nominal voltage. This also applies to chip internal voltages which are generated on the product. Traditionally, the BI stress voltage could be calculated from equation (1) with T_{user} and V_{user} (use-conditions). (Where: E_a =Activation energy (eV), k = Boltzmann's constant, β = Voltage acceleration rate factor. (V^{-1}))

$$V_{stress} = V_{User} + \left\{ \left(\frac{1}{\beta} \right) \ln AF_{Total} - \frac{E_a}{k} \left(\frac{1}{T_{User}} - \frac{1}{T_{Stress}} \right) \right\} \quad (1)$$

To predict lifetime of multiple defects in fig.5 and fig.6, the equation to describe distribution after BI is shown in equation (2) and fig.7 [4]

$$\sum_{defect A-D} F_{pBI}(t) = \frac{F(t + t_{BI equiv}) - F(t_{BI equiv})}{1 - F(t_{BI equiv})} \quad (2)$$

These equations apply to extrinsic and intrinsic distribution [5]. By using these equations, ELFR could also be obtained by estimating the product defective part per million (DPPM) from user condition.

RESULTS AND DISCUSSION

Burn-in effectiveness relies on the capability to accelerate any latent defects to failure. However the margin between operating voltages and any additional voltage that may be applied during burn-in is shrinking because the intrinsic reliability margins to voltage are shrinking. Consequently, elevated voltage are not only uncovering latent defects, but are impacting the expected lifetime of the intrinsic material properties of semiconductor device. Conventionally, when designers decide the stress voltage, limitations such as acceleration parameters should be taken into consideration. In this study, in order to help circuit and process designers who work early design stage, we propose method of determining the Burn-in stress voltage without acceleration parameters. For obtaining the optimized stress voltage, we investigated the history of Burn-in stress voltage over past ten years as shown in fig.8. We found the increase ratio of stress voltage which is to meet field ELFR (ppm) target as shown in fig 9.

Methodology

Various histories of products and process were reviewed to confirm the increasing ratio of BI stress voltage in fig 10, 11. The ratio involves a two node approach. The first node which determines charge level of DRAM cell capacitor is Bit line (BL) voltage. Second power node is word line (WL) voltage level with operating gate node of cell transistor. [6] In fig.10 (a), constant increasing ratio of BL voltage is observed $64\% \pm 14\%$. Furthermore, as shown in Fig. 10(b), increasing ratio of monitoring voltage of Product Reliability Test (PRT) which is evaluated ELFR (~1year) is observed $33.1\% \pm 9\%$. Fig.11 shows the average increasing ratio of WL voltage is observed $24.3\% \pm 8\%$. Also, as shown in Fig. 11(b), increasing ratio of monitoring voltage of PRT is observed $11.7\% \pm 3\%$, even though materials and processes, architectures, was changed during past ten year. It is indicated that circuit designer can obtain the screen voltage without product defect information. The above described concept was verified from ELFR which were returned field data to meet reliability target as shown in fig.9. Utilizing this BI stress concept is effective and shortens the required development time substantially.

CONCLUSION

Design for next generation DRAM on early development stage should be concerned about the intrinsic reliability margins and maximum Burn-in stress voltage. This paper proposes that BI stress voltage, when latent defects could not be evaluated by burn-in to obtain the acceleration parameters, is decided by the increasing ratio (as shown in Table.1.) of historical burn-in stress voltage trend.

REFERENCES

- [1] "International Technology Roadmap for Semiconductors" <http://public.itrs.net/>
- [2] C.Glenn Shirley., "Infant Mortality Control" *IRPS tutorial*, 2002.
- [3] Klaus Nierle., et al., *IRW*, 2000, pp.183-184.
- [4] Rolf-P. Vollerten., et al., *IRW*, 1999, pp. 167-173
- [5] Thomas J.Anderson., et al., *IRPS*, 2006, pp. 545-551
- [6] J.Y.Seo et al., *Microelectronics Reliability*, 2005, pp. 1317-1320

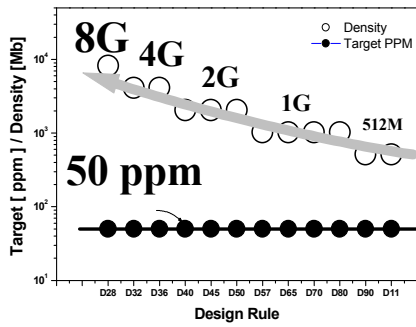


Fig.1. DRAM Product Generation vs Early failures target (Failures during the first 4000 hours of operation (~1 year's use at 50% duty cycle)) [1]

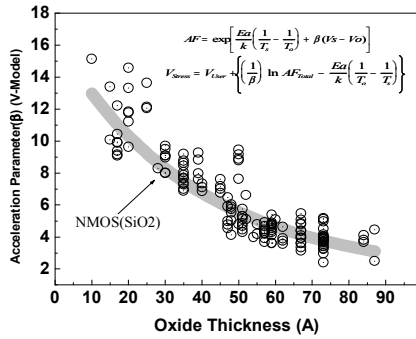


Fig.4 Voltage acceleration parameter values (β) as function of Gate oxide thickness (\AA).

$$F(t) = 1 - R(t) = 1 - \exp\left[-\left(\frac{t}{\eta}\right)^\beta\right] \quad (3)$$

$$F(\text{Use} + \text{BI} | \text{BI}) = 1 - R(\text{Use} + \text{BI} | \text{BI}) = a(1 - R_a(\text{Use} + \text{BI} | \text{BI})) + b(1 - R_b(\text{Use} + \text{BI} | \text{BI})) + c(1 - R_c(\text{Use} + \text{BI} | \text{BI})) + d(1 - R_d(\text{Use} + \text{BI} | \text{BI})) + \dots \quad (4)$$

Fig.7. Equation (3): Weibull distribution and Equation (4): Cumulative failure of components post Burn-in stress [5]

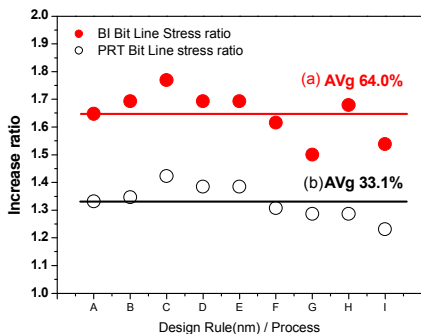


Fig.10. Increase ratio of Bit line (BL): (a) Burn-in stress, (b) ELFR monitor stress (~1 year's equivalent condition)

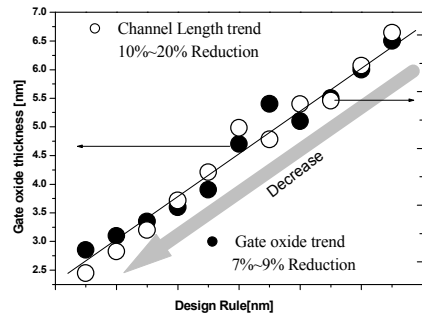


Fig.2. Design rule versus Gate oxide thickness / channel length reduction

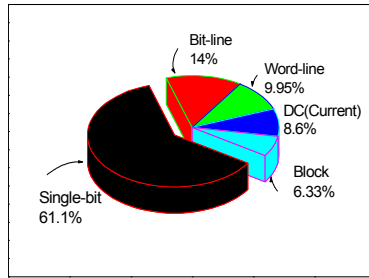


Fig.5 Distribution of the analyzed early failure case by stressing burn-in.

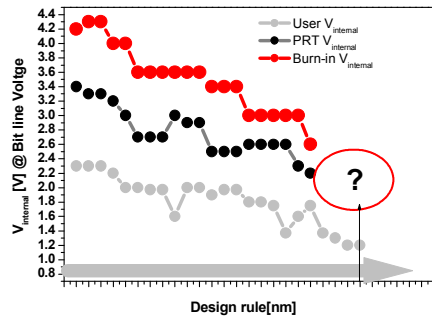


Fig.8. Voltage reduction trend (Use, Monitoring, Burn-in) versus DRAM design rule

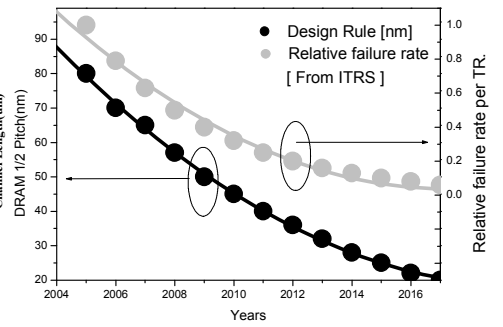


Fig.3. Scaling of DRAM Half Pitch and Relative failure rate per TR. [1] from ITRS

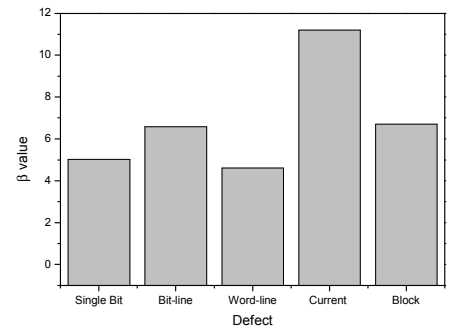


Fig.6 Acceleration parameters (β) with multiple defects are experimentally determined for etch defect.

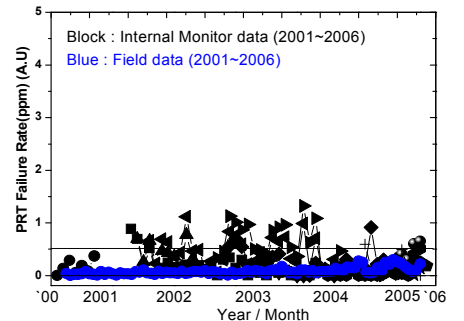


Fig.9. Early life failure (ppm) of internal monitoring (Block color) trend and filed monitoring trend (Blue color)

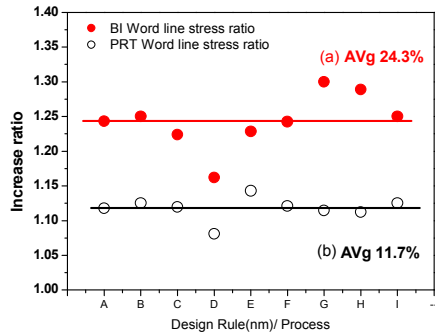


Fig.11 Voltage increase ratio of word line (WL): (a) Burn-in stress, (b) ELFR monitor stress (~1 year's equivalent condition)

Stress Voltage	Bit Line voltage	Word Line voltage
*User (Reference)	* x1	* x1
PRT(Use-like monitor)	x1.33	x1.17
Burn-in	x1.64	x1.24

Table.1. Summary of Increase ratio (Comparison between word line and bit line level)