Impact of Deep Trench Isolation on Advanced SiGe HBT Reliability in Radiation Environments

Stanley D. Phillips [1*], Akil K. Sutton [1], Aravind Appaswamy [1], Marco Bellini [1] John D. Cressler [1], Alex Grillo [2], Gyorgy Vizkelethy [3], Paul Dodd [3], Mike McCurdy [4], Robert Reed [4], and Paul Marshall [5]

School of Electrical and Computer Engineering, Georgia Institute of Technology, Atlanta, GA 30332-0250, USA [1]
University of California at Santa Cruz, Santa Cruz, CA, USA [2]
Sandia National Laboratories, Albuquerque, NM, USA [3]
Vanderbilt University, Nashville, TN, USA [4]
Consultant to NASA-GSFC, Greenbelt, MD, USA [5]
Phone: 1-404-385-6403, Email: stan.phillips@gatech.edu [*]

Abstract— **We investigate, for the first time, the impact of deep trench isolation on the total ionizing dose (TID) and single event upset (SEU) tolerance of advanced SiGe HBTs. We employ a combination of 63MeV protons, 10keV X-rays, and 36MeV oxygen ion microbeam irradiation and compare a 3rd generation, high-performance (HP), deep-trench isolated, SiGe BiCMOS platform with its cost-performance (CP) variant without deep-trenches. Although the CP SiGe HBTs are shown to be more susceptible to TID damage, the elevated damage is not attributed to variations in deep trench isolation (DTI), but to spacer oxide differences. CP SiGe HBTs are surprisingly found to offer a potential built-in self-mitigation mechanism for SEU, which is a direct result of the influence of the deep trench isolation on the charge collection dynamics associated with ion strikes. Calibrated, full 3D ion strike TCAD simulations are employed to explain the results, revealing substantial enhancement of radial charge diffusion for structures implemented with little to no deep trench. Mitigation of charge collection events are found to occur for emitter-center strikes for devices with limited/eliminated DTI with the caveat of larger collection for outside-DTI ion strikes.**

Keywords- Deep Trench Isolation, SEU, SEE, Total Ionizing Dose, Silicon-Germanium Technology, SiGe, HBT

I. INTRODUCTION

Microelectronic system reliability in an "extreme environment" context is contingent upon numerous parameters that are inherent to the environment in question. For example, space-based electronic system design must account for the nuances of the technology platform utilized, operating temperature variations, and the relevant impinging radiation fields. Silicon-Germanium (SiGe) BiCMOS technology platforms have emerged as a natural fit for both space and terrestrial applications, due to its improved performance over intrinsic silicon at similar process complexity and better cost-performance than III-V technologies [1]. Specifically, SiGe heterojunction bipolar transistors (HBTs) offer enhanced *dc* and *ac* metrics at low (i.e. cryogenic) temperatures as well as built-in suppression of Multi-Mrad (SiO_2) total ionizing dose (TID) effects. While intrinsically TID hard, previous work has

shown that SiGe HBTs are highly susceptible to single-event effects (SEE) [2]; therefore, radiation hardening by design (RHBD) techniques, at substantial area/power overhead, must be utilized to mitigate SEU for space systems. Given the speed advantage of incorporating SiGe HBTs into digital logic applications, the vulnerability to digital state flips or single even upset (SEU) has received particular attention. Over the past decade a significant amount of research has targeted the characterization of the sensitivity of SiGe HBTs to SEU [3]-[5], understanding the physical processes mechanisms associated with SEU [6]-[7] and assessing mitigation strategies on both the device and circuit levels [8]-[9].

For SEU to occur, generated charges from ion tracks in struck devices must be "collected" by the depletion regions of the transistor, hence inducing charge on the device terminals. If sufficient charge is induced, a significant voltage transient can be introduced, potentially altering the state of a digital cell. A figure-of-merit which has emerged to correlate ion strike events with a corresponding SEU rate is the critical charge parameter [10]. This variable has been shown to be a highly circuit-specific term whose value and validity strongly depend on the nodal impedances of a device embedded in a circuit [11]. However, an understanding of charge collection statistics and work towards collection suppression remains fundamental for improving the sensitivity of transistors to SEU.

Substrate engineering for SEU mitigation has been proposed by several groups and examined through both simulation and fabricated structures. Previous work has examined the incorporation of highly doped, buried p+ blocking layers to introduce opposing electric field lines for charge collection suppression [12], while others have developed highly doped n+ guard ring structures to introduce competing electric fields for collecting deposited charge [13]. In the present work, for the first time, the impact of the presence of deep trench isolation (DTI, an advanced electrical isolation processing step) in SiGe HBTs is analyzed in the context of TID and SEU vulnerability. Although previous studies have identified the repercussions of complex charge collection mechanisms in technologies incorporating deep trench processing [6], no studies to date have been performed on the potential mitigation of SEU through the inclusion/exclusion of this isolation processing step. The
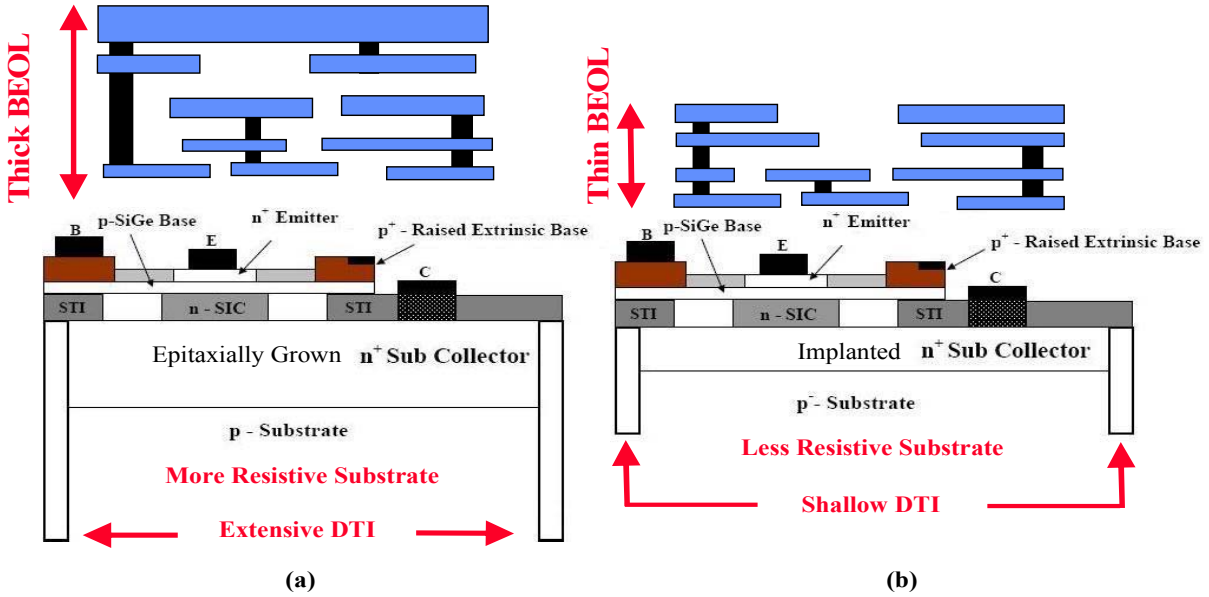
Figure 1. Sample device cross sections for both the HP platform (a) as well as the CP platform (b) are shown, with important process variations in the context of radiation environments highlighted.

hardware used in this study came from two sets of IBM's high-speed 3rd generation SiGe BiCMOS process. The first is a 130 nm, high-speed variant (IBM's 200GHz 8HP technology) labeled here "HP" for "high-performance," and the second is a scaled, lower cost version (IBM's 8WL technology) of the aforementioned technology and is labeled "CP" for "cost-performance" [14]. Both total dose testing (X-ray and high-energy protons) and ion microprobe analysis were used for hardness qualification and the results are interpreted through full 3-D Technology Computer Aided Design (TCAD) simulations.

II. EXPERIMENT DETAILS

A. Device Technology

With higher demands on system performance for satellite communication systems, designers are turning to advanced technology platforms to meet the needs of aggressive system specifications. IBM's 3rd generation platforms are exemplary technologies whose aggressive scaling and innovative device topology leads to extended AC performance while maintaining acceptable breakdown voltages. Cross sections of the HP and CP platforms are shown in Fig 1. Both platforms are a 130 nm technology node that share many similar process steps characteristic of standard high-speed SiGe HBTs. These include a raised-extrinsic base, a retrograded collector, and shallow trench isolation schemes. The important differences between the CP platform from the HP platform reside in the exclusion of deep trench isolation (trench isolation is still employed but is significantly shallower), a more resistive substrate, an implanted sub-collector (as opposed to epitaxially grown), a different collector reach-through process, and a thinner back end-of-the-line process (BEOL), all of which are intended to lower the cost of the CP platform.

B. Total Ionizing Dose Testing

SiGe HBTs of matching emitter areas ($A_E = 0.48$ μm^2) were used for a one-to-one comparison of the damage response between the HP and CP SiGe HBTs to total ionizing dose radiation. All transistors were packaged in 28 pin dual-inline packages (DIP) and independently irradiated with 63 MeV protons and 10 keV X-rays. All device terminals were grounded during both irradiations. The 63 MeV proton irradiation was performed at Crocker Nuclear Laboratory at the University of California at Davis, whose set-up has been previously described [15]. A dose rate of 1 krad/s was used, with fluences ranging from 1.19×10^{12} p/cm^2 to 1.49×10^{13} p/cm^2. The equivalent gamma dose points (all units in SiO$_2$) of 300 krad, 600 krad, 1 Mrad, 2 Mrad, and 3 Mrad were achieved. Previous work has shown SiGe HBTs from this technology generation to show no evidence of an enhanced low-dose rate (ELDR) effect, so no low-dose rate exposures were performed [17]. 10 keV X-ray irradiation was performed at Vanderbilt University's facility with an ARACOR X-ray test system. A dose rate of 1 krad/s was employed to achieve doses of 180 krad, 540 krad, 1080 krad, 1800 krad, and 5.4 Mrad. Pre- and post-irradiation dc characterization of the response to both radiation sources consisted of forward Gummel measurements taken at a collector-base (V_{CB}) voltage of 0 V. The excess base current density (extracted at a base-emitter bias, V_{BE}, of 0.6 V) was used as the figure-of-merit for characterizing total dose degradation.

C. Ion Microprobe Testing

For the charge collection studies performed, a high spatial precision (1 μm x 0.5 μm resolution) heavy ion microbeam at Sandia National Laboratory's Microprobe facility was utilized. Ion beam induced charge collection (IBICC) measurements on both HP and CP SiGe HBTs with identical areas ($A_E = 0.36$

μm^2) and a C-B-E-B-C layout were performed. All four transistor terminals (base, collector, emitter, and substrate) were monitored simultaneously, with total integrated charge and accompanying X-Y position information recorded for each ion strike event. The experiments were conducted using normally incident 36 MeV [16]O ions, having a surface incident linear energy transfer (LET) of 5.4 MeV-cm^2/mg and a range of 25.5 μm in silicon, as determined by the Stopping and Range of Ions in Matter (SRIM) calculations [16]. Samples were prepared in 28 DIP packages with all terminals grounded except for the substrate which was held at -4 V. These biases were intended to mimic transistor "off-state" conditions, a highly sensitive region of operation for SEU. No etching was performed prior to beam exposure, so any ion energy lost in the overlayers of the device had to be estimated with the SRIM calculations.

III.   MEASURED RESULTS

A.   Total Ionizing Dose

The base current degradation of SiGe HBTs due to ionizing radiation has become a well-understood phenomenon and has been documented for numerous technology generations, industry platforms, and radiation sources [17]-[18]. Radiation-induced holes within oxides migrate to semiconductor-oxide interfaces, breaking silicon-oxygen bonds and creating generation-recombination traps that induce larger base currents. The sensitive interfaces present in SiGe HBTs are specifically the emitter-base (EB) spacer oxide for forward-mode degradation and shallow trench isolation (STI) oxide for inverse-mode degradation. Based on this understanding of damage sources, the authors predicted that changes in the depth of the DTI should have no effect on the TID degradation of SiGe HBTs.

Given the predominance of forward-mode operation for circuit architectures, our measured results will only focus on this regime. Given the limited supply of hardware available for all experiments, only single device statistics are available for each radiation source. Although still valuable for comparison purposes, it should be understood that with the probabilistic nature of radiation interactions, these specific values are not representative for every device in the given technology. The excess base current density (ΔJ_B) as a function of absorbed dose for both the CP and HP devices, irradiated with 63 MeV protons and 10 keV X-rays and extracted at a bias value of V_{BE} = 0.6 V, is depicted in Fig 2. A trend in accelerated damage of devices for X-ray radiation is seen in these data sets, as has been noted in [17]. This increase in sensitivity to X-rays can be attributed to the higher charge yield (more un-recombined holes free to migrate to the oxide-semiconductor interface) as compared to 63 MeV protons [19]. Although classically these radiation sources have been shown to have comparative damaging properties, these studies have centered on MOSFET devices where electric field lines are well defined. For bipolar devices, the field lines in spacer oxides are fringing and not uniform as are E-fields within the gate oxides of MOSFETs.

Both data sets indicate that the CP device is inherently softer to TID as compared to the HP device. Given the lack of dependence of the deep trench on base current kinetics, this
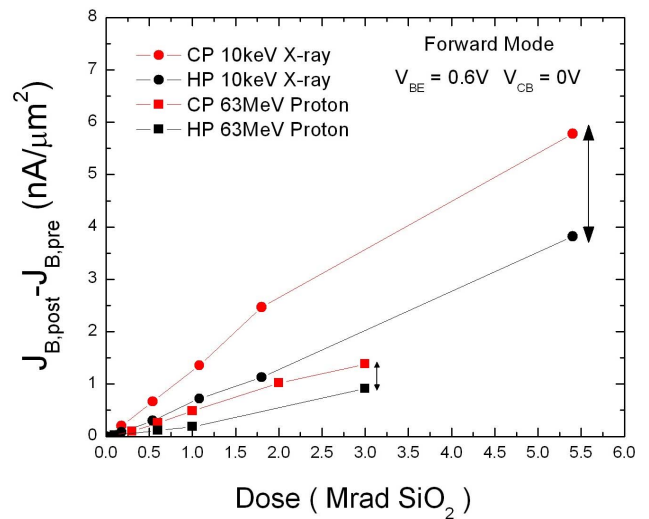

Figure 2. Excess base current of identical area (0.12 μm x 3 μm) devices from the CP and HP platforms, extracted at a V_{BE} of 0.6 V and a V_{CB} of 0.0 V, for both 63 MeV proton and 10 keV X-Ray irradiations.

exaggeration of excess base current can be attributed to either an increase in the overlap of the EB spacer for the CP technology, or variations in the composition of the oxide structure. However, it should be stressed that despite the observation that the CP platform is softer; at typical bias levels to acquire peak f_T ($V_{BE} \sim 0.85$ V) no gain degradation is experienced in either the CP or HP platforms.

B.   Heavy Ion Microbeam

IBICC measurements provide three dimensional integrated charge induction profiles for all device terminals. However, given that current-mode digital bipolar logic (CML) typically employs the collector node of the transistor as the output node of the circuit, we focus on the collector-induced charge following an ion strike. Fig. 3 shows 2-D cuts through the center of the devices of the 3-D collector-induced charge data sets (Z direction collapsed onto the X-Y plane with one coordinate held constant) obtained for both the CP and HP SiGe HBTs. We have plotted the data in the form of a fractional charge induced ($Q_{induced}/Q_{deposited}$) since ion energy loss in the overlayers of the devices are not equivalent, implying different amounts of charge deposited in the two platforms. Referencing the cross-sections of the two platforms, the HP platform has a distinctly larger BEOL process due to both increased metal layers and thicker metal layers. Back calculating the energy lost of the oxygen ion in these overlayers using SRIM, we find that there are significant differences in the energy of the oxygen ion penetrating the surface of each device. These differences in energy will correspond to two distinct LETs for the ions striking the two platforms – hence two separate amounts of deposited charge. For the CP platform, the 36 MeV oxygen ion is attenuated to 29 MeV, or a corresponding LET of 5.69 MeV-cm^2/mg, while for the HP platform the oxygen ion is attenuated to 9 MeV, or an LET of 6.93 MeV-cm^2/mg. The theoretical charge deposited, calculated from the ion LET and penetration depth, is 0.932 pC and 0.404 pC for the CP and HP platforms respectively. By plotting the fractional induced charge, the response to an ion strike is normalized, and the two platforms can be directly
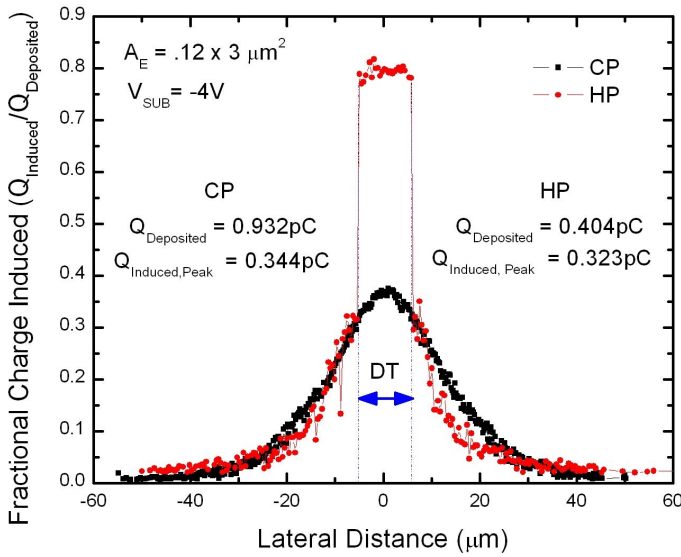
Figure 3. A 2-D cut through the collection peak of the measured fractional collector-collected charge for both the CP and HP devices. Separate charge depositions for the two platforms (due to the substantial BEOL thickness differences) are also indicated, in addition to the peak collection value.

compared. There are several striking characteristics to be noted from Fig. 3, the first being that the shallower trench isolation (~2 μm for CP as opposed to ~8 μm for HP) of the CP device leads to an increase in collected charge outside of the subcollector-substrate junction (defined by the boundaries of the trench isolation). As opposed to the sharp drop in induced charge for HP devices due to deep trench isolation (trench boundaries indicated by arrows in Fig. 3), deposited charges in the CP device outside of the active area can freely diffuse towards the subcollector-substrate junction and be collected. This gradual, smooth decrease of induced charge on the collector terminal moving outwards from the active area of the CP device implies a wider range of sensitive area for upsets when compared to the HP device.

Despite increased charge collection from strikes outside the trench boundary, the CP platform shows considerable mitigation of charge collected for strikes directly to the active area of the HBT (most sensitive region). Charge collection efficiency for the HP HBT is approximately 80%, while the CP HBT barely has an efficiency of 40%. This is an exciting result that isn't fully intuitive. Although significant charge confinement is expected to take place due to the 8 μm deep trench isolation of the HP platform, this platform also incorporates a lower resistive substrate which lowers minority carrier lifetimes (more recombination within the charge track – beneficial). Unlike the HP platform, the CP device has much shallower trench isolation which is expected to promote radial diffusion of charges from the charge track; however, this platform also has a much more resistive substrate. A lower doped substrate will result in a wider depletion region, increasing the amount of charge initially deposited and swept from the collector-substrate junction. Additionally, the dielectric relaxation time of the substrate will be larger, which has classically been reported to result in extended durations of accelerated charge funneling [20]. These conflicting mechanisms leave it unclear as to why the CP device has much

lower charge collection efficiencies for active-area ion strikes. Full 3-D TCAD simulations were employed to evaluate the impact of the processing differences between the two platforms on the measured charge collection statistics.

IV. 3-D TCAD SIMULATIONS

A. *Emitter-Center Simulated Heavy Ion Strikes*

Full 3D models of devices from both platforms were built using Computational Fluid Dynamics Research Corporation's (CFDRC) finite element modeling software package NanoTCAD. The decks were calibrated to both measured *dc* characteristics, as well as microbeam data – an iterative process involving adjustment of minority carrier lifetime model parameters within various semiconductor regions. NanoTCAD ion strike simulations employ a Gaussian charge generation with a peak time of 2 picoseconds. An ion LET of 5.4 MeV-cm^2/mg was used for both platforms for a direct comparison of the charge collection mechanisms inherent to each platform. The spatial location for the ion strike was chosen to be the center of the emitter for both the CP and the HP device. This position has been determined to be the most sensitive strike coordinate, with ions passing through all junctions of the device. Fig. 4 shows the current transient waveforms acquired from the simulation of a normally incident ion strike on the center of the emitter of both devices. These waveforms retain a similar shape between the two platforms; a shape that has been attributed to quick collection of charges from modulated electric fields in the substrate (the classic funnel effect), coupled with drift-diffusion collection of generated carriers [21]-[24]. There is significant attenuation of the slow tail collection (20 ps – 20 ns) in addition to a lower, maximum peak current spike in the transient for the CP platform when compared to the HP platform. This current reduction couples to a reduction in the total integrated charge which is induced on the collector terminal, as seen in Fig. 5.
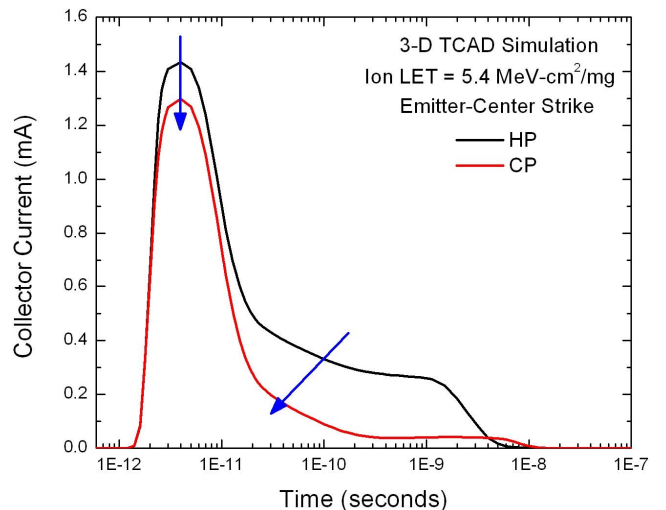

Figure 4. Induced collector current transients from an ion strike normal to the emitter with an LET of 5.4 MeV-cm^2/mg. Reductions to peak current and significant mitigations of "tail" currents are evident for the CP device.

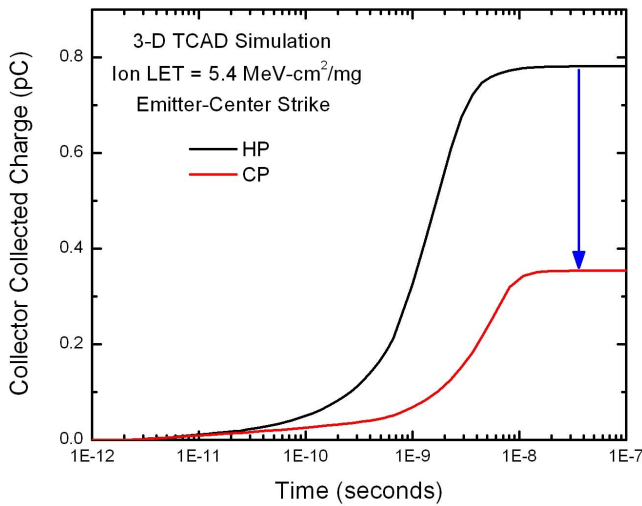**Figure 5.** Integrated collector-collected charge for simulated emitter-center ion strikes to indentical area (0.12 μm x 3 μm) CP and HP SiGe HBTs. A nearly 50% reduction in collected charge is observed for the CP device.

While the simulated charge collection of the HP platform due to an ion strike with an LET of 5.4 MeV-cm^2/mg is approximately 0.8 pC, the CP platform only collects approximately 0.35 pC for an ion with equivalent LET. To understand the large difference between these two charge collection profiles, the evolution of the drift and diffusion of the generated charge is examined.

Fig. 6 and Fig. 7 show the time evolution of the electron drift current density projected on the X-Y plane with one spatial coordinate held constant for both technology platforms. The location of the Z-cut was identical for both the CP and HP platforms and was located directly below the bottom of the deep trench of the HP device. The drift component is observed to be consistently higher for the HP device, stemming from larger field perturbations in the substrate which accelerate electrons in the charge track up into the subcollector-substrate depletion region. Although the CP device also shows a large drift contribution early after the strike (2 ps), the term is smaller than in the HP case, and very quickly shrinks in magnitude. To understand the rapid drop in the electron drift current component in the CP device, the projection of the time evolution of the radial distribution of generated charge carriers on the X-Y plane is plotted in Fig. 8 and Fig 9, for the CP and HP platforms, respectively. The location of the Z-cut was once again identical for the two platforms and was located directly below the bottom on the deep trench of the HP device.

Immediately following the strike, both platforms have nearly the exact same carrier concentration distribution within the charge track. Given that the peak carrier density in the charge track remains roughly constant between the two platforms, yet drift currents are not equivalent, larger carrier diffusion components are expected to be noticeable in the CP device. Increased radial diffusion of free charges *is* evident in the CP device, with smooth reductions in the peak as carriers spread outward into the quasi-neutral substrate. Referring to Fig. 9, the HP device clearly shows slower radial diffusion of charge carriers, even for charges below the deep trench implying a coupling effect between charges confined within the
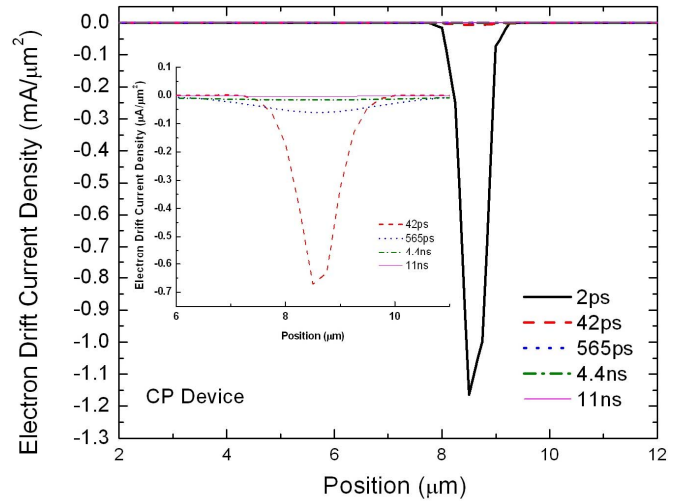

Figure 6. Time evolution of the electron drift current density of the CP device in the Z-direction, collapsed on the X-Y plane and plotted with one spatial coordinate held constant. The inset shows a magnified plot of the drift current density (μA/μm^2) for times well beyond 2 ps. The electron drift component quickly falls off to extremely low values after only 42 ps following the ion strike.
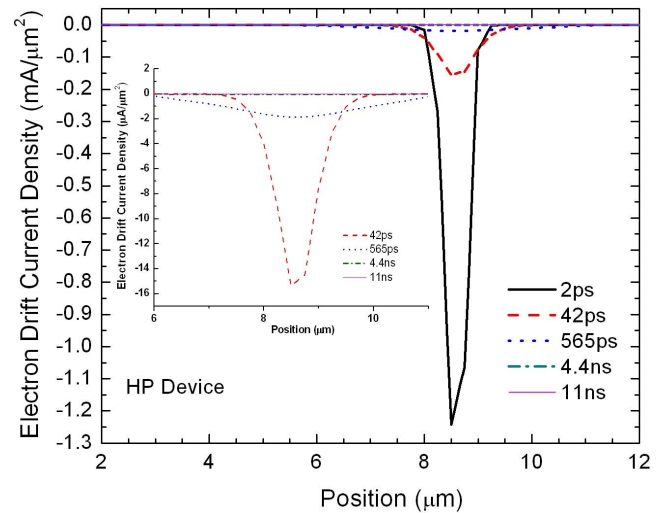

Figure 7. Time evolution of the electron drift current density of the HP device in the Z-direction, collapsed on the X-Y plane and plotted with one spatial coordinate held constant. The inset shows a magnified plot of the drift current (μA/μm^2) for times well beyond 2 ps. The electron drift component maintains distinctly non-zero values for nearly a nanosecond after the strike.

DTI, to the charges in the track below the DTI. Significant difference between the diffusion of the two platforms is especially noticeable for a time of 565 ps after the ion strike. Although the peak carrier concentration remains relatively similar between the two devices at this time, distributions spreading from the peak are quite different. Given that charge deposition is identical between the two platforms and there is a similar peak concentration for both devices, the charge that has not diffused in the HP device has drifted to the sensitive junction and been collected. With limited differences between technologies, the factors which could impact the charge collection process for the two platforms are the substrate resistivity and the DTI. Previous substrate resistivity studies have shown that higher resistive substrates should suffer from
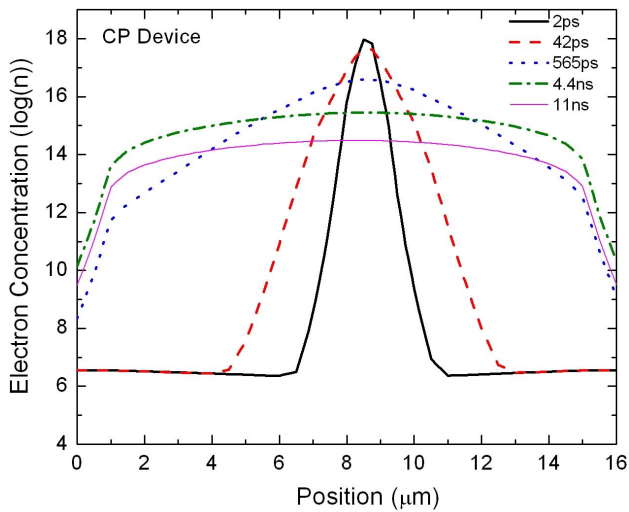
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Figure 8. Time evolution of the radial diffusion of the carrier concentration of the HP device in the Z-direction, collapsed on the X-Y plane and plotted with one spatial coordinate held constant. Large diffusion is evident with smooth spreading of the peak spatially outward in both directions.
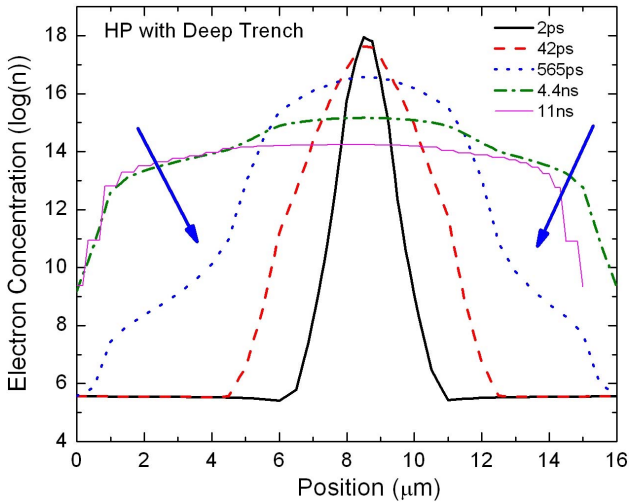

Figure 9. Time evolution of the radial diffusion of the carrier concentration of the HP device in the Z-direction, collapsed on the X-Y plane and plotted with one spatial coordinate held constant. Significant variation in diffusion between the CP device is evident for the time regimes greater than 565ps.

Figure 10. Time evolution of the radial diffusion of the carrier concentration of the HP device in the Z-direction, collapsed on the X-Y plane and plotted with one spatial coordinate held constant. Significant variation in diffusion between the CP device is evident for the time regimes greater than 565ps.

Figure 11. Time evolution of the radial diffusion of the carrier concentration of the HP device in the Z-direction, collapsed on the X-Y plane and plotted with one spatial coordinate held constant. Similar to the CP platform, much larger diffusion arises when compared to the standard HP device.

larger charge collection events [11] (in contrast to the measured data and simulations performed herein); therefore, we attribute the decreased sensitivity of the CP device to variations in the depth of the trench isolation structure.

B. DTI and no-DTI Ion Strikes

For a direct comparison of trench dependence on charge collection events, an additional TCAD model deck was constructed using the model parameters from the HP device. This variant incorporated all of the features of the HP platform, except complete elimination of the DTI. No variation in substrate resistivity was made between these two model decks. An ion LET of 5.4 MeV-cm^2/mg was used for all strike simulations. A plot of the current transient waveforms acquired from the simulation of a normally incident ion strike on the
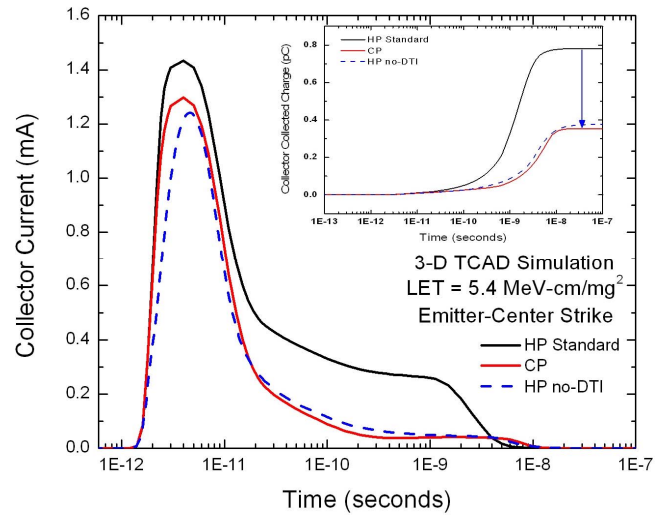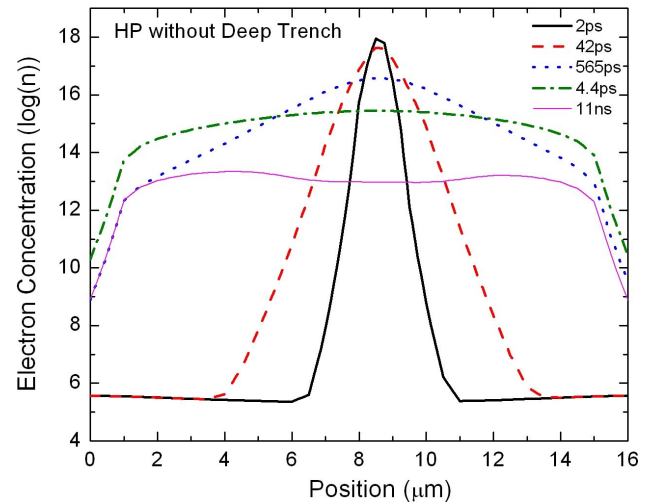
center of the emitter of both the DTI and no-DTI device is shown in Fig. 10. Strong similarities between these results and those for the CP/HP comparison are evident; namely a reduction in peak transient current as well as attenuation of the current tail which couples to a reduction in total charge collected. Examination of the time duration of electric field lines penetrating into the substrate show an equivalent period of charge funneling (which is expected given the identical substrate resistivity); however, smaller electron drift currents exist for the no-DTI device. Once again this reduction can be attributed to larger radial diffusion of charge carriers from the charge track. The projection of the time evolution of carrier density on the X-Y plane is plotted at a depth corresponding to the bottom of the deep trench in DTI device in Fig. 9 and Fig. 11, for the DTI device and the no-DTI device respectively. Similar again to the CP device, the no-DTI structure exhibits

faster spreading of free carriers from the center of the charge track, generating large diffusion away from the sensitive junction where charge would be collected.

C. Outside DTI Sensitivity

Up to this point, only simulated ion strikes orthogonally impingent (i.e. vertical strikes) on the emitter of a device have been under consideration. Despite being the most efficient volume for charge collection events, sensitivity to SEU also exists for ion strikes occurring in the exterior of the trench-enclosed volume, as well as for angled strikes. Given the relatively low doping density of SiGe substrates, minority carrier diffusion lengths can reach magnitudes as large as 100 μm. This large distance allows charges deposited well outside the DTI boundary to have a high probability of diffusing to the active area of the device and be collected before undergoing recombination events. For many SiGe processes, the sensitivity to outside DTI is much less than that for normal emitter-center strikes because of the impedance to carrier diffusion due to deep trench isolation; however, critical charge values for upset have been found to be as low as 100 fC – a quantity which could be collected after outside-DTI strikes for large values of ion LET. For structures which have eliminated or shallower DTI, this sensitivity is greatly enhanced.

The induced collector current transient waveforms as well as integrated charge for the CP device, standard HP device, and no-DTI HP device are shown in Fig. 12 for an ion with an LET of 5.4 MeV-cm^2/mg striking 1 μm from the DTI boundary. Both the CP platform and the HP device with no DTI show greatly enhanced collector current transients, coupling to much larger integrated charges; however, the no-DTI device shows a distinctly different current waveform shape from the other devices. This variation, having much larger currents, is due to the partial collapse of the subcollector-substrate junction from free carriers flooding the depletion region. With no trench isolation impeding the diffusion of carriers to the active area, charges can freely move into the depletion region and compensate the fixed charges present, collapsing the space charge region. The collapse in the depletion region will result in electric fields being pushed into the substrate to support the applied reverse bias to the subcollector-substrate junction, accelerating charge collection through funneling mechanisms.

A proposed method for almost completely mitigating charge collection outside of the DTI of a SiGe HBT has been previously presented by the authors [13]. With the incorporation of a highly doped n$^+$ diffusion layer encompassing the device, a shunt path for minority carrier electrons is introduced, which reduces carrier concentrations reaching the sensitive subcollector-substrate junction. Incorporating these structures into platforms with limited to no DTI (essentially reverting back to a junction isolation platform) will eliminate the caveat of exaggerated charge collection of outside DTI strikes while maintaining reduced collection for ion strikes in the active areas of the device.
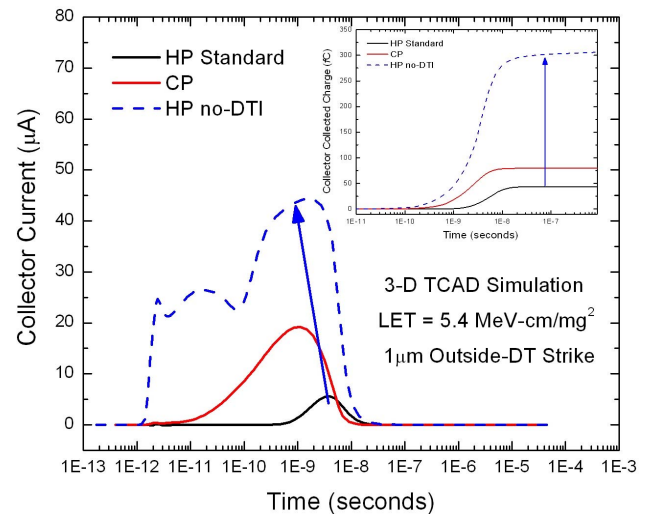

Figure 12. Induced collector current transients from an ion strike normal to the emitter with an LET of 5.4 MeV-cm^2/mg with an inset showing integrated charge collected. Increases in collected charge for outside DTI strikes are observed for devices with limited DTI and extreme increases are seen in the no-DTI variant due to junction collapse from charge flooding in the depletion region..

V. SUMMARY

Through comparisons of IBM's HP and CP technology platforms, the impact of DTI on radiation response has been analyzed in the context of total ionizing dose and single event upset. Although no effect of trench isolation is found to affect the base current degradation resulting from TID, (the accelerated degradation in the CP platform was attributed to differences in oxide thickness and/or compositions, Fig. 2), a large difference in charge collection statistics is found between the CP and HP devices. To understand these differences, device models were constructed for both platforms, as well as a third device model for the HP device which encompassed no trench isolation, to allow a direct correlation between DTI and SEU susceptibility.

The CP showed substantial reduction in collected charge for emitter-center strikes when compared to the HP device, despite having a lower substrate doping. This decrease in charge collection is attributed to larger radial diffusion of deposited charges away from sensitive depletion regions as well as higher carrier mobility in the bulk substrate. The incorporation of a deep trench in the HP device impedes carriers from escaping the drift-region of the charge track, resulting in more charge being swept into the subcollector-substrate junction. Although lower doping has traditionally been observed to increase charge collection, these studies have been performed in platforms with identical trench depths. For a device with little to no DTI, the higher carrier mobility accompanying a lower doped substrate will enhance the radial diffusion of charge.

To directly assess the impact of DTI depth, similar simulations were performed on an HP deck with no trench isolation. Similar results to the CP device were observed, namely a drastic decrease in the amount of charge collected. The time evolution of carrier concentration following the strike

supports the claim that DTI impedes carrier diffusion away from the sensitive subcollector-substrate junction. Despite the mitigation of charge collection for emitter-center strikes, devices which limit DTI depth show extreme sensitivity to ion strikes outside the active area of the device. Potential mitigation schemes for reducing this sensitivity have been explored previously and suggest that reverting to a reversed-biased junction isolation scheme is preferable over DTI for platforms planned to be incorporated in applications where SEU is a concern.

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