Recent Progress of Phase Change Memory (PCM) and Resistitve Switching Random Access Memory (RRAM)

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Abstract—**The increasing demand for high-capacity non-volatile memories in the electronic portable and media applications has required continuous scaling of the conventional FLASH memory technology beyond perceived limits. At the same time, system designers envision the use of novel memory technology may revolutionize the organization of the memory hierarchy of processors and the design of SoC and SiP. This has resulted in the exploration of many alternate memory technologies like PCM, RRAM, STTRAM. In this paper we discuss some of our recent works on understanding the various aspects of PCM and RRAM.**

*Keywords-component: **Non-volatile memory, PCM, RRAM, Scaling.***

I. INTRODUCTION

The amount of information storage in a hand-held device is increasing exponentially with the increase in the functional capabilities of such devices every year [1]. We need to store a large amount of information in a smaller device and there is also a need to access these data in a short time. This has resulted in the replacement of magnetic hard-drives with high storage density FLASH memories as solid-state drives for laptops and other hand-held applications. However the challenges faced in reliably scaling the FLASH technology beyond 2x nm and the desire to reduce the access time has resulted in the exploration of many alternative technologies including PCM and RRAM [1]. These technologies do not seem to pose any fundamental limits in scaling the device dimensions down to single-digit nanometer dimensions [6] and are highly competitive in terms of their speed, endurance, and retention properties to meet the demands of the future electronics industry [2][20]. However there are a number of issues that are yet to be addressed [2][7][8] in these technologies especially in terms of understanding their physics of operation and improving their reliability to enable large-scale integration of these memory devices. In this paper, we focus on some of the key aspects of PCM and RRAM such as understanding their physical mechanism of switching, reducing the power consumption, and also their use in other alternate applications that are beyond the conventional memory applications.

II. PHASE CHANGE MEMORY

Phase change memory (PCM) is one of the most promising emerging memory devices. It has the potential to combine DRAM-like features such as bit alteration, fast read and write, and good endurance and Flash-like features such as non-volatility and a simple structure. PCM is expected to be a highly scalable technology extending beyond scaling limit of existing memory devices [3]. Prototypical PCM chips have been developed and are being tested for targeted memory applications [4][5][9]. However, a complete understanding of the fundamental physics behind PCM operation is still lacking because the key material in PCM devices, the chalcogenide, is relatively new for use in solid-state devices. Evaluation and development of PCM technology as successful mainstream memory devices require more study on PCM devices. The following section focuses on some of our recent works on understanding the key aspects of phase change memories such as the reset resistance drift, thermal disturbance, and the conduction mechanism.
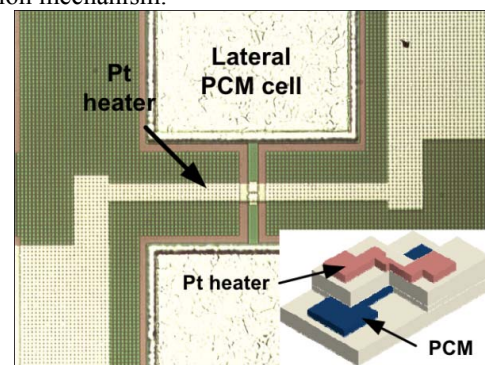

Fig. 1. Microscope image of micro-thermal stage. Pt heater is integrated on top of the lateral phase change memory (PCM) cell. The inset 3D figure shows the MTS heater overlapped region over narrow phase change material programming region. After [12].

A. Understanding Resistance Drift and Thermal Disturbance using Micro Thermal Stage

One of the major challenges for PCM is the drift in the resistance value in its reset state that makes it difficult to be used in multi-level applications. This drift behavior is highly temperature dependent and hence there is a need to study the nature of the drift by controlling the cell temperature [10]. Conventional approaches of using the hot-chuck to control the temperature have speed limitations due to the large thermal

time constant of the chuck. But to better understand drift, we need to extend these measurements to µ s time scale which is relevant for PCM operation. Hence a faster heater is required which has a thermal time constant in microsecond time scale. We implement such a fast heater with a micro-thermal stage (MTS). Fig. 1 shows the lateral PCM cell integrated with the platinum micro-thermal stage [11][12].

By generating Joule heat in the Pt heater, the temperature of the programming region of the PCM cell is controlled. Since the heater is located only a 1 µ m away from the programmed region and also due to its smaller dimensions, the thermal time constant of this structure is ~1 µ s extending the measurement capability by up to 6 orders of magnitude compared to the conventional thermal stages. The power to the micro-thermal heater can be controlled precisely in a nearly linear fashion by controlling the voltage amplitude to the heater, resulting in accurate control of the amount of temperature rise for wide range of temperatures that is calibrated based on the measured temperature co-efficient of resistance of the platinum heater. To measure the temperature dependence of the R_{RESET} drift coefficient, we vary the annealing temperature (T_A) between 25°C (no annealing) and 185°C. The PCM cell is programmed and read at 25 °C without any heating from the micro-thermal heater. Fig. 2(a) shows the R_{RESET} drift over time for various T_A. Fig. 2(b) shows the R_{RESET} drift coefficient calculated from the same data in Fig. 2(a) for various T_A. At low temperature, the drift coefficient increases rapidly. At high temperature, the drift coefficient increases slowly and even decreases possibly due to the simultaneous crystallization.
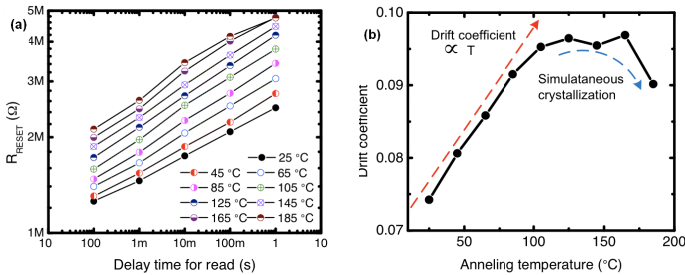

Fig. 2. (a) Reset resistance and (b) R_{RESET} drift coefficient as a function of time after reset programming for various annealing temperatures (T_A). After [12].
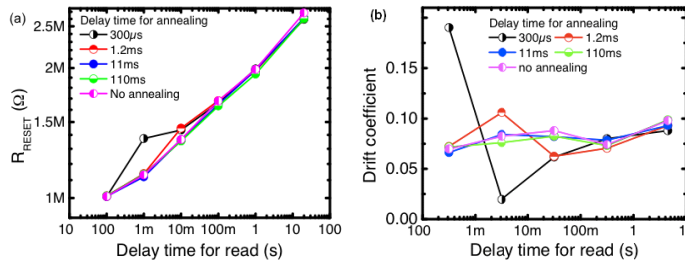

Fig. 3(a) R_{RESET} for various delay time for annealing (d_A). The width of heating pulse is 600 µs at 65 °C. (b) R_{RESET} drift coefficient calculated from Fig. 3(a) The R_{RESET} drift coefficient dramatically changes during and right after annealing for small d_A. After [12].

In the practical scenario for PCM cell in operation, the annealing temperature cannot be constant because cells are thermally disturbed by thermal disturbance [11]. In this case an annealing pulse of fixed amplitude and duration was applied after a certain delay d_A from the time the device is reset. Fig. 3 (a) shows that he R_{RESET} drift over time with various d_A. It can be seen that the annealing pulse at shorter time delay accelerates the drift process whereas the effect of the thermal disturbance reduces for larger delays. This can also be seen from the extracted drift co-efficient values in Fig 3 (b). This is because the decaying of the trap states is accelerated initially by the annealing pulse and does not cause much change at later time delays. It should also be noted that the different annealing delays does not cause any change in the final cell resistance.

B. 1/f Noise Measurements

The amorphous phase of a PCM cell is of a highly disordered state comprising of a large number of traps or localized states. The electrical conduction in the amorphous state of the phase change material is by hopping through these localized states also called as Poole-Frenkel conduction [13]. The density of these trap states or the trap spacing plays a major role in determining the characteristics of the PCM cell in the sub-threshold region. 1/f noise is one of the tools commonly used to characterize the surface and oxide traps in MOSFETs and other electronic devices [14]. Hence measuring 1/f noise in PCM can give us valuable information on the nature of the traps within the amorphous state. It has been proposed that 1/f noise is due to the random fluctuations of the atoms or clusters of atoms inside the amorphous GST [15]. These atomic fluctuations cause the mean trap energy of the different localized states to fluctuate thereby causing a change in the number of available carriers resulting in the current fluctuations. Measuring the power spectral density of the current noise in the PCM devices would give us further details on the nature and number of traps present in the amorphous material.
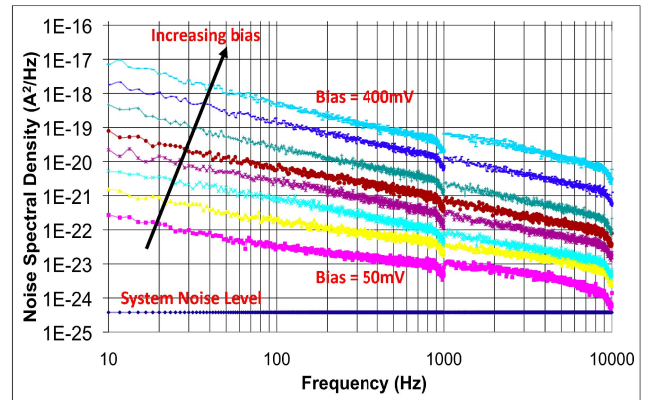

Fig. 4 Power spectral density of 1/f noise measured in a fully reset PCM device. The spectrum was recorded at different bias values.

The PCM cell similar to the one described in [16] was programmed to its fully reset state. The 1/f noise was then measured at various bias values in the sub-threshold region. The power spectral density of the current noise for various bias values are shown in Fig 4 [17]. The noise spectral density follows a 1/f trend in the low frequency regime. Also the spectral density is exponentially dependent on the bias voltage showing that the 1/f noise is an indicator of the current generation process in the amorphous material, which in this

case is believed to follow Poole-Frenkel mechanism. Further experiments on measuring 1/f noise at different temperatures and different programmed resistances can give us additional information on the nature of traps and the conduction mechanism. Measurement of the Random Telegraph Signal in PCM cells will also help reveal the relaxation times of the fluctuation process that causes the 1/f noise [18].

III. RESISTIVE SWITCHING RANDOM ACCESS MEMORY

Metal oxide resistive random access memory (RRAM) is one of the most competitive candidates for future non-volatile memory applications due to its simple structure, fast switching speed (~10 ns), great scalability (<30 nm), and compatibility with current CMOS technology [19][20]. The mechanism of resistive switching phenomenon in metal oxides has been widely attributed to the formation/rupture of conductive filaments (CFs) which may be associated with the migration of oxygen vacancies or metal precipitates [21]. Many reports show that the electrode/oxide interface property would affect the switching modes [22]: if a noble metal such as Pt, Ru is used as the electrode, usually the unipolar switching (reset occurs at the same polarity as set) is observed; if an oxidizable metal such as Ti, TiN, TaN is used as electrode (reset occurs at the opposite polarity as set), usually the bipolar reset is seen. It has been suggested that the unipolar reset is a Joule heating-driven process, while the bipolar reset is a field-driven ion migration process. The key challenges hindering RRAM from large-scale manufacturing includes poor switching and resistance uniformity, relatively large reset current, and a lack of a clear physical picture of the switching mechanism. Significant parameter fluctuations exist in the switching voltages and the resistances, including temporal fluctuations (cycle to cycle) and spatial fluctuations (device to device). Furthermore the requirement of high current density selection devices [20] to provide for the large peak reset current during the switching process imposes great challenges for large array integration [23]. Recent work in the literature show HfOx to be the most attractive RRAM material [24-26]. We further explore the switching properties of HfO_x and AlO_x based RRAM to achieve low power, reliable and fast switching devices.
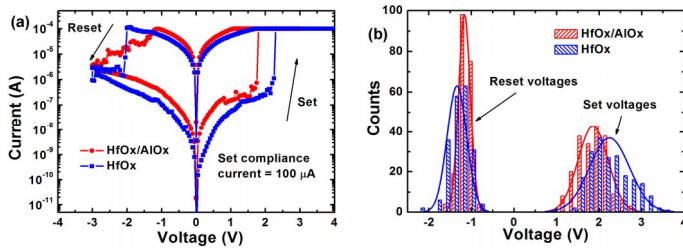
Fig. 5 (a) Typical I-V characteristics of the HfO_x/AlO_x bi-layer sample and HfO_x single layer sample. (b) Distribution of set/reset voltages obtained by 200 DC sweep cycles. Better uniformity in the bi-layer sample.

A. HfOx/AlOx bi-layer RRAM: improved switching uniformity, multilevel storage capability and energy-efficient programming scheme

RRAM devices of TiN/HfO_x/AlO_x/Pt stacks with 0.5×0.5 μm^2 active cell area were fabricated [27]. 5 nm AlO_x and 5 nm HfO_x was deposited by atomic layer deposition (ALD) method. Fig. 5(a) shows the DC sweep I-V characteristics of the bi-layer sample and the single HfO_x layer control sample. Bipolar

switching behavior is shown probably due to the TiN oxygen reservoir effect. Fig. 5(b) shows less dispersion of the set/reset voltages in the bi-layer sample than those in the single-layer samples obtained by 200 DC sweep cycles. Besides the switching voltages, the resistances in either high or low resistance states are also more tightly distributed in bi-layer samples as compared to the single-layer samples. These results suggest that materials engineering by stacking oxides multi-layers may help improve switching uniformity. To explore the multilevel storage capability in RRAM, we found that it was possible to modulate the resistance states during the reset process by varying the reset voltages.
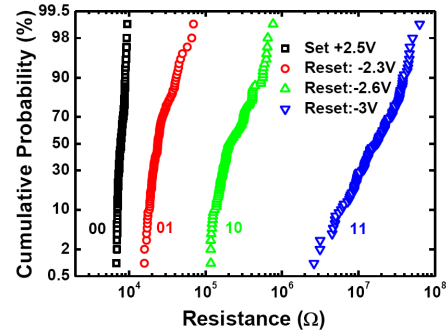
Fig. 6 The resistances distribution of four levels in the HfO_x/AlO_x bi-layer sample. "00" was achieved by +2.5 V/50 ns pulse, and "01", "10", "11" were achieved by -2.3 V/ 50 ns, -2.6V/ 50 ns, -3 V/50 ns pulses, respectively.

Fig. 6 shows possible 2-bit storage potential for the bi-layer sample. The resistance distribution of one set state and three reset states were obtained by varying the reset pulse amplitudes. The intermediate states during the reset process were achieved by partially rupturing the CFs. Besides the programming scheme by varying the reset pulse amplitudes, there are other feasible methods to achieve multilevel states. For example, the two equivalent pulse programming schemes [28] can give the same resistance modulation capability: one is to linearly increase the reset pulse amplitudes; the other is to exponentially increase the reset pulse width. The two schemes are equivalent because of the observed voltage-time relationship in the switching dynamics: the oxygen ion migration velocity exponentially depends on the applied electric field [28].
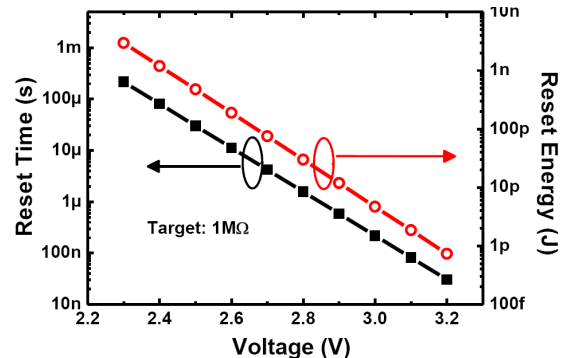
Fig. 7 shows the simulated reset time and reset energy versus the applied voltage according to our developed oxygen ion migration model [27].

Both schemes can achieve the target multilevel resistances. Therefore, we came to a question which programming scheme is better? We performed the transient current response waveform measurement to evaluate the energy consumption of

these two schemes: to obtain the same target resistance (~50 kΩ) from an initial resistance (~10 kΩ), a shorter and larger pulse (-2.3 V/50 ns) would consume 7.4 pJ while a longer and smaller pulse (-2 V/500 ns) would consume 60.9 pJ [28]. Fig. 7 shows the simulated reset time and reset energy versus the applied voltage according to an oxygen ion migration model [28]. We can see that with the increase of voltage, the reset time and reset energy exponentially decreases, and sub-pJ energy consumption is achievable in RRAM operations. The programming scheme with varying pulse amplitudes is an energy efficient scheme for future high-speed RRAM arrays for multi-bit application.
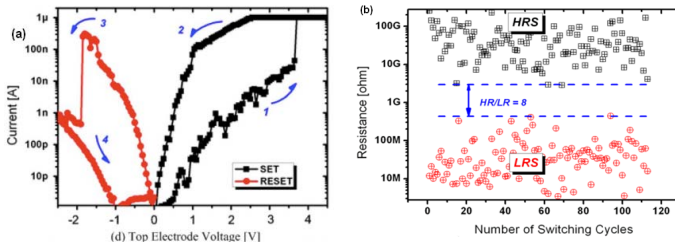

Fig. 8 (a)Al/AlOx/Pt RRAM using ALD AlOx with 1μA programming current. (b) Resistance ratio is about 8. The HRS has very high resistance.

B. Al2O3 based RRAM using Atomic Layer Deposition (ALD) with 1μA RESET Current

One challenge for the RRAM device is power consumption. Most RRAM devices reported in the early literatures show typical switching current in the order of mA or hundreds of μA. Using ALD grown oxide for Al/Al$_2$O$_3$/Pt, Wu et al. [29] have demonstrated exceptionally low reset current of ~1μA as shown in Fig 8. The low switching current substantially increases the LRS resistance to several hundreds of MΩ and this can potentially allow for ultra-large scale memory arrays without selection devices because the sneak leakage currents are significantly reduced due to the high LRS resistance.

IV. CONCLUSION

In this paper, we reviewed some of the recent work on phase change and resistive change memories. The key challenge facing the PCM is in the reduction of its reset current and mitigating the effect of drift. Understanding the physical mechanism of switching and drift can go a long way in making reliable multi-level PCM arrays. For RRAM, the major challenge lies in improving the uniformity in the device switching behavior and understanding the physical mechanism involved in switching.

V. ACKNOWLEDGEMENTS

VI. REFERENCES

[1] R. Bez and P. Cappelletti, "Flash memory and beyond", IEEE VLSI-TSA 2005, pp 84-87.

[2] H.-S. P. Wong et al., "Phase Change Memory", Proc. IEEE. vol. 98, no. 12, pp. 2201-2228, 2010.

[3] Pirovano et al., "Scaling analysis of Phase Change Memories", IEDM Tech. Digest 2003, pp 29.6.1

[4] G. Servalli, "A 45nm generation Phase Change Memory technology", IEDM Tech Digest 2009. pp 1-4.

[5] K.J. Lee, "A 90nm 1.8V 512Mb Diode-switched PRAM with 266MB/s read throughput", IEEE Journal of Solid State Circuits, vol. 43, no. 1, pp 150-162, 2008.

[6] Marissa A. Caldwell, Simone Raoux, Robert Y. Wang, H.-S. Philip Wong and Delia J. Milliron, "Synthesis and size dependent crystallization of colloidal germanium telluride nanoparticles" J. Mater. Chem, pp.1285-1291, 2010

[7] S. Raoux et al., "Phase change materials and their application to random access memory technology", Microeleectronic Engg., vol. 85, no. 12, pp 2330-2333, 2008.

[8] S. Raoux, W. Welnic and D. Ielmini, "Phase change materials and their application to non-volatile memories", Chem. Rev., vol. 110, no. 1, pp 240-267, 2010.

[9] H.Chung et al., "A 58nm 1.8V 1Gb PRAM with 6.4MB/s Program BW", IEEE ISSCC, 2011.

[10] D. Ielmini et al., "Reliability Impact of Chalcogenide-Structure Relaxation in Phase-Change Memory (PCM) Cells Part I: Experimental Study. Electron Devices", IEEE Transactions on Electron Devices, vol. 56, no. 5, pp. 1070-1077, 2009.

[11] S. Kim et al., "Thermal Disturbance and its Impact on Reliability of Phase-Change Memory Studied by the MicroThermal Stage", IEEE IRPS, 2010, pp. 99-103.

[12] S. Kim et al., "Resistance and Threshold Switching Voltage Drift Behavior in Phase-Change Memory and Their Temperature Dependence at Microsecond Time Scales Studied Using a Micro-Thermal Stage", IEEE Trans. On Electron Devices, vol .58, no. 3, pp 584-592, 2011.

[13] D. Ielmini and Y. Zhang, "Evidence for Trap-limited Transport in Subthreshold Conduction Regime of Chalcogenide Glasses," Applied Physics Letters, vol. 90, 192102, 2007.

[14] M. B. Weissman, "Low-Frequency noise as a tool to study disordered materials", Annual Review of Mat. Sci, vol. 26, pp. 395-429, Aug 1996.

[15] G.B. Beneventi et al., "Analytical Model for Low-Frequency Noise in Amorphous Chalcogenide Based Phase Change Memory Devices," Jnl. Of Applied Physics, vol. 106, 054506, 2009.

[16] B.J. Bae et al., "1D Thickness Scaling Study of Phase Change Material (Ge2Sb2Te5) using a Pseudo 3-Terminal Device", IEEE IEDM Tech Digest, Dec 2009, pp 93-96.

[17] R. Jeyasingh et al., "Low frequency in Phase Change Materials", Intl. Conf. on Noise and Fluctuations, Toronto, 2011. to be presented.

[18] D Fugazza et al., "Random Telegraph Signal Noise in Phase Change Devices", IRPS 2010, pp. 743-749.

[19] H. Akinaga, and H. Shima, "Resistive random access memory (ReRAM) based on metal oxides", Proc. IEEE vol. 98, pp. 2237-2251, 2010.

[20] H.-S. P. Wong, et al. "Metal oxide RRAM", Proc. IEEE, submitted for publication.

[21] R. Waser, et al. "Redox-based resistive switching memories - nanoionic mechanisms, prospects, and challenges", *Adv. Mater. vol. 21, pp. 2632-2663, 2009.*

[22] S. Yu, and H.-S. P. Wong, "A phenomenological model for the reset mechanism of metal oxide RRAM", IEEE Electron Device Lett. vol. 31, pp.1455-1457, 2010.

[23] I. G. Baek, et al. "Highly scalable non-volatile resistive memory using simple binary oxide driven by asymmetric unipolar voltage pulses", Tech. Dig. IEDM 2004, pp. 587-590.

[24] H. Y. Lee, et al. "Low power and high speed bipolar switching with a thin reactive Ti buffer layer in robust HfO$_2$ based RRAM", Tech. Dig. IEDM 2008, pp. 297-300.

[25] H. Y. Lee, et al. "Evidence and solution of over-RESET problem for HfO$_x$ based resistive memory with sub-ns switching speed and high endurance", Tech. Dig. IEDM 2010, pp. 460-463.

[26] S. Yu, et al. "Improved uniformity of resistive switching behaviors in HfO$_2$ thin films with embedded Al layers", Electrochem. Solid-State Lett., vol. 13, H36-H38, 2010.

[27] S. Yu, et al. "Characterization of switching parameters and multilevel capability in HfO$_x$/AlO$_x$ bi-layer RRAM devices", VLSI-TSA 2011, to be presented.

[28] S. Yu, Y. Wu, and H.-S. P. Wong, "Investigating the switching dynamics and multilevel capability of bipolar metal oxide resistive switching memory", Appl. Phys. Lett., 2011, to be published.

[29] Wu, Y., B. Lee, and H.-S.P. Wong, "Al$_2$O$_3$-based RRAM Using Atomic Layer Deposition (ALD) with 1μA Reset Current", IEEE Electron Device Letters, vol. 31, no.12, pp. 1449-1451, Dec 2010.