

# Effects of Interface-Trapped Charge on the SiC MOSFET Characteristics

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## ABSTRACT

High quality SiC/SiO<sub>2</sub> interfaces are critical to the development of silicon carbide power MOSFETs, IGBTs, and MOS-controlled thyristors. In this work, we examine the effects of thermal stress on the SiC/SiO<sub>2</sub> interface of n-channel MOSFETs that had gate oxides formed by low-pressure chemical-vapor deposition on the silicon face of a 6H-SiC epitaxial layer with subsequent re-oxidization to improve the interface. These devices were found to have a pre-stress mean interface-trap density of  $5 \times 10^{11} \text{ cm}^{-2} \text{ eV}^{-1}$  at room temperature. The interface-trap density for these oxides was shown to be significantly increased by applying moderate stress (2MV/cm) at 300°C. The post-stress change in device characteristics is shown to be consistent with the stress-induced increase in interface traps.

## INTRODUCTION

The potential for silicon carbide (SiC) semiconductor devices to operate at high temperature and high power has been widely discussed in the literature for over 40 years. This potential has moved closer to realization in the last 10 years due to the commercial availability of SiC wafers. A number of different types of SiC devices have been reported in the literature and it has been noted that one advantage of SiC is that silicon dioxide (SiO<sub>2</sub>) can be grown on SiC just like it can on silicon (Si) to produce metal-oxide-semiconductor (MOS) devices. However, one of the remaining problems is the development of high-quality, high-reliability gate oxides and passivation layers to be used on SiC for high-temperature and high-power applications for all-electric vehicles. SiC MOS devices that have been demonstrated to date exhibit channel mobilities [1,2] unacceptably low for practical device applications and the quality of the gate dielectric may in fact be largely responsible.

This study has been initiated to understand the role that the fixed oxide charge  $Q_F$ , the interface-trapped charge  $Q_{IT}$ , the oxide-trapped charge  $Q_{OT}$ , and the mobile charge  $Q_M$  have on the device characteristics and how their contribution may vary when the devices are subjected to stresses simulating operating

conditions. The Army's electric vehicle applications will require electronics which are stable and reliable for extended operations (10,000 hours) at junction temperatures of 300° to 400°C.

## DEVICE DESIGN

A number of 6H-SiC MOSFETs were received from Cree Research, Inc. The devices on which we are reporting here were the output of an initial study to investigate deposited oxides for use as gate dielectrics in n-channel MOSFETs. Some studies [3] have presented the difficulties of producing thermally grown oxides on the *p*-type SiC epitaxial layer as gate oxides for *n*-channel MOSFETs. However, other studies [4] reported in the literature have shown success at producing MOS structures with low fixed oxide charge  $Q_F$  and low interface-trapped charge  $Q_{IT}$  using deposited oxides but including a re-oxidation step to produce a thin thermal oxide at the Si/SiO<sub>2</sub> interface. For the n-channel 6H-SiC MOSFETs used in this study, the deposited/re-oxidized gate oxide is 350 Å thick and was formed by low-pressure chemical-vapor deposition on the Si face of a *p*-type (doped with Al to  $5 \times 10^{15} \text{ cm}^{-3}$ ) 6H-silicon carbide epitaxial layer with subsequent re-oxidization to improve the interface [1]. The ohmic source and drain contacts are nickel and the gate metal is molybdenum. The device width and length are 20 μm and 70 μm, respectively. The room temperature drain current-drain voltage ( $I_D$ - $V_D$ ) characteristics (for several values of gate voltage) and  $I_D$ - $V_D$  characteristics (for  $V_g = 6 \text{ V}$ ) measured from 25° to 300°C for one of the SiC MOSFETs are shown in Fig. 1. The low (< 5μA) room temperature drain saturation current reflects the degraded channel mobility caused by both interface-trapped charge and fixed oxide charge. The continued drain current increase with temperature out to 300°C suggests the extent to which the channel mobility has been degraded by the presence of large numbers of interface traps.

## INTERFACE TRAP DENSITY

The development of oxides for SiC is very immature; the  $Q_F$  and  $Q_{IT}$  are especially large for the *p*-type substrate and very little has been reported on the long term stability of the interface required for the n-channel enhancement mode MOSFET. It is

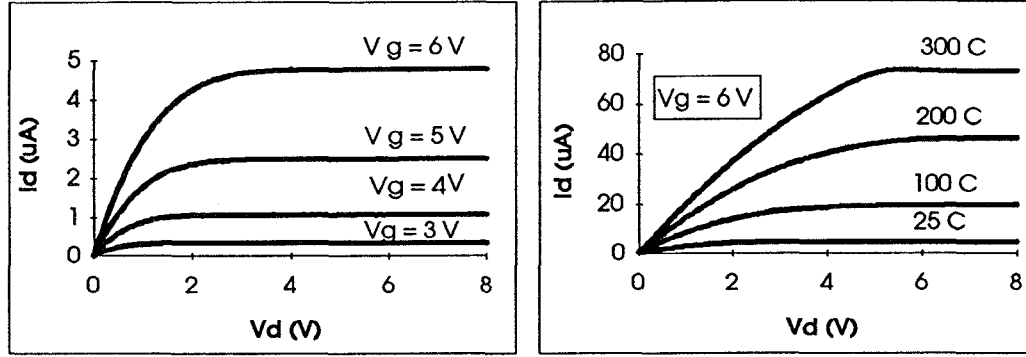
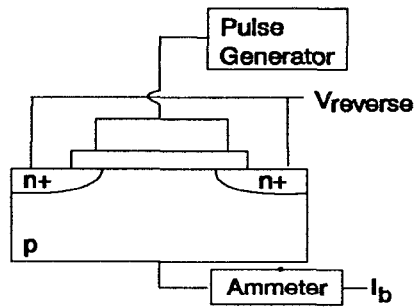


Figure 1. The drain current-drain voltage ( $I_d$ - $V_d$ ) for several values of gate voltage at 25°C and  $I_d$ - $V_g$  characteristics for  $V_g = 6$  V from 25° to 300°C for 6H-SiC  $n$ -channel MOSFET.

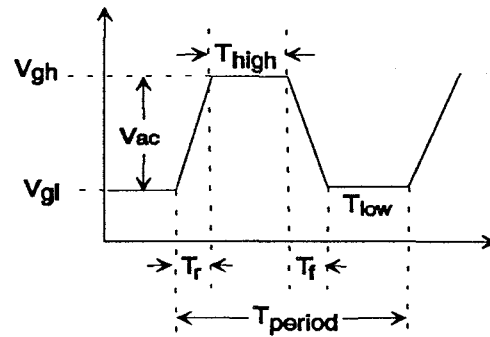
important to be able to evaluate the oxide-SiC interface in a large number of devices, both before and after the devices have been subjected to bias and temperature stresses. As discussed below, charge pumping is an electrical measurement made directly on the MOSFETs undergoing the stress and provides an immediate, direct measurement of the effects on the interface trap density in state of the art SiC MOSFETs.

The charge-pumping (CP) technique [5] consists of applying a voltage pulse to the gate of a MOSFET while the source and drain are shorted together and held at a small reverse bias with respect to the substrate (Fig. 2). The gate pulse base voltage  $V_{gl}$  and pulse height  $V_{ac}$  are adjusted to change the surface potential of the semiconductor so that the interface goes from accumulation to inversion and then returns to accumulation. During the rising edge of the pulse the semiconductor surface becomes deeply depleted and electrons are supplied to the

channel from the source and drain. Some of these electrons are captured by positively charged interface traps in the lower half of the bandgap (those that were not able to emit holes during this time frame) and neutral electron traps in the upper half of the band gap. On the falling edge of the pulse as the semiconductor is being driven back into accumulation the mobile electrons emitted from interface traps in the upper half of the bandgap during the fall time drift back to the source and drain under the influence of the reverse bias. Electrons that were captured by the interface states in the lower half of the bandgap (during rising edge of gate pulse) and negatively charged interface traps in the upper half of the bandgap (those traps that were not able to emit electrons during the falling edge of the gate pulse) recombine with majority carriers from the substrate as the surface returns to accumulation. This process results in a net charge  $Q_{ss}$  transfer (pump) to the substrate which is proportional to the interface trap density  $D_{IT}$ , and is



(2a)



(2b)

Figure 2. Experimental set-up for charge pumping measurements (a) and charge pumping signal applied to MOSFET gate (b).

given by:

$$Q_{ss} = qA_g \int D_{IT}(E) dE \quad (1)$$

where  $q$  is the electronic charge,  $A_g$  is the gate area and  $D_{IT}(E)$  is the interface-trap density at energy level  $E$  ( $\text{cm}^{-2} \text{eV}^{-1}$ ). When this pulse is repeated at a frequency  $f$  a substrate current or charge pump current  $I_{CP}$  results

$$I_{CP} = fQ_{ss} = q^2 f A_g \bar{D}_{IT} \Psi_s \quad (2)$$

where  $\bar{D}_{IT}$  is the mean interface-trap density averaged over the surface potential range  $\Delta\Psi_s$  swept during the voltage pulse ( $\text{cm}^{-2} \text{eV}^{-1}$ ). By applying a fixed amplitude gate pulse  $V_{ac}$  and stepping the gate pulse base voltage from  $V_{gl}$  less than  $V_t - V_{ac}$  to  $V_{gl}$  greater than  $V_{fb}$ , an  $I_{CP}$  vs.  $V_{gl}$  curve is produced which increases from a minimum current to a saturated level and then decreases to a minimum current level. The peak current in the saturation regime is the  $I_{CP}$  used in the calculation of  $\bar{D}_{IT}$ .

In the remainder of the paper, the number ( $N_F$ ,  $N_{IT}$ ,  $N_{OT}$ ,  $N_M$ ) of discrete charges of a particular type per unit oxide area ( $\text{cm}^{-2}$ ) and their distribution within the oxide will be discussed rather than charge density of a particular type ( $Q_F$ ,  $Q_T$ ,  $Q_{OT}$ ,  $Q_M$ ) as has been previously discussed. The relationship between these two quantities is given by  $Q_{(F,IT,OT,M)} = qN_{(F,IT,OT,M)}$  where  $q$  is the electronic charge and  $N_{IT}$  is the product of  $\bar{D}_{IT}$  and the semiconductor bandgap.

#### INTERFACE-TRAP DENSITY MEASUREMENTS ON SiC DEVICES

CP measurements were first made on high quality Si-SiO<sub>2</sub> MOSFETs to calibrate the measurement equipment and the method. Fig. 3(a) shows the charge pump current  $I_{CP}$  plotted as a function of gate base voltage  $V_{gl}$  for a 2 V fixed amplitude

pulse  $V_{ac}$  applied to the gate. Using the gate area ( $2.0 \times 10^{-6} \text{cm}^2$ ) for this special closed geometry charge pump device and the gate pulse frequency of 100 kHz a  $\bar{D}_{IT}$  of  $1.4 \times 10^{10} \text{cm}^{-2} \text{eV}^{-1}$  was calculated for a peak  $I_{CP}$  of 200 pA measured over a surface potential sweep of  $E_i \pm 0.22 \text{eV}$  or over the central 40 % of the Si 1.1 eV bandgap.

CP measurements as described above were made on six unstressed (as delivered) 6H-SiC n-channel MOSFETs (as described earlier) at room temperature (RT) and the associated interface state densities were calculated. The charge pumping parameters were adjusted so that the surface potential sweep during the measurement was over the range of energies  $E_i \pm 1.1 \text{eV}$  or over the central 75 % of the 6H-SiC 2.9 eV bandgap. The six devices were chosen randomly from a lot of 20 engineering devices and the mean interface state density  $\bar{D}_{IT}$  for five of these devices was  $5.0 \pm 0.5 \times 10^{11} \text{cm}^{-2} \text{eV}^{-1}$  at one standard deviation. The sixth device was eliminated from the mean average since its  $\bar{D}_{IT}$  was beyond two standard deviations of the mean average and was  $2.6 \times 10^{11} \text{cm}^{-2} \text{eV}^{-1}$ .

Figure 3(b) gives a typical plot of charge pump current  $I_{CP}$  vs. gate pulse base voltage  $V_{gl}$  for the devices measured. The peak charge pump current given in this figure is 1.9 nA and is equivalent to a  $\bar{D}_{IT}$  of  $5.5 \times 10^{11} \text{cm}^{-2} \text{eV}^{-1}$ . Note that the rising and falling edges of the SiC CP curve are not nearly as symmetrical and exhibit large current tails when compared to the Si CP curve (fig. 4a). Also note that the SiC  $I_{CP}$  saturation is not constant but gradually decreasing as the  $V_{gl}$  increases from -7.6 V ( $V_{gl} > V_t - V_{ac}$ ) to -3 V (flat band voltage). Such asymmetries are due to the variation in the CP threshold and flat band voltages in the vicinity of the source and drain which are caused by lateral variations in the doping profile, increasing non-uniform distributions of  $N_{IT}$ ,  $N_F$  or  $N_{OT}$ , or some combination of these [6].

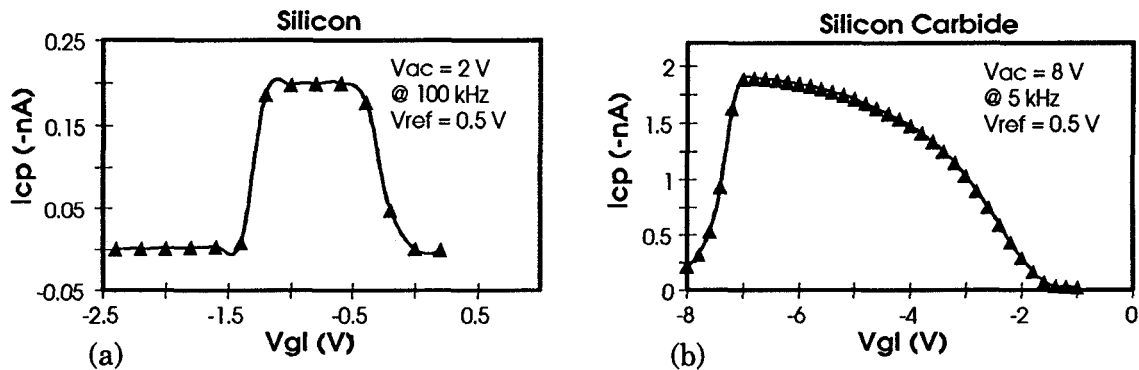


Figure 3. Charge pump current  $I_{CP}$  as a function of gate pulse base voltage  $V_{gl}$  for (a) Si-SiO<sub>2</sub> MOSFET and (b) SiC-SiO<sub>2</sub> MOSFET.

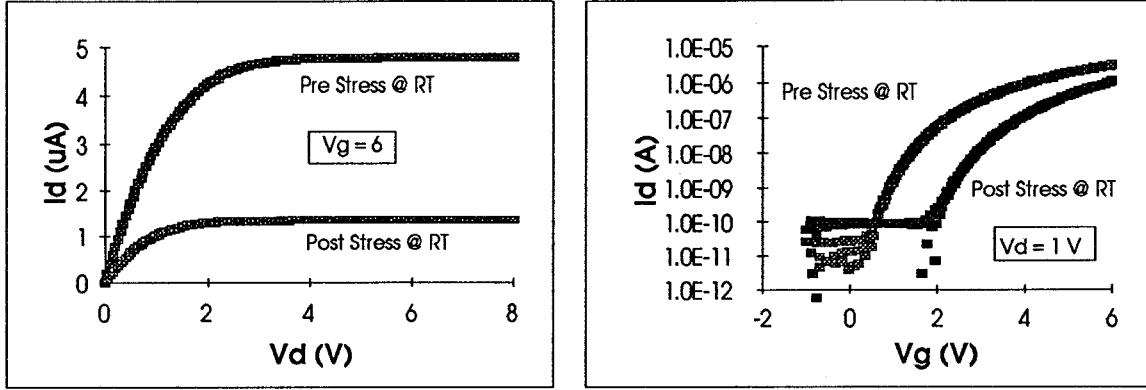


Figure 4. Comparison of pre-stress and post-stress  $I$ - $V$  characteristics for 6H-SiC  $n$ -channel MOSFET with deposited re-oxidized gate oxide.

### STRESS EFFECTS

Charge pump current measurements were made on the SiC device with the lowest interface state density at room temperature before and after the device was subjected to moderate electrical stress at temperature. CP measurements were not made during the stress due to the leakage currents occurring at high temperature. The stress bias consisted of applying an 8 V fixed-amplitude gate pulse with a base voltage of -7 V at a frequency of 5 kHz while the source and drain were dc-biased at 0.5 V; all bias voltage was referenced to the substrate at 0 V. This stress was applied during heating steps and interrupted only when  $I$ - $V$  measurements were made. The duration of the heating steps were: 30 minutes each at 100° and 150° C, 45 minutes each at 200° and 250° C, and the final step at 300° C lasted one hour. Figure 4 compares the pre-stress and post-stress  $I$ - $V$  characteristics measured at room temperature for

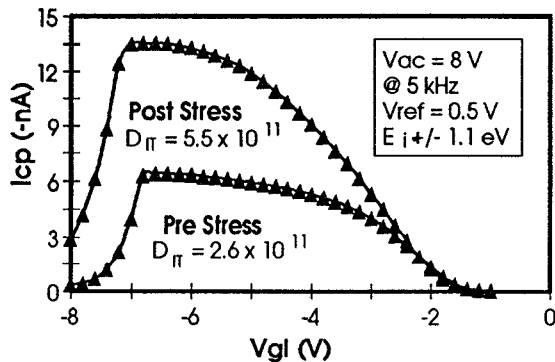


Figure 5. Pre-stress and post-stress charge pump current  $I_{cp}$  as a function of gate pulse base voltage  $V_{gl}$  for 6H-SiC  $n$ -channel MOSFET with deposited re-oxidized gate oxide.

the device. The plot of  $I_d$  vs.  $V_d$  for  $V_g = 6$  V shows the post-stress measured drain saturation current decreased by about a factor of 3.5 from the pre-stress value. The plot of  $I_d$  vs.  $V_g$  for  $V_d = 1$  V shows a positive shift in the post-stress threshold voltage shift of 1.8 V from the pre-stress value.

The pre-stress and post-stress room temperature measurements of charge pump current vs. gate base voltage are compared in figure 5. The post-stress peak  $I_{cp}$  is shown to have increased by more than a factor of two over the pre-stress value; the mean interface state density associated with these pre- and post stress peak currents are  $2.6 \times 10^{11} \text{ cm}^{-2} \text{ eV}^{-1}$  and  $5.5 \times 10^{11} \text{ cm}^{-2} \text{ eV}^{-1}$ , respectively. The 110% increase in post-stress  $\bar{D}_{IT}$  over the pre-stress value is equivalent to a net increase in interface states  $N_{IT}$  of  $8.4 \times 10^{11} \text{ cm}^{-2}$  over the pre-stress value. (Recall that  $N_{IT}$  is  $2.9 \text{ eV} \times \bar{D}_{IT}$ , where 2.9 eV is the SiC bandgap.) The positive shift in threshold voltage and decrease in drain saturation current shown in Fig. 5 is consistent with this 110% increase in  $\bar{D}_{IT}$ , as will be discussed in the following section.

### DISCUSSION

In the following analysis it is assumed that the effect due to electrical stress-induced changes in  $N_{OT}$  and  $N_{IT}$  on the charge in the conduction channel can be expressed as

$$Q_N(y) = -C_{ox}(V_g - V_T - V_C) - q\delta N_{OT} + q\delta N_{IT}, \quad (3)$$

where  $C_{ox}$  is the gate oxide specific capacitance and  $V_C$  is the potential along the channel. Note that  $N_{OT}$  is a centroid weighted quantity as if all the charge is located at the interface.  $N_{OT}$  can be either positively or negatively charged and  $N_{IT}$ , although it changes polarity depending on the SiC surface potential as mentioned earlier, is considered here to be negatively charged under the strong channel inversion

condition. Although fixed charge  $qN_F$  affects both inversion charge and channel carrier mobility, we assume that it does not change during the stress at 300° C based on results reported on Si MOS devices [7]; and hence is not included in eq. 3.

By substituting eq. 3 into the gradual channel approximation [8] for the potential rise along the channel, and taking into account that the pre-stress drain current must be reduced by the post-stress mobility, and by integrating from source to drain, the following relation giving post-stress drain current for moderate drain voltages ( $V_{DS} < V_T$ ) results

$$I_D = u_N C_{ox} \frac{W}{L} [V_g - V_T - 0.5V_D] V_D + u_N \frac{W}{L} V_D q (\delta N_{OT} - \delta N_{IT}) \quad (4)$$

where  $\mu_N$  is the post-stress degraded mobility and  $V_T$  is the linearly extrapolated threshold voltage. Hence the post-stress drain current can be expressed as a decrease in the pre-stress drain current caused by the degradation in channel mobility (first term) and the reduction in inversion charge (second term), both caused by the increase in  $N_{IT}$ .

By substituting the identity,  $V_{DSat} = (V_g - V_T) + V_S$  into Eq. 4 a similar relation results giving post-stress drain saturation current for  $V_S = 0$  V

$$I_{Dsat} = u_N C_{ox} \frac{W}{2L} [V_g - V_T]^2 + u_N \frac{W}{L} q (\delta N_{OT} - \delta N_{IT}) (V_g - V_T) \quad (5)$$

The post-stress threshold can be expressed as a function of the change in the flat band voltage due to the change in the oxide

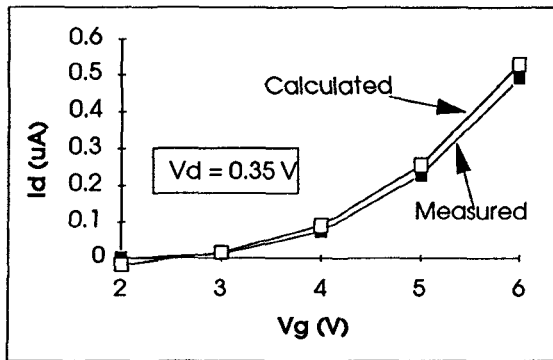


Figure 6. Comparison of calculated to measured post-stress drain current as a function of gate voltage for  $V_d = 0.35$  V for 6H-SiC  $n$ -channel MOSFET with deposited re-oxidized gate oxide.

charge by

$$V_T = V_{T0} + \delta V_{FB} = V_{T0} - q \frac{\delta N_{OT}}{C_{ox}} + q \frac{\delta N_{IT}}{C_{ox}} \quad (6)$$

where  $V_{T0}$  is the pre-stress threshold and  $N_{OT}$  is again a centroid-weighted quantity as if the charge is all located at the interface.  $N_{OT}$  is the net oxide trapped charge which includes both holes and electrons that may have been injected into the oxide under the negative bias stress. In contrast, if all  $N_{OT}$  were to be located adjacent to the gate, it would have no effect on  $V_{FB}$ . Therefore, redistribution of any existing prestress charge away from the interface which occurs during high temperature electrical stress could cause a threshold shift, even without any net change in total oxide charge.

The above analysis was applied to the calculation of the post-stress characteristics of the device initially assuming that the  $N_{OT}$  did not change significantly during the electrical and thermal stress. The pre- and post-stress thresholds were extracted from linear extrapolation of the  $I_D$  vs.  $V_g$  curve for  $V_D = 0.35$  V. The pre- and post-stress channel mobilities were calculated using the following relation applied to measurements taken on the device in the linear regime for a family of  $I_D$  vs.  $V_D$  curves for several gate voltages:

$$I_D = u_N C_{ox} \left( \frac{W}{L} \right) V_D (V_g - V_T) \quad (7)$$

The post-stress current in the linear regime was calculated for several gate voltages for  $V_D = 0.35$  using equation 4 and the CP-measured  $\delta N_{IT}$  of  $8.4 \times 10^{11} \text{ cm}^{-3}$ . The calculated post-stress linear currents are compared to the measured post-stress currents in figure 6 and are shown to be in good agreement (within 15 %). For example, the calculated and measured post-stress drain currents for  $V_g = 5$  V are 0.26  $\mu\text{A}$  and 0.23  $\mu\text{A}$ , respectively. The pre-stress and post-stress calculated mobilities for  $V_g = 5$  V are  $22 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$  and  $12 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$ , respectively. Hence, the post-stress-measured drain current is reduced from the pre-stress-measured value of 0.81  $\mu\text{A}$  due to the nearly 50 % reduction in channel mobility and the reduction in mobile inversion charge resulting from an increase in  $N_{IT}$  of  $8.4 \times 10^{11} \text{ cm}^{-3}$  due to the stress. The favorable comparison of poststress calculated to measured drain currents of figure 6 suggests the initial assumption that the stress produced little change in  $N_{OT}$  is valid. It is also noted that the comparison in this figure also shows that the calculated post-stress drain current is an overestimate. This is consistent with the fact that the increase in interface traps has been underestimated by using the value of  $\delta D_{IT}$  of  $2.9 \times 10^{11} \text{ cm}^{-3}$  averaged over the energy range of 2.2 eV and applying this estimate to the entire 2.9 eV bandgap.

By evaluating equation 6 for the post-stress change in threshold voltage, it is found that the voltage shift due to the CP-measured  $N_{IT}$  accounts for about 80 % or 1.4 V of the total

positive threshold shift of 1.8 V. Hence, suggesting that as a result of the electrical stress either a redistribution of positive oxide charge away from the interface has occurred or a net negative change in  $N_{OT}$  has occurred due to electron injection. Both explanations are certainly plausible since the negative stress gate bias applied at high temperature could have caused either of the suggested effects. A portion of this unexplained 0.4 V threshold shift is also due to our underestimation of the net change in interface trap density as previously mentioned.

#### CONCLUSIONS

Improvements in quality of the oxides on SiC are needed before the potential for high temperature power MOSFETs, MCTs and IGBTs can be realized. Based on these results and others reported in the literature, the initial values of  $N_F$  and  $N_{IT}$  need to be reduced through careful oxide growth studies. Also, the stability of the oxides subjected to high temperature operation needs to be improved. The charge pumping technique, we believe, is a useful tool to support this research.

Values for  $N_F$  of less than  $1 \times 10^{11} \text{ cm}^{-2}$  and for  $N_{IT}$  of less than  $1.5 \times 10^{11} \text{ cm}^{-2}$  ( $\bar{D}_{IT}$  of less than  $5 \times 10^{10} \text{ cm}^{-2} \text{ eV}^{-1}$ ) have been suggested as reasonable goals by Lipkin and Palmour [4]. Progress toward these goals for thermally grown oxides have been reported by Lipkin et al [2] for MOS capacitors on p-type substrates with  $\bar{D}_{IT}$  of  $3 \times 10^{10} \text{ cm}^{-2} \text{ eV}^{-1}$  but with still relatively large  $N_F$  of  $7 \times 10^{11} \text{ cm}^{-2}$ . Even when the technology goals are met, the long term stability of these oxides will need to be confirmed at temperatures up to 500° C.

In this initial study of stress effects in 6H-SiC n-channel MOSFETs with deposited/re-oxidized gates, we have suggested that interface-trap build-up is the dominant oxide effect responsible for the degradation of the device characteristics. Systematic studies of the effects of all components of the oxide charge on the device characteristics of unstressed, as well as bias-temperature stressed, state-of-the-art SiC MOSFETs need

to be performed. Future studies should also measure the temperature-dependent effects of interface-traps on the device performance.

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