

Hybrid Integration of III/V Lasers on a Silicon-on-Insulator (SOI) Optical Board.

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Abstract- A multipurpose optical platform in SOI technology is presented. Hybrid integration of the active devices is realised by AuSn solder technology. The device adjustment by passive self-alignment is in the 1 μm tolerance range.

I. INTRODUCTION

The still increasing traffic in optical communication networks now reveals new bottlenecks in the infrastructure, located in the metropolitan area networks (MAN), the local area networks (LAN) and access networks. These high volume markets are in need of a new generation of products, particularly with respect to optical and electro-optical components. At the same time new technical requirements arise, such as compactness, performance, reliability and reduced assembly costs. The main driving force today is “low cost” rather than high bandwidth.

Hybrid integration is a promising way to achieve these requirements. Therefore active optical components, e.g. photodiodes or lasers, should be flip-chip mounted on optical boards. The Silicon-on-Insulator (SOI) material system is well qualified to serve as optical platform. SOI material is today applied for a variety of optical components, like microring resonators [1], modulators or switches [2].

The high refractive index contrast allows small dimension of the devices. Furthermore, SOI is employed in the VLSI-technologies as well, therefore the optical and electronic parts are compatible, and established processes for fabrication can be used.

A replacement of the conventional mounted fibre based transmitter and receiver devices by optical boards would reduce the subcomponents and as well lower the mounting costs.

In hybrid integrated optoelectronics, a critical and costly factor is the high-precision alignment of the optical axes of devices and waveguides. This problem can be solved by using passive self-alignment.

II. CONCEPT

Based on hybrid integration of III/V lasers on a SOI optical board, a versatile integration concept is presented. The precise mechanical integration of the active devices is based on a passive self-alignment process. Especially designed solder bumps, adjustment planes and standoffs are used.

Figure 1 gives an overview of the SOI motherboard, which consists of three planes. The first plane, realised in the silicon top layer, comprises waveguides, passive components and standoffs. Single mode rib waveguides are used for guiding and manipulating light on the board. The second plane consists of parts of the buried oxide and acts as an adjustment plane for the vertical alignment. Finally, the solder bumps and electrical coplanar transmission lines are placed in a third plane realised by deep etching (about 12 μm) through the buried oxide into the silicon substrate. Eutectic gold-tin (80Au20Sn) solder bumps deposited on the third plane are used for the electrical connection of active devices as well as for the precise passive alignment process.

The active components are adapted to the SOI board: Chemically assisted ion beam etched (CAIBE) trenches are implemented in the active chip as counterparts to the board

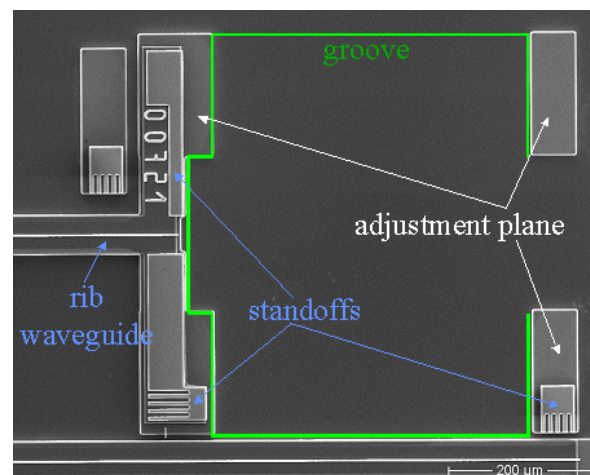


Fig. 1. SEM picture of the hybrid integration region of the optical board. Three different planes are etched into the SOI board to ensure a precise alignment of the active component. No metallisation is shown.

standoffs. For the laser device alignment tolerances ($\pm 1 \mu\text{m}$) are accomplished by the monolithic integration of an optical spot-size converter. The geometry of the SOI waveguide is chosen to match the taper field distribution.

III. FABRICATION AND RESULTS

A $1.55 \mu\text{m}$ buried heterostructure (BH) $\lambda/4$ phase-shifted DFB laser based on the InGaAsP/InP material system has been realised. The laser diode consists of a $300 \mu\text{m}$ $\lambda/4$ phase shifted DFB section and a separate $200 \mu\text{m}$ spot size converter region. The component has the potential to be directly modulated up to 10 Gbit/s in a coarse wavelength division multiplexing (CWDM) system. The laterally tapered spot-size converter section is designed as an integrated twin guide (ITG) coupled passive waveguide. For that purpose no additional epitaxial growth step is required. In detail the laser is described in [3].

For the fabrication of the optical board, bonded-and-etched-back SOI (BESOI) wafers with a silicon top layer of about $H=4 \mu\text{m}$ are used. The rib waveguide width W is chosen to $W=3.2 \mu\text{m}$. In order to achieve the single mode condition the etching depth is $(H-h) \leq 2 \mu\text{m}$. The fabrication process consists of three photolithographic masks, as mentioned above. All three etching steps are realised by fluorine based reactive ion etching (RIE) at low substrate temperature. A robust photo resist based on polymer is used to avoid problems with the non-planar surface of the wafer during the etching steps two and three. In detail the fabrication of the SOI board has been reported in [4].

Since then, the under bump metallisation (UBM) has been developed and is realised by a dielectric layer and a stack of metal layers. The gold tin bumps are fabricated by sputtering, using an AuSn target plus an additional Sn step for fine adjustment of the eutectic ratio. The sputtered solder thickness is around $5 \mu\text{m}$. During the reflow process the AuSn retracts to a wetting under bump area. By this retraction the bump height can be adjusted.

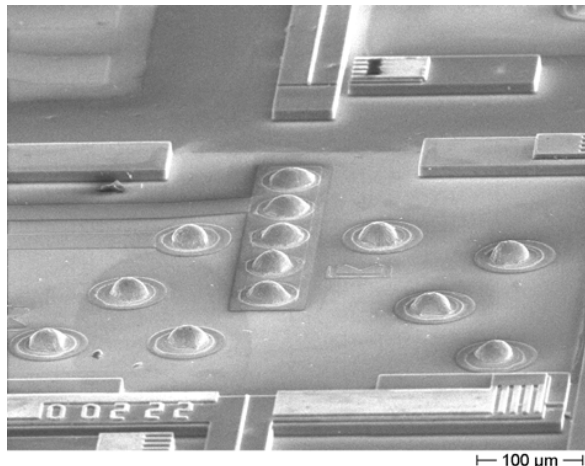


Fig. 2. View at sputtered bumps in the optical board after reflow.

This tunable bump high is essentially to get the bumps in proper contact with the pads of the laser. An overview of bumps in the board after the reflow is given in fig. 2.

For integrating the lasers on the SOI board a pick-and-place system is applied. The soldering process consists of a pre-heat step, the soldering and a cool-down ramp. An inert gas atmosphere is used for the soldering at a temperature of approximately $300 \text{ }^\circ\text{C}$. One soldered laser is shown in fig. 3.

After the soldering process, the alignments of the lasers toward the standoffs show a reproducible tolerances of $1 \mu\text{m}$. A zoom in on the left rear standoff is shown in fig. 4. Even under the SEM, a tilt less than 0.1 degree is observable on the device.

The measurements of the lasers, shown in fig. 5 and fig. 6, display good electrical and optical properties before and after the soldering process. Serial resistance increases and power decreases slightly after soldering the laser in the optical board.

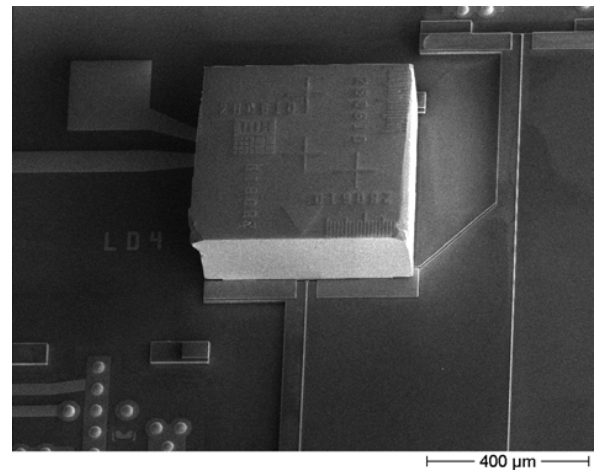


Fig. 3. A laser soldered on the optical board. The laser emits in the waveguide in front. Another bump field for further integration can be seen on the left side.

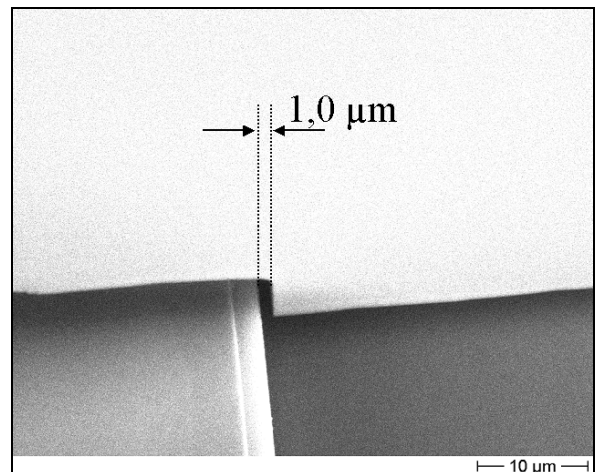


Fig. 4. Zoom in on the left rear standoff. The big block on top is the laser, the edge on the left side the standoff. The laser alignment is in the $1 \mu\text{m}$ tolerance range.

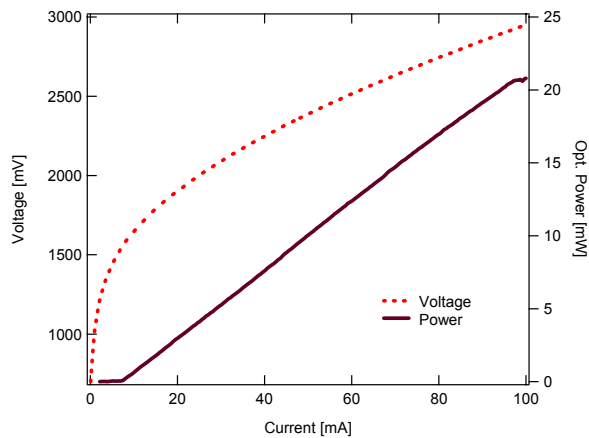


Fig. 5. Measurement of the laser before the soldering, still on the laser bar.

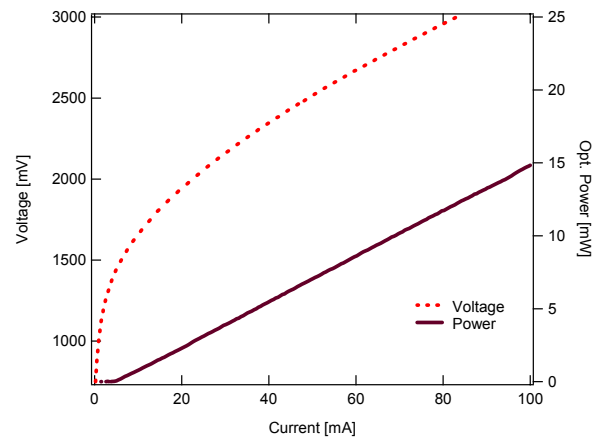


Fig. 6. Measurements after soldering the laser on a testboard.

IV. CONCLUSION

An optical board with passive self-alignment structures has been presented. The crucial process step during the fabrication of the optical board is the reliable covering of the topology in the subsequent etching steps. The active devices are integrated by use of AuSn solder technology. The lasers are designed for flip-chip mounting, further pads and standoff corners for the self-alignment are added. The alignment of the laser soldered on the optical board is in the 1 μm tolerance range. After hybrid integration there is only a small variation in the optical and electrical performance of the lasers on the SOI board.

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