

Low Temperature (LT) Grown GaAs Buffer Layers for III-V Semiconductor Processes

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Abstract

Low Temperature Grown (LTG) GaAs buffers have been shown to eliminate backgating, reduce subthreshold leakage, provide ultrashort carrier lifetimes [1], and radiation hardness [2]. However, undoped LTG buffers have shown poor reliability, poor RF performance [3], and inconsistent lot-to-lot properties. Recent p-doped LT GaAs buffers promise thermally stable material to withstand changes during annealing steps, plus improved performance over undoped LT GaAs buffers.

I. Introduction

Over 10 years ago, it was discovered by researchers at MIT that GaAs grown with As overpressure at low temperatures provided higher resistivity and shorter carrier lifetimes than observed in normally grown epitaxial or bulk GaAs [1]. Implementing LT GaAs buffer layers below FET structures eliminated backgating, and improved output resistance. This material is also utilized for ultrafast optical switches. Later it was recognized that LT GaAs buffers could provide soft error immunity for GaAs ICs [2]

The low temperature Molecular Beam Epitaxy (MBE) growth is used to provide a non-stoichiometric material with approximately 1-2% excess As in the GaAs crystal. The defects present in this low temperature grown GaAs are As antisites (As_{Ga}) and Ga vacancies (V_{Ga}). To achieve the highest resistivities, the growth temperature is required to be in a tight window between 200°C and 220°C. However, there are several problems due to this growth requirement: 1) thermocouples in production MBE systems have difficulty accurately measuring this temperature at the wafer surface, 2) below 200°C the material becomes non-crystalline, 3) above 220°C the resistivity reduces dramatically, and 4) heat from the ion sources can alter the wafer temperature. These problems make it difficult for production MBE vendors to consistently provide reproducible material.

Problems also arise in utilizing LTG material for buffers under GaAs FETs. Once annealed, (intentionally or by

continuing epitaxial growth or by implantation annealing) the properties of the undoped LTG material change. These anneals allow excess As to precipitate into clusters which reduces the strain in the non-stoichiometric layer. The As movement is assisted by V_{Ga} present in the LTG. The resulting material has high resistivity due to the As_{Ga} which act as deep electron traps. The As_{Ga} is ionized due to the p-type V_{Ga} and thus provides an excellent electron trap in the sub-picosecond regime. Recombination mainly occurs between the V_{Ga} hole trap and As_{Ga} and is on the order of several hundred picoseconds. The concentrations of these traps are on the order of $10^{19}/\text{cm}^3$ to $10^{20}/\text{cm}^3$.

Other problems associated with defect movement are As or V_{Ga} migrating outside of the intended buffer region. These point defects degrade performance by reducing activation of Si implants. Most techniques to alleviate this problem either utilize a diffusion barrier, such as AlGaAs or AlAs or place the buffer sufficiently below the FET. Both techniques can compromise performance. Wide bandgap diffusion barriers can influence the back-channel properties and may provide difficulty when using the same diffusion barrier under both N and P channel FETs. Placing the barrier far below the FET does not effectively reduce backgating.

For digital circuits, Honeywell and Motorola has used the undoped LTG buffers in their Complementary Heterojunction FET (CHFET) and Complementary GaAs (CGaAs™) processes respectively. The two major reasons to use the LTG buffers were to reduce backgating and to improve the soft error immunity for space applications [2,3]. However, the use of undoped LT GaAs buffers in some of these processes can cause reduction in transconductance if the buffer is in the vicinity of the channel. Fig. 1 shows that the LT buffer can be inserted into the Honeywell CHFET process without degrading I-V characteristics of either the N-channel or P-channel FETs. The CHFET process utilizes the LT buffer with no change to the circuit design, layout, or wafer fabrication process.

For RF devices, LT GaAs buffers have shown poor performance. Even though DC output conductance and backgating voltages have been shown to improve

dramatically, the noise performance for devices on LT GaAs buffer has been consistently poor. Diffusion of V_{Ga} from the LT buffer into the channel and/or DX centers in the AlGaAs diffusion barriers have been suggested to account for the poor performance [4,5].

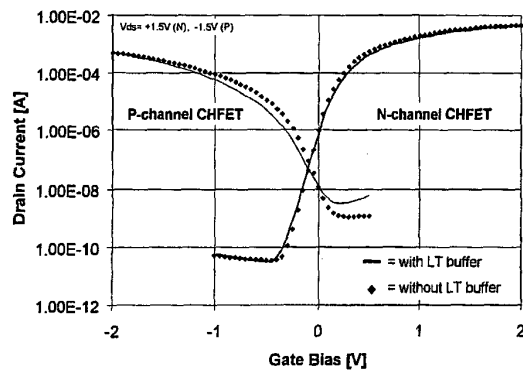


Fig. 1 - I-V plot of typical N&P-channel Complementary Heterostructure FET (CHFET) transistors from Honeywell. Gate W/L= 10/0.6um. LT buffer is located 3000 Å beneath the AlGaAs/InGaAs/GaAs heterostructure.

II. P-doped LT GaAs Buffers

In 1997, P. Specht et. al. at UCB studied the use of a p-dopant Beryllium (Be) in the growth of LTG GaAs [6]. Their initial results showed thermally stable buffers, but also improved electron trapping due to the As_{Ga} becoming doubly ionized. However, one important aspect of this work for manufacturing was that the MBE LT GaAs buffer could be grown between 275°C to 350°C, a much more suitable environment for MBE growth. The implementation of the Be dopant provided several improvements to the LT GaAs buffer. These were: 1) The Be occupied the V_{Ga} site, thus reducing vacancies in the material, 2) The Be concentration became the dominate mechanism to control resistivity other than growth temperature, 3) The Be_{Ga} acceptors stabilized the point defects (i.e. As_{Ga}) by first mechanical compensation due to the smaller Be atom and second electrically by the double ionization of the As_{Ga} . Fig. 2 illustrates the differences between undoped LT GaAs and Be-doped LT GaAs.

Controlling the p-dopant in the LT GaAs allows the flexibility of adjusting resistivity, carrier lifetime, defect stability, or breakdown field. Recent results from UCB have shown breakdown fields of 5×10^5 V/cm and resistivities greater than 10^9 ohm-cm can be achieved [7].

After UCB's initial results, UCB and Quantum Epitaxial Devices (QED) grew epitaxial GaAs and GaAs HFET structures on Be-doped LT GaAs buffers for implanting studies at the Naval Research Laboratory (NRL) and device

fabrication at Motorola respectively. The initial expectation was that the Be would diffuse out of the LTG buffer layer, similar to the problem known in Be-doped HBT bases [8].

LT GaAs parameters					
Antisite	Ga site	cond. minimize	ratio	lifetime ~As(Ga) & charge	
As_{Ga}^{+1}	V_{Ga}^{-3}	hopping	3:1	~1ps	
As_{Ga}^{+1}	Be_{Ga}^{-1}	lowest	1:1 ?	>1ps ?	
As_{Ga}^{+2}	Be_{Ga}^{-1} Be_{Ga}^{-1}	p-type	1:2 ?	<1ps	

Fig. 2 - Illustration of the interaction of As_{Ga} , V_{Ga} and Be_{Ga} dopants. The top row is undoped LT GaAs, while the last two rows illustrate low and high doped Be-LT GaAs.

The results showed very good stability in the 5000Å Be-doped LT GaAs layer. Fig. 3 is an "as grown" sample, and Fig. 4 is after a 850°C, 10 second RTA anneal. A furnace annealed 700°C for 60 minutes sample (not shown) showed stable Be, but some Si moved out of the n-type substrate.

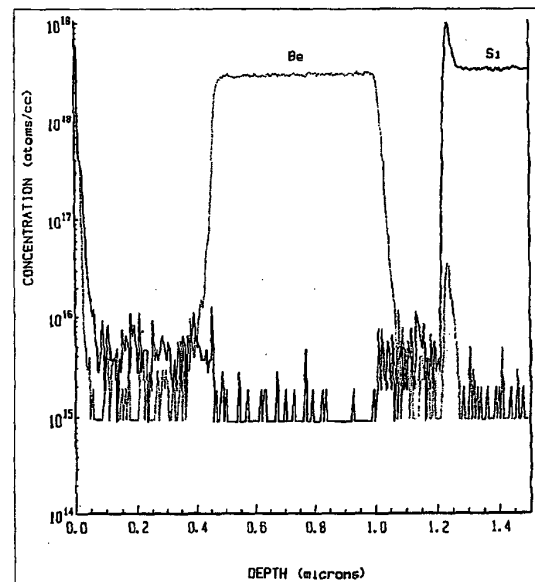


Fig. 3 - Secondary Ion Mass Spectroscopy measurement of an "as grown" sample of 4000Å of undoped GaAs epi, over 5000Å of Be-doped LTG, 2000Å undoped epi on a Si-doped n-type substrate.

Implementing LTG buffers in an implanted E/D MESFET process has also been pursued. Two issues exist:

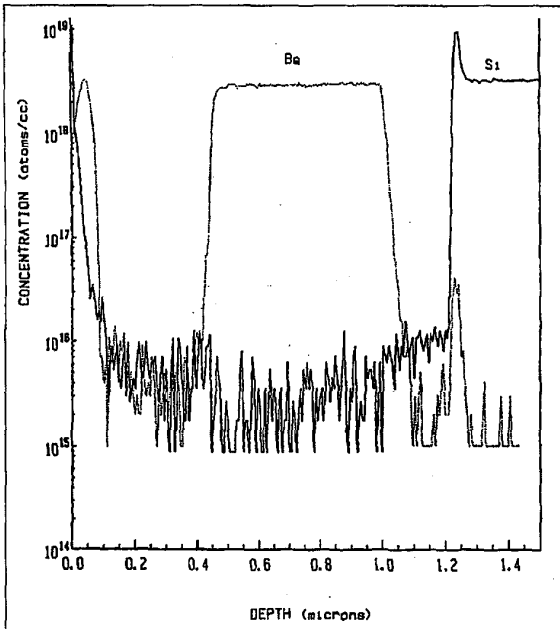


Fig. 4 – The same structure as in Fig. 3 but after a 850°C, 10 second RTA anneal.

1) GaAs bulk wafers and MBE epitaxial wafer activate differently and 2) implant anneals diffuse As and V_{Ga} out of the LTG buffer. An example of an implanted E-MESFET on an undoped buffer is shown in Fig. 5. Diffusion of point

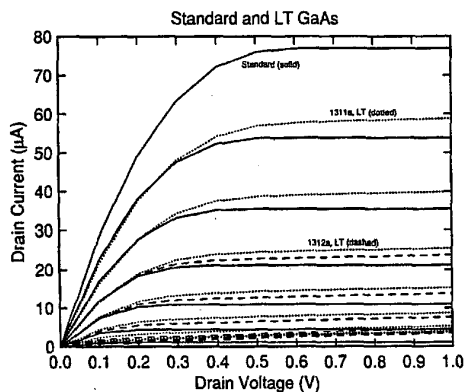


Fig. 5 – $0.8\mu\text{m} \times 10\mu\text{m}$ Ion Implanted MESFET I-V for a standard process and two undoped LTG buffers. V_{gs} max is 0.6V, and is in steps of 50 mV.

defects has shifted the threshold. Both LTG samples 1311a and 1312a were identical but different lots. This shows the problems of wafer-to-wafer uniformity.

As just shown, a challenging problem is to show good activation for ohmic or channel implants in epitaxial material above an LT GaAs buffer. Si implant studies (Table 1) at NRL have shown that activation in a 3000Å GaAs epitaxial layer above a 5000Å Be-doped LT GaAs layers is slightly improved over bulk and is equivalent to conventional epi material [9]. This was the first time activation has shown to improve with LTG buffers.

Table 1 – Implant study of 70 KeV Si implants; bulk, epi material, and epi over Be-doped LT GaAs with no diffusion barrier. All samples received an 800°C, 15 second RTA. [6].

70 KeV Si Implant	Fluence $6 \times 10^{12}/\text{cm}^2$	Fluence $4 \times 10^{12}/\text{cm}^2$
Activated in Bulk	NA	$1.9 \times 10^{12}/\text{cm}^2$
Activated in Epi GaAs	$3.0 \times 10^{12}/\text{cm}^2$	$2.3 \times 10^{12}/\text{cm}^2$
Activated in Epi / Be-LTG	$3.4 \times 10^{12}/\text{cm}^2$	$2.1 \times 10^{12}/\text{cm}^2$

Wafers grown at QED with Be-doped LTG buffers were fabricated in Motorola's CGaAs™ process in parallel with undoped LTG buffers. The Be concentrations were $8 \times 10^{17}/\text{cm}^3$ and $10^{18}/\text{cm}^3$ and buffer growth temperatures of 320°C and 295°C were used. Various ohmic implants were used. All of the N-channel Be-doped LT GaAs samples outperformed the undoped samples. The N-channel transconductance exceeded the undoped LTG buffer devices by 11% to 51%. P-channel device transconductance ranged from 14% improvement to a 38% reduction. N-channel subthreshold was one to two orders of magnitude lower than the undoped LTG devices [10]. Analysis of the QED wafers by UCB showed these first Be LTG buffers were slightly p-type increasing the P device leakage. Fig. 6 and Fig. 7 show device I-Vs.

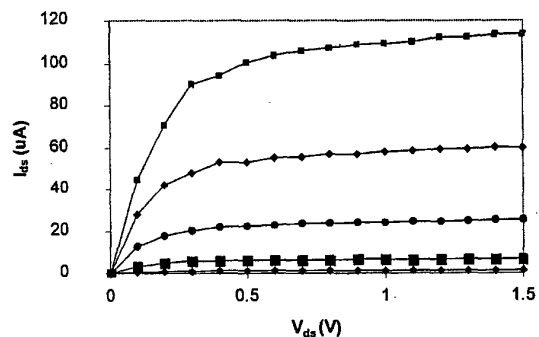


Fig. 6 shows an I-V characteristic of a $1 \times 10\mu\text{m}$ N-HFET fabricated on a Be-doped (295°C, 10^{18} Be) LTG buffer. V_{gs} is in steps of 100mV, V_{gs} maximum is 0.8 volts.

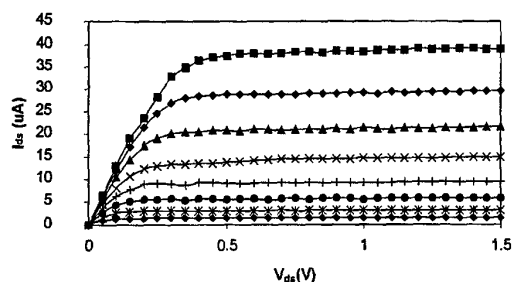


Fig. 7 shows an I-V characteristic of a $1 \times 10 \mu\text{m}$ N-HFET fabricated on a Be-doped (320°C , 8×10^{17} Be) LTG buffer. V_{gs} in steps of 50 mV, V_{gs} maximum is 0.8 volts.

III. Conclusions

The use of p-dopants in LTG buffers open a new approach to use precise control of point defects to control electrical properties and to provide thermal stability. The Be-doped LT GaAs buffer can not only provide high resistivity equivalent to undoped LTG buffers, but also provide more efficient trapping and recombination properties. The LT GaAs buffer layer, unlike insulators which block conduction (and introduce interface states), acts as a sink to absorb scattered hot carriers. Backgating effects hamper GaAs FETs (and SOI devices) however, the use of LTG buffers can provide a constant Fermi level without contacting conductive underlayers or body ties. Since the Be-doped LTG has reduced V_{Ga} 's, and no diffusion barrier exists to introduce DX centers it remains to be seen if a RF device on a Be-doped LTG buffer can show improved performance.

Thus, the ability to manufacture thermally stable LT GaAs buffer layers can:

- 1) improve performance: higher G_m than previous LT buffers,
- 2) eliminate backgating,
- 3) lower subthreshold leakage,
- 4) provide simple implementation – wafer substitution,
- 5) be applicable to other material systems – InAlAs/InGaAs P-HEMT and HBT devices,
- 6) increase soft error immunity – alpha particle sensitive and space applications.

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