Hermetic Wafer-Level Packaging for RF MEMs: Effects on Resonator Performance

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Abstract

The work presented here details the wafer-level fabrication and integration of aluminum nitride (AlN) micro resonators into hermetic micro environments. By etching cavities into the lid wafer and then bonding the lid wafer to a wafer of AlN micro resonators, a hermetic micro environment is created. After bonding, the lid wafer is thinned by plasma etching to expose individual die. This sequence presents the opportunity to perform resonator release on a wafer level while providing protection from dicing and other fabrication steps. We present here, fabrication and integration specifics on the wafer-level-packaging (WLP). Further we detail challenges encountered during the integration process including: elimination of micro voids created during eutectic wafer bonding, the use of plasma etching of lid wafers as a replacement to polish based wafer thinning, techniques to confirm hermetic environments, and significant failure mechanisms of the process limiting yield. Finally, we quantify improvements of the AlN micro resonators by correlating quality factors and integrated Pirani gauges.

Introduction

Microresonator filters are of great interest due to their small size and ability to realize many filter frequencies on a single chip [1]. To make the filters more viable in the market place, integration of these devices into a CMOS compatible facility is critical. This need further extends to the packaging of these devices. As an example, when a full wafer of these RF die are created, they must first be diced, cleaned, then the resonators can undergo a release step, such as vapor hydrofluoric acid (HF) or XeF_2 etch, on a die by die basis. Furthermore, once released the die would then need to be individually packaged. WLP has been widely touted as a potential solution for cost effective improvement in the packaging sequence. Previous efforts have demonstrated that by packaging on a wafer scale, the process time and cost can be reduced. In particular, if the resonators could be encapsulated on a wafer level, then the release step could also be performed at the wafer level thereby reducing costs and time via parallel processing of the die.

Previous efforts in WLP have successfully demonstrated a cost effective integration scheme whereby a silicon lid wafer is bonded to an AlN resonator die wafer [2]. In this previously reported integration sequence, a lid wafer is fabricated by deep reactive ion etching (DRIE) of both a shallow and deep cavity into the silicon wafer. The lid wafer then undergoes patterning and deposition of metal layers used for eutectic bonding of the lid wafer to the die wafer. Before bonding, the resonators on the die wafer are released using a XeF_2 etch of a polycrystalline silicon release layer. Once released, the die wafer is aligned to the lid wafer's shallow cavity, and the eutectic bond is performed. Following the bond, the backside of the lid wafer is then polished back until the deep cavity becomes exposed. This creates silicon caps over the resonators whose sidewall thickness is defined by the spacing between the shallow and deep cavities. If the two wafers are bonded in a vacuum environment, the resonator cavity will subsequently be under that same vacuum environment with outgassing from the interior cavity's surface reducing the level of vacuum. The wafer can then be diced with little to no degradation or slurry deposition on the encapsulated resonator.

Although a highly cost effective and successful WLP integration scheme, continual refinements of said integration sequence has led to some substantial improvements in the final product, figure 1. In this paper we discuss improvements in the integration sequence and reasoning for the modifications. , The first alteration was changing the eutectic bonding chemistry from using an Au-Ge eutectic bond (at 363 C), [3], to using an Au-amorphous Si (aSi) eutectic bond (also at 363 C), [4]. Further, the bonding stack was adjusted from using a Ti/Pt/Au/Ge/Au patterned on the lid wafer's substrate, which mated to a Au/Pt/Ti patterned metallization on the die wafers' AlN layer, to a lid wafer bonding stack of SiO2/a-Si layer bonded to Au/Pt/Ti die wafer stack. This modification dramatically reduced the number of failures from bonding as well as micro voids in the lid wafer under the bond ring.

The second significant improvement was to eliminate the lid thinning chemical-mechanical polishing step in favor of using a Bosch chemistry inductively coupled plasma reactive ion etch (ICP RIE). Using the back polishing step unnecessarily exposed the bonded wafers to a wet slurry environment and placed mechanical stresses and vibrations on the seal ring used to attached the package. By using the SF_6 fluorine rich environment, a rapid silicon removal rate could be achieved without said mechanical insults to the die while leaving the product wafer significantly cleaner than a post slurry wafer. Problems and solutions to etch uniformity will also be discussed.

To quantify the hermetic environment created, several metrics were used. For some of the die, Pirani gauges and lower frequency resonators were included on the die specifically for vacuum measurements. These devices permitted the non-gettered vacuum level to be measured and correlated; the Pirani gauges permitted direct measurement while the quality factor (Q) of a 22 MHz resonator provided an indirect measurement. The resonators also provided direct feedback on the effect of packaging on the resonators. Measurement of series resonant and anti-resonant peaks generated information such as resonant frequency and

resonant frequency shifts, Q factor, and insertion loss; by performing this measurement before and after bonding, information on how packaging affected the devices could be ascertained.

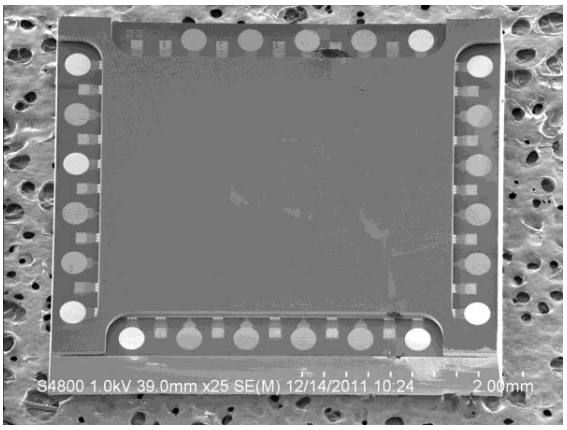

Fig 1. SEM of a hermetic packaged micro resonator die. The silicon lid has 100 um sides and top and the cavity is at approximately 8 Torr.

WLP and Integration Sequence

In general, fabrication of hermetic cavities containing micro resonator devices consists of: generating a die wafer consisting of resonators, generating a lid wafer where the cavity is defined, and then bonding of the two wafers. The die wafer is fabricated using a CMOS foundry, utilizing AlN as the active device layer [1]. The wafer then is imported into a micro fabrication lab where metallization is performed to generate the contact pads, bonding seal ring, and alignment marks. Typical metallization layers are fabricated using photoresist to define the structure, plasma sputtering deposition of the metals (20 nm of Ti / 50 nm of Pt / 500 nm of Au on the AlN layer) and then liftoff using spray solvents. The Ti and Pt layers are utilized for adhesion purposes and the Au layer thickness is defined by interconnect resistance, step coverage over layers, and bonding eutectic stoichiometry. To correct for curvature of the wafers, a compressive silicon dioxide is deposited on the backside of the die wafer until the radius of curvature is higher than 100 m. The final step is to release the pirani gauges and AlN resonators at the wafer level. A photoresist pattern is coated over the Au pads and bonding ring to protect the metals and a XeF_2 isotropic etcher is used to etch a sacrificial poly-Si layer under the AlN resonators. Etching of this poly-Si layer releases the MEMs resonators. The protect resist is then stripped using an O_2 plasma barrel asher. At this point, the die wafer is tested to ensure operation of the resonators and pirani gauges.

Fabrication of the lid wafer, described in detail later in this paper, is performed using high resistivity silicon 6" wafers. The wafers first have a thermal oxide grown of 250 nm and then 136 nm of aSi is deposited using CVD. The wafer then has 3 patterned etches into the wafer, using a photoresist etch mask, to define the aSi bond ring, pad and package cavities. Upon removal of the etch mask, the lid wafer is bonded to the die wafer using an Au –aSi eutectic bond [4–6], also described in detail later. During bonding, the chamber is pumped to 0.1 mTorr and then the wafers brought into contact and then heated. This enables the chamber surrounding the micro resonators to be evacuated prior to eutectic formation. Upon completion of bonding, the wafers are then placed in a ICP RIE chamber and a silicon etch is performed to thin the wafer. Singulation of the die is then performed and the hermetic environment adequately protects the resonators from moisture and slurry associated with dicing.

Eutectic Bonding

To create the hermetic cavity, the lid and die wafers are eutectic bonded, using Au and aSi, under vacuum thereby creating a 1-10 Torr hermetic chamber [7] [8]. The lid wafer is fabricated using a series of Bosch etches to define the lid cavity and pad cavity, described in the Lid Wafer Back-Etch section, and 250 nm of thermal oxide is grown followed by a CVD of amorphous silicon 136 nm thick. The 136 nm aSi on the lid wafer and the 500 nm Au bonding ring on the die wafer was selected to generate a eutectic stoichiometry of 3.16 % Si by weight. The wafers are aligned using an EVG 610 aligner and bonded in an EVG 520 bonder. During the bonding sequence, the chamber is first pumped out and the temperature elevated to 150 C. Since the wafers are still separated, the wafers are permitted time, 25 minutes, to out-gas thereby theoretically increasing the hermetic cavity's vacuum level by reduction of water off of the cavity surface. The wafers are then brought into contact and placed under 2 kN of force and the temperature is ramped to 400 C for a 25 minute bonding time. This fabrication sequence generates the eutectic bond and hermetic cavity encapsulating the resonator.

In the original reporting [2], a Ge-Au eutectic was used with the die wafer consisting of a metal stack of 20 nm of Ti / 100 nm of Pt / 500 nm of Au on AlN and the etched lid wafer consisting of a 20 nm of Ti / 100 nm of Pt / 440 nm of Au / 500 – 700 nm of Ge / 100 nm of Au metal stack on the silicon lid substrate. Bonding was generally performed in the temperature range of 365-375 C for times ranging from 5 min to 15 min under 2-3 kN of pressure after an extended time, 20-30 minutes, at 320 C utilized for outgassing. Although quick inspection of the wafers would indicate that a bond occurred, when the wafers continued on to lid wafer thinning, using chemical-mechanical polished (CMP), and then dicing, the majority of the dies were measured to be at atmosphere, as read by Pirani gauges. Upon further investigation, large amounts of residue were found inside the cavities indicating that a hermetic seal was never formed. Further investigation of the bond seal indicated thicker than designed eutectic layers with a significant amount of eutectic pushed into the cavity and the electrical contact pads, figure 2. Cross sectioning and SEM revealed that the eutectic extended deep into the silicon substrate and created micron sized voids [6].

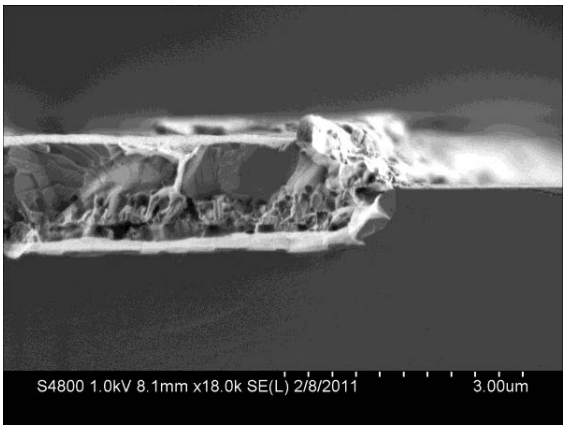

Fig 2 Cross sectional SEM of the Ge-Au eutectic bond on the lid wafer. The eutectic is seen to extend into the lid wafer's silicon substrate resulting in significant amount of voids.

Further experiments, described in detail in other reports [9], indicated that although Pt prevented diffusion of Au into the silicon substrate, a large amount of undesired silicon diffused from the substrate into the Ge-Au eutectic as shown in Fig. 2; experiments using aSi-Au eutectic also demonstrated this problem, figure 3. The extra volume of eutectic is attributed to the contribution made from the silicon substrate migrating into the Ge-Au alloy. From this understanding, oxide and nitride barriers were utilized between the substrate and eutectic bonding layers on both the lid and die [9].

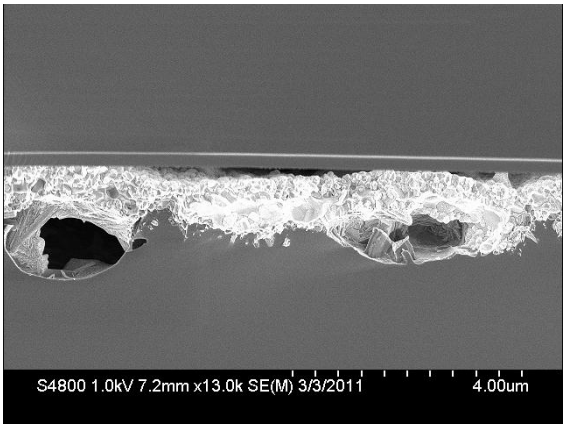

Fig 3. Cross sectional SEM of the aSi-Au eutectic bond line on experimental wafers. The eutectic is seen to extend into the silicon substrate resulting in large voids, significantly more eutectic, and is effectively blocked using 250 nm of silicon dioxide.

Although the barriers were highly effective at isolating the eutectic bond, a second difficulty arose. We observed de-bonding of the wafer stacks, indicating eutectic bond shear strength significantly lower than expected. SEMs indicated that the Ge-Au was not completely forming, figure 4. Further experimentation revealed that successful eutectic formation required bonding temperatures of 400C and bonding times of 40 minutes, figure 5. Microchemical analysis on the bonded interface indicated that the intended Ge-Au eutectic contained a large amount of Si. It is likely, given the lower bonding temperatures and times utilized for the microresonator assembly described earlier [2], that the eutectic alloy was mostly Si-Au eutectic where the silicon was introduced from the substrate. Due to the required elevated temperatures, bonding times, and increased difficulty using Ge, an aSi-Au eutectic was chosen. The current, and successful, bonding stack consists of an aSi-Au eutectic between a silicon dioxide barrier layer on the lid wafer and a AlN barrier layer on the die wafer as described earlier in this section.

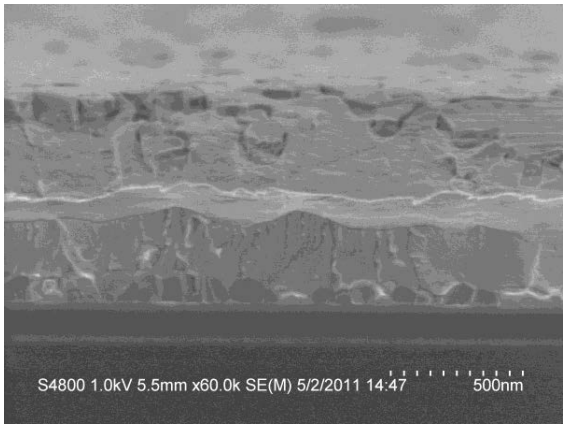

Fig 4. Cross sectional SEM of a failed Ge-Au eutectic bond after utilization of silicon dioxide barriers. Although the voiding problem is no longer observed, incomplete eutectic formation is observed with only a thin eutectic layer sandwiched between metallization layers.

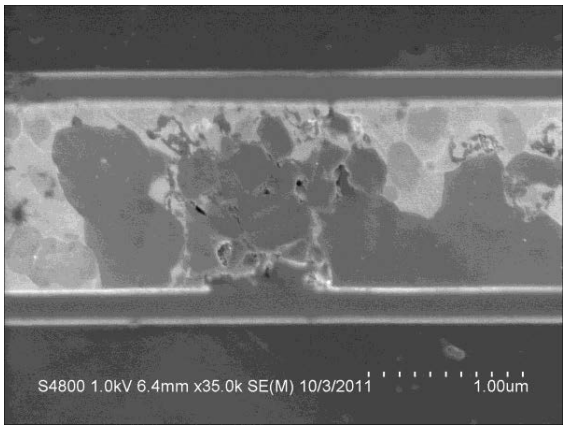

Fig 5. Cross sectional SEM of a successful Ge-Au eutectic bond utilizing oxide barrier layers. Successful Ge-Au eutectic mixing is observed without extensive voiding and no observed substrate loss. Bonding temperatures and times were required to be extensively elevated from 375 C to 400C and 10 min to 40 min.

Lid Wafer Back-Etch

Fabrication of the lid wafer was performed using a series of Bosch silicon etches to establish two major cavities, the resonator cavity and the bond pad cavity. A third, shallower, silicon etch was utilized to define the aSi bonding ring, figure 6. Upon completion of the lid wafer fabrication, the lid and die wafers are then bonded, as described earlier, and then the

lid side is back etched until the pad region becomes uncovered. This sequence leaves a 100 um thick, 5 sided cap over the micro resonators, figure 7.

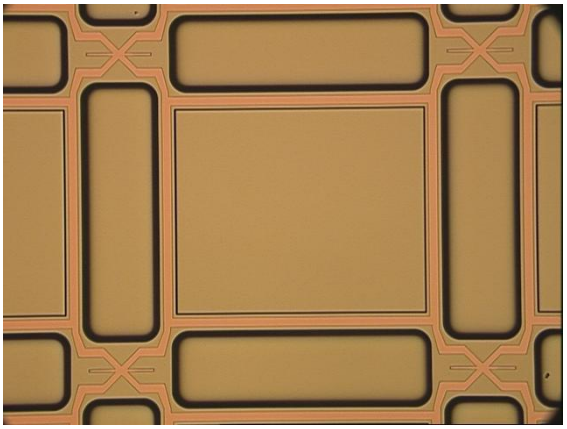

Fig 6. Optical microscope image of a lid wafer prior to bonding. The square resonator cavity is Bosch etched 20 um and the rectangle bond pad cavity is etched 120 um. The ridges between the two cavities has a 1-2 um elevated bonding ring of aSi on SiO_2.

The lid wafer fabrication began with a thermal oxidation of 250 nm followed by a low temperature CVD of 136 nm of amorphous silicon; the oxide provides the eutectic isolation from the substrate and the amorphous silicon provides the stoichiometry for the eutectic bond. These layers are first patterned with a shallow silicon/silicon dioxide etch defining a 100 um bond ring around the resonator cavity approximately 1-2 um tall. The wafer is then patterned using Az 4330 photoresist to expose both the resonator cavity and pad cavity followed by a hard bake. Then the wafer is re-patterned using Az 4330 but only to lithographically define the pad cavity. A 100 um Bosch etch is then performed; this creates the pad cavity and defines the thickness of the cavity lid. The top resist is then removed using acetone leaving both the pad and resonator cavity exposed. A second Bosch etch is then performed for 20 um. This increases the pad cavity depth to 120 um and creates a 20 um deep resonator cavity with a 1-2 um aSi/SiO_2 ring surrounding the resonator cavity. The wafer is then stripped and thoroughly cleaned. The lid wafer is then bonded to the die wafer creating a 1-10 Torr hermetic resonator cavity. Note that at this point, the contact pads are also encased in a cavity 120 um tall. It is further of interest to note that although 120 um is the goal, a distribution of etch depths across the wafer is common with the pad etch at the edge of the lid wafer approaching 10% deeper than at the center of the lid wafer.

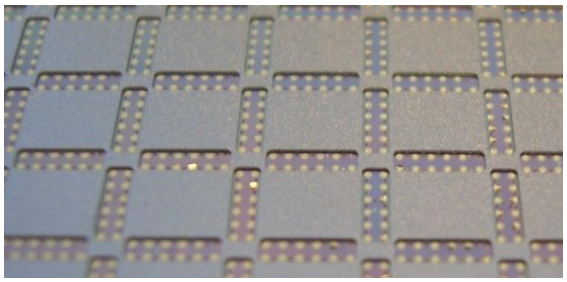

Fig 7. Image of hermetic capped micro resonator die. After the back etch, each die is encased on 5 sides with ~100 um thick silicon cap and the electrical contact pads are exposed.

Once bonded, the oxide on the back of the lid wafer is removed and the wafer stack is then isotropically etched in a low pressure SF_6 plasma in a PlasmaTherm Unaxis tool. Figure 8 is an example of a full wafer back etched to reveal the contact pads; the die can be seen in better detail in figure 7. Previously [2], it was reported that the wafer stack was thinned using CMP to ~ 550 um. This removed the silicon above the 120 um deep pad cavities immediately revealing the contact pads beside the resonator cavity. However, even with cleaning, a significant amount of silicon and polishing residue remained on the bond pads increasing insertion resistance. The mechanical stress on the 100 um thick packages also generated a significant amount of stress resulting in cracks in the package seal and flooded the resonator chambers. For this reason, the lid back etch was chosen to be performed using an ICP RIE tool. SF_6 chemistry is highly selective to the layers surrounding the pads including AlN, Au, and oxide. The plasma etch rates are also fast enough, 2-4 um/min, such that processing times remain reasonable, around 3.5 hours. Finally, since the etching is mostly chemical no stress is placed on the resonator cavities during the processing.

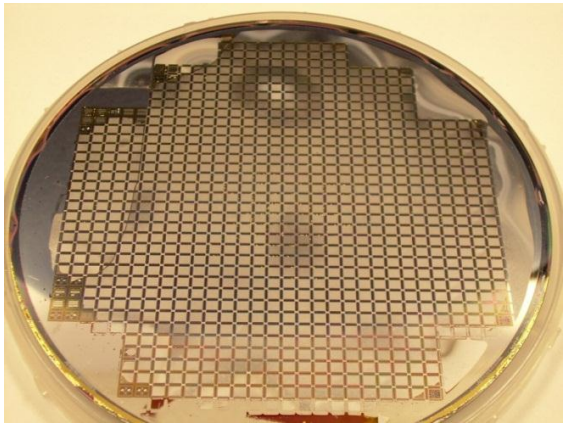

Fig 8. Image of bonded lid and die wafer after plasma back etch. The etch back process demonstrated enough uniformity to leave most of the die capped.

One of the most problematic aspects of using this back etch technique to thin the wafer is the relatively bad uniformity of etch rates across the wafer. As seen from the deep pad etch, across the wafer a 10% uniformity variation established an etch depth range of approximately 10 um. When the back side is etched over 550 um, the same

approximate uniformity initiates further problems. Keeping with the same 10% uniformity implies that the edges etch an extra 55 um before the center of the wafer pads open. Instead of simply having 100 um thick lids at the center and 35 um thick lids at the edge, we find a significant amount of die with all of the lids etched away. We approximate the outer 1"of the wafer results in lid-less devices dramatically decreasing wafer yield. We suggest that the effect causing the much faster than expected etch rates is due to a significant amount of localized fluorine loading around the pad due to the metallization; a localized silicon loading decrease from 100% to ~70%. This arises from the fact that once the silicon above the pads is completely removed, the nitride and metal locally decrease the silicon loading of the etch.

To verify this hypothesis, an etched cavity wafer was plasma bonded to blank 6 inch silicon wafer [10],[11], [12]. The bonding surface was prepared by a 10 min SC-1 clean followed by a DI rinse and 3 min O_2 RIE plasma at 50 W. The bond was annealed at 200 C for 4 hours and 2 kN in the EVG 520 bonder. Upon performance of the same back etch, we find a significantly more uniform etch profile with no un-lidded cavities, figure 9. A profilometer indicated a little over 10 um of etch variation over the entire wafer. Cross sectional SEM of the wafer indicated that although the depth of the lid (from top of the lid to pad area) maintained 100 microns at the center and ~ 90 microns at the edge, the substrate was etched 45 microns at the center and 62 microns at the edge. The implication is that once the silicon over the pad cavity was etched, the silicon pad area below also began to etch. Although there is still uniformity variation in the lid back etch, the experiment indicates that there is another contributor to the uniformity variation beginning once the pad cavities are uncovered reducing the silicon loading, a localized etch rate increase, decreases the amount of uniformity of lid thickness across the wafer.

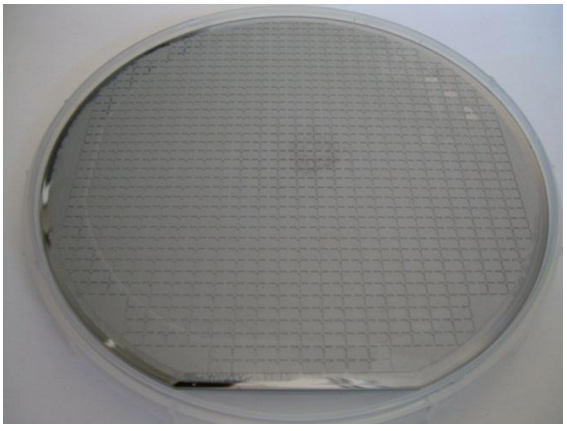

Fig 9. Image of a plasma bonded blank silicon wafer to lid wafer after back etch. Increased uniformity in this wafer indicates that on micro resonator wafers, a rapidly increased localized etch rate decreases the yield.

One technique used to mitigate the variation in the lid back etch, is by using a 1.5 inch wide ring of oxide deposited around the outside of the lid wafer. The lid back etch is then performed to etch the lid wafer's center down approximately 50 um while the edge of the wafer is protected. The oxide halo is then removed and the lid back etch then continues normally. This method permits the faster etch rates on the edge to catch up with the wafer center's 50 um head start approximately at the time of when the etch begins to reach the pad cavity. This technique is highly successful in achieving improved uniformity across the wafer but does require careful monitoring of the etch back process so that the wafer's edge and center thickness expose the pad areas simultaneously.

A second technique investigated here is the use of silicon on insulator (SOI) wafers as the lid. The SOI consists of a high resistivity top silicon layer of 150 um, with a buried oxide layer of 2 um. The normal lid fabrication sequence is then applied to the top silicon wafer. As a verification of this technique, the lid was eutectic bonded to a 6" silicon wafer with the following metallization stack: 500 nm Au / 50 nm Pt / 20 nm Ti / 250 nm SiNx. The lid was then back etched using the previously described chamber conditions. Due to the high etch selectivity of silicon to oxide the etch effectively comes to a stop when the buried oxide layer is reached. The pad cavity then is exposed with only the thin oxide over the top; the thin oxide layer is slightly deflected inward due to the vacuum environment created, figure 10. For this experiment, the initial Bosch pad etch was again deeper on the edges than the center by approximately 10 microns leaving the center pads chambers still isolated from the front side silicon. However, based on these results, we speculate that the silicon lid thinning (back side) and pad (120μm front side) etches could be landed on the buried oxide resulting in highly uniform thickness encapsulated wafer cavities.

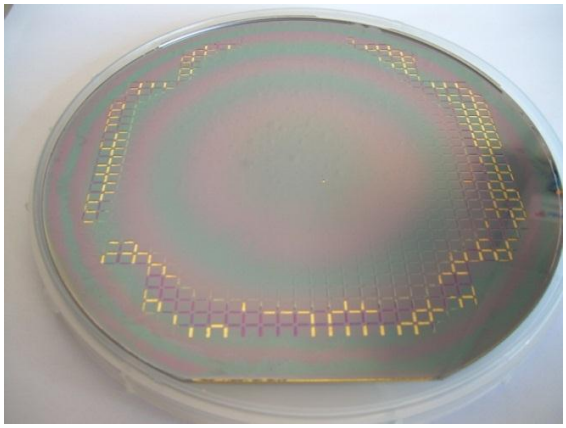

Fig 10. Image of a SOI lid wafer eutectic bonded to a blanket Au/Pt/Ti/SiNx. Although the lid fabrication did not stop on the oxide, the lid back etch process successfully landed on the BOX as observed by the optical rings.

Hermetic Cavity Testing

Upon completion of lid back etch, the contact pads for each die are available for probing. This permits testing of Pirani gauges and a low frequency, 22MHz, AlN resonator [13]. For each reticle, 2 of the 15 die contain pirani gauges and 1 of the 15 die contain both a pirani gauge and a 22MHz resonator. The pirani gauges are constructed using the aluminum and AlN layers also utilized for the micro resonators. During the fabrication sequence, as the resonators

are released, the pirani gauges are also undercut leaving two anchors to serve as mechanical supports and only path for conductive thermal loss. The geometrical design of the gauges establish an approximate 5KΩ nominal resistance at room temperature and standard atmosphere and are most sensitive in the 0.1-10 Torr pressure regime; essentially, higher pressures permit a thermal conduction to substrate via gas molecules and in the low pressure regime the resolution is limited by thermal conduction via the support anchors. By measuring the small signal resistance ratio of high to low injection current levels of the pirani gauges, the pressure can be determined. A representative example of the released pirani gauge and 22 MHz resonator is shown below in figure 11.

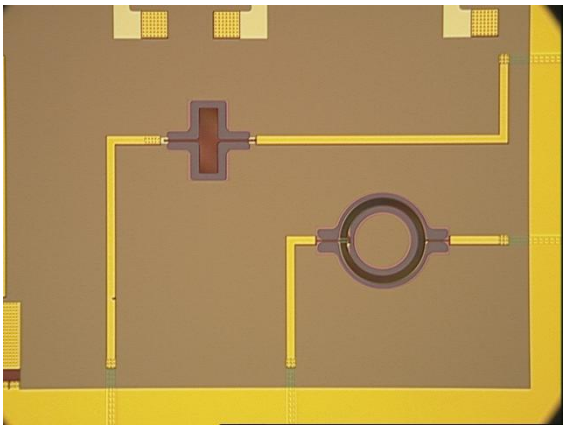

Fig 11. Image of a released pirani gauge and 22 MHz microresonator utilized for measuring vacuum in the hermetic micro resonator cavities.

To calibrate the gauges, 7 pirani gauges were placed in a vacuum chamber and their resistance ratio measured at specified levels of vacuum. These data were then fitted to a 1/x function, where the resistance ratio was the x parameter and all subsequent pirani measurements referenced to this calibration curve equation:

$$P = \frac{2.431}{(R_r - 1.101)},$$

where P is the pressure in Torr, and R_r is the small signal resistance ratio. The figure below illustrates a wafer map of reticles (defined by red lines), and individual die (blue squares) of a standard WLP micro resonator wafer. The shaded blue circle represents the usable potentially hermetically packaged area from one particular wafer displayed on a wafer map, figure 12. From 30 measurable pirani gauges, 21 indicated a level of vacuum around the 10 Torr range.

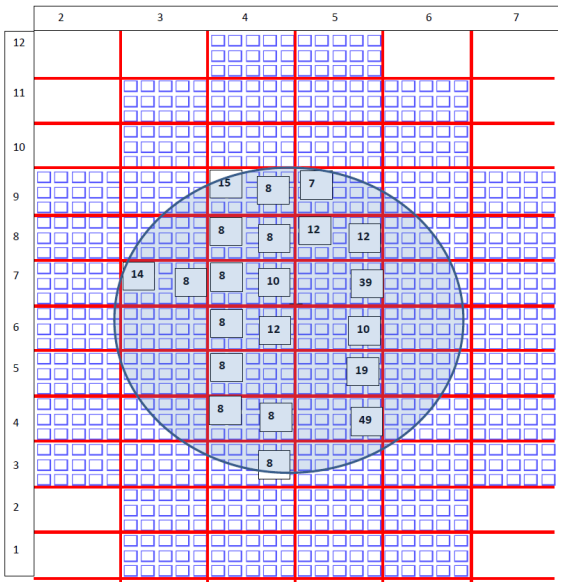

Fig 12. Distribution of measured pirani pressure yield from a 6" wafer. The reticle is defined by the red boxes, and each die is defined by the blue box. The circle represents the usable hermetic sealed lidded die. The boxes with numbers represent the approximate location and level of vacuum of the die. Note that only 2 die per reticle contain pirani gauges.

One experiment performed was to measure 22 MHz resonators, located on the same die as a pirani gauge, and compare the resonator loss over a finite frequency range before and after bonding and lid wafer back etch. The devices are designed to resonate in the 1st length extensional mode around 22 MHz with loss approximating -12 dB on resonance [14]. At approximately 50 kHz higher in frequency a second resonance occurs in which the resonator peaks to -55 dB of loss. This second resonance is referred to as the anti-resonance peak and is useful for understanding unloaded resonator performance; the very large impedance loss of the resonator is typically much greater at this anti-resonant frequency than the insertion impedances which are loaded by the 50 ohm terminations. A frequency sweep of 250 kHz is performed using a Hewlett Packard 4396B Network Analyzer with an Agilent 87512A Transmission/Reflection Test Set. A typical resonator transmission response for a device in a hermetic cavity can been seen in the figure below, figure 13:

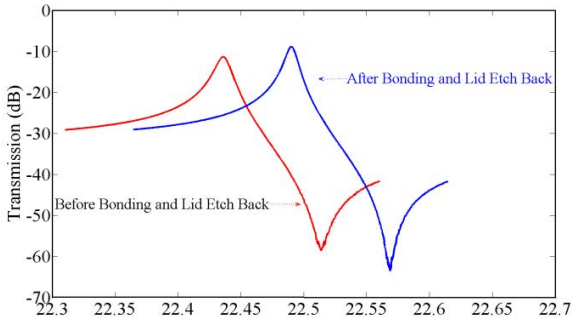

Fig 13. Measured transmission characteristics of a 22MHz resonator measured before (red, atmosphere) and

after bonding and lid wafer etch back (blue). Curves were adjusted to account for tool calibration.

Several distinctive features emerge by comparison of the two measurements. First is that the insertion loss is reduced by 2.5 dB, figure 14, and second is that the resonator Q factor improves, figure 15. This trend is consistent with previously published work where a vacuum environment improves both features of lower frequency micro resonators. In all instances of this experiment, when the Pirani gauge indicates vacuum better than 100 Torr the resonator Q shifts up by at least 1000. In all instances when the pirani gauge indicates vacuum better than 10 Torr, the resonator Q shifts up by at least 3000. Correlated with the shift of resonator Q is the decrease in insertion loss. In the specific case of sample 11, although the pirani gauge indicated atmosphere, the shift of Q and reduction of insertion loss suggests that the pirani gauge failed and the cavity was in a hermetic environment.

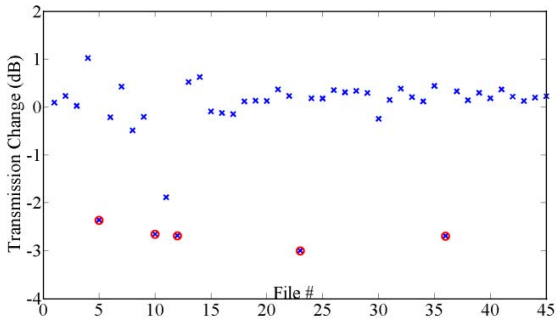

Fig 14. Measured transmission change of 22MHz resonators measured before and after bonding and lid wafer etch back. Data points with red circles indicate Pirani gauge vacuum better than 100 Torr. Curves were adjusted to account for tool calibration

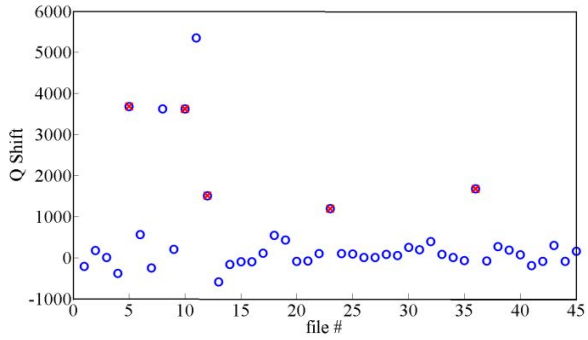

Fig 15. Measured Q change of 22MHz resonators measured before and after bonding and lid wafer etch back. Data points with red circles indicate Pirani gauge vacuum better than 100 Torr.

Another feature which stands out is the frequency increase in the resonant and anti-resonant peaks. However, this feature was noted to occur for both hermetic encapsulated resonators and those whose 22 MHz resonator and pirani gauge indicated atmosphere. The majority of the devices had the anti-resonant frequency up-shift between 50 and 75 kHz, figure 16. We suggest that the cause of this frequency shift is due to the elevated temperatures encountered during wafer bonding. During the bonding, the resonators are heated to 400 C for 25 minutes under vacuum. It is likely that layers deposited during fabrication of the die wafer, such as TiN, could be annealing and thin film stress could be shifting. Although further research should be performed to understand this effect, it could prove to be a useful feature for tuning resonant frequencies of AlN micro resonators.

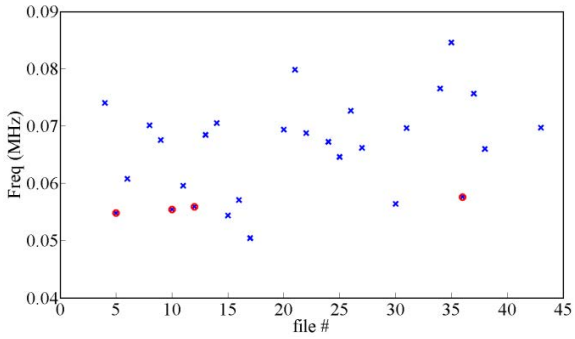

Fig 16. Measured resonant frequency change of 22MHz resonators measured before and after bonding and lid wafer etch back. Data points with red circles indicate Pirani gauge vacuum better than 100 Torr.

Conclusions

Wafer level packaging of AlN micro resonators into a hermetic environment has demonstrated significant advantages. Here we have shown that hermetic packaging with vacuums better than 100 Torr can increase quality factor and reduce insertion losses. From a fabrication standpoint, WLP also provides the opportunity to release resonators and perform die singulation on a wafer scale, rather than on a die by die basis, without having problems of contamination or damage to the devices. Integration of this process can prove difficult with technical problems arising during the bonding and cap thinning process.

Specifically, we have encountered and solved problems with bonding eutectic chemistry and micro voids. These micro voids can reduce the integrity of the hermetic environment but are easily eliminated using diffusion barriers such as silicon dioxide or a nitride. We have also improved the integration process by using plasma back etch to thin the lid wafer to reveal die instead of CMP. This technique has significantly improved yield and cleanliness of the resulting product die. By measuring properties of resonators before and after bonding, we have measured the effects of a vacuum environment and thermal anneal upon AlN micro resonators.

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