

# Evaluation of 15 kV SiC N-IGBT and P-IGBT for Complementary Inverter Topology with Zero $dv/dt$ Stress on Gate Drivers

Arun Kadavelugu and Subhashish  
Bhattacharya  
FREEDM Systems Center  
North Carolina State University  
Raleigh, NC, USA.

Sei-Hyung Ryu, David Grider  
and Anant Agarwal\*  
Cree, Inc.  
Durham, NC, USA.  
\*Currently with the U.S., Dept. of  
Energy.

Scott Leslie  
Powerex, Inc  
Youngwood, PA, USA.

**Abstract**—The complementary inverter topology with N-channel and P-channel switching devices is a known method of eliminating  $dv/dt$  stress on the gate drivers. In the Silicon (Si) based applications, this advantage did not gain wide attention due to inherent inefficiency of the P-type devices, and the matured technology to handle the  $dv/dt$  stress levels produced by these devices with highest blocking voltage rating of 6.5 kV. On the other hand, the ultrahigh voltage ( $> 12$  kV) SiC devices generate high  $dv/dt$  due to their high speed switching. This requires meticulous design of the gate drivers for reliable operation of high power converters. As an easy alternative, the option of using a complementary inverter has been explored in this paper. Both N-channel and P-channel IGBTs with blocking capability of 15 kV have been investigated for the complementary structure. The N-IGBT is found to be more efficient than the P-IGBT, based on the experimental switching characterization results at 6 kV and 5 A. The results of the 3 kV half-bridge complementary inverter prototype are also presented. The option of trade-off of P-IGBT field-stop buffer layer parameters (thickness, doping concentration and lifetime) for better switching characteristics can provide the use of complementary topologies a promising alternative for high power conversion.

## I. INTRODUCTION

The growing interest in the efficient power conversion for the smart-grid and medium voltage motor drives applications has generated significant interest to develop ultrahigh voltage devices using SiC [1], [2]. Currently, Cree has successfully built 10 kV SiC MOSFETs [2] and 15 kV SiC IGBTs. The IGBT can be further scaled up in voltage without significantly increasing the power loss due to its bipolar physics.

The earlier IGBTs were developed with P-type drift due to practical limitation in preparing low resistivity P+ SiC substrates required for the N-IGBTs [3]. However, with advances in the SiC technology, N-IGBTs have also been

built [4], [5] and are found to be more efficient. However, the availability of complementary devices at such high voltage creates a unique option for simple and reliable high power converter design.

The use of complementary switching devices for power conversion has been explored with low voltage (up to 600 V) Si devices. The higher power loss of the P-channel devices has substantially narrowed their application. Also, the maturity of the Si IGBT technology at lower voltage (up to 6.5 kV) to design highly reliable gate drivers has not favored their use in complementary topologies. On the other hand, the SiC IGBTs have created a new paradigm with ultrahigh voltage blocking and  $dv/dt$  stress handling requirements.

At this point, the option of exploring the application of P-IGBT, despite the fact that it is not as efficient as N-IGBT, is worth consideration with the motivation to achieve zero  $dv/dt$  stress on the gate drivers. The following sections of the paper present characteristics of 15 kV P-IGBT and N-IGBT followed by experimental results on a 3 kV complementary half-bridge inverter prototype. Fig. 1 shows the co-pack module of the 15 kV, 5 A IGBTs packaged by Powerex that are evaluated in the paper.

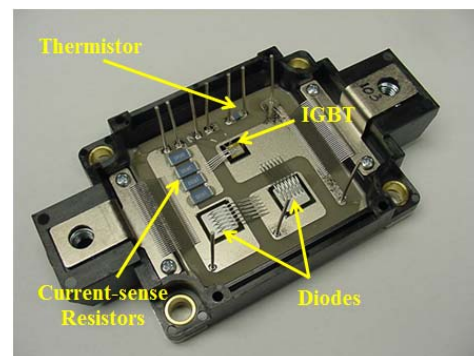


Figure 1: The packaging information of the 15 kV(N-type) IGBT co-pack module.

## II. COMPLEMENTARY INVERTER TOPOLOGY

Fig. 2 shows phase-leg of an inverter using N-channel switching devices on both high-side and low-side. The emitter of the low-side device (E2) is connected to the negative rail (fixed potential) permanently, and therefore zero  $dv/dt$  is seen between the converter control ground and the emitter of the bottom switch. It is shown in the figure that the mid-point (E1) voltage is floating with quick transitions from full dc-bus voltage to zero and vice-versa, in response to the PWM pulses for power conversion. This is a concern as even a small coupling capacitance between the gate driver input side (converter control ground) and the output side (E1) will induce significant common mode currents into the control logic circuit [6]. This can be catastrophic and may lead to failure of the power converter. Hence, care should be taken to design the gate drivers with ultralow coupling capacitance, to make the converter operation highly reliable.

These limitations can be overcome by the complementary inverter topology with P-IGBT on high-side and N-IGBT on low-side as shown in Fig. 3. As shown in the figure, the emitters of both the devices, E1 and E2 are connected to the steady potential terminals of  $+V_{dc}$  and zero respectively, completely eliminating the possibility of  $dv/dt$  coupling currents through the gate drivers. However, as mentioned above the use of P-channel device increases the power loss. The following sections evaluate this phenomenon based on the switching losses and  $dv/dt$  generated by both the devices, with advantages and disadvantages of application of the complimentary topology for high power conversion.

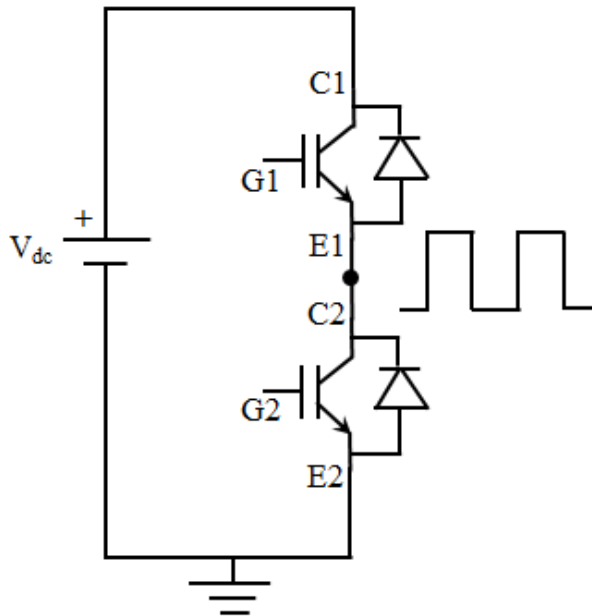


Figure 2: Schematic of an inverter phase-leg with N-type devices.

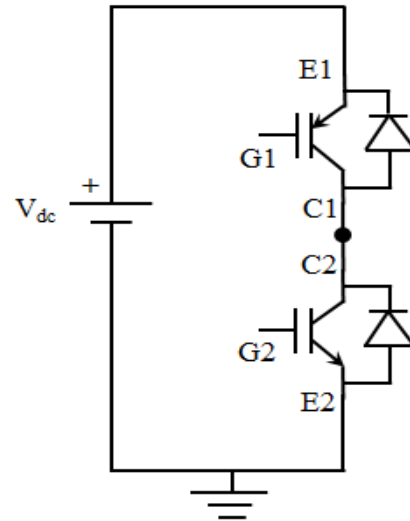


Figure 3: Schematic of phase-leg of a complementary inverter with P-type device (on top) and N-type device (on bottom).

## III. CHARACTERISTICS OF THE P-IGBT

Fig. 4 shows cross-sectional view of the 15 kV P-IGBT. The forward characteristics of the IGBT are shown in Fig. 5. The forward drop of the IGBT is 5.5 V for a current of 5 A at room temperature. Fig. 6 shows turn-off waveforms of the IGBT under clamped inductive load test at 6 kV and 5 A. The transition duration is 2.2  $\mu s$  with energy loss of 21 mJ. The corresponding turn-on transition is shown in Fig. 7. Unlike the turn-off transition, the turn-on transition has a spike of 66 A with a very short transition time of about 500 ns. The high current spike is due to discharge of the capacitance of the diode across the load inductor due to high  $dv/dt$  generated by the IGBT. It is to be noted that the polarities of the current and voltage have been reversed for convenience and for ease of comparison with the N-IGBT.

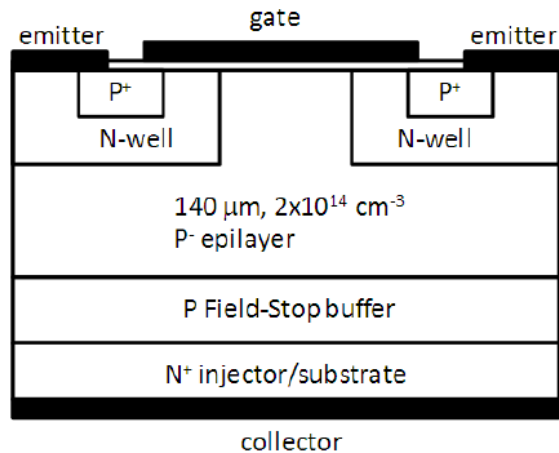


Figure 4: Cross-sectional view of the 15 kV P-IGBT

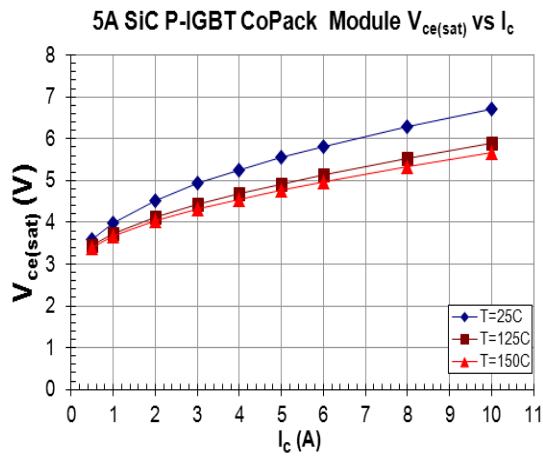


Figure 5: Forward characteristics of the 15 kV, 5 A, P-IGBT at different temperatures. ( $V_{GE} = -20$  V)

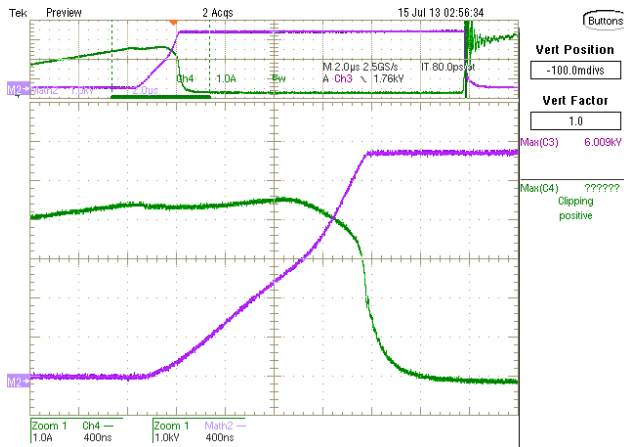


Figure 6: Turn-off transition of the 15 kV, 5 A, P-IGBT under clamped inductive load test at 6 kV and 5 A with  $R_{G(OFF)} = 10 \Omega$ . [Ch4(Green):  $I_C - 1$  A/div; Math2(Violet):  $V_{CE} - 1$  kV/div; Time scale: 400 ns/div].

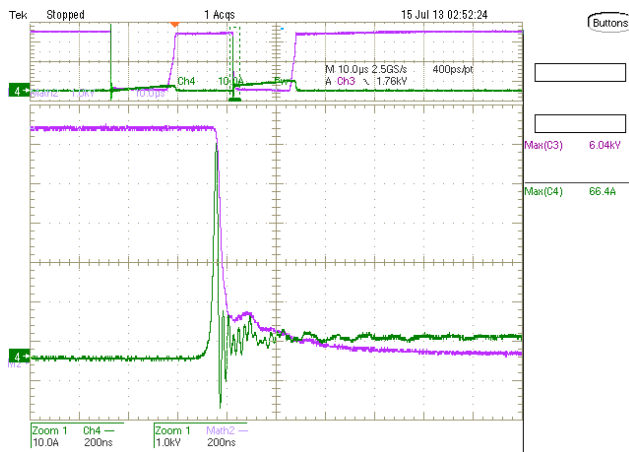


Figure 7: Turn-on transition of the 15 kV, 5 A, P-IGBT under clamped inductive load test at 6 kV and 5 A with  $R_{G(ON)} = 200 \Omega$ . [Ch4(Green):  $I_C - 10$  A/div; Math2(Violet):  $V_{CE} - 1$  kV/div; Time scale: 200 ns/div].

The turn-off gate resistance,  $R_{G(OFF)}$ , used in the evaluation is  $10 \Omega$ , whereas the turn-on gate resistance,  $R_{G(ON)}$ , is  $200 \Omega$ . The gate voltage,  $V_{GE}$ , used is  $-20$  V for turn-on, and  $+4.5$  V for turn-off. The high  $R_{G(ON)}$  is used to suppress the current spike at the beginning of the transition by limiting the rate of discharge of the depletion capacitance of the IGBT. As the injection of the  $N^+$  emitter is very efficient, the current spike is not suppressed further. The high injection efficiency is also responsible for the long turn-off duration. However, further increase of  $R_{G(ON)}$  will reduce the spike and decrease the rate of voltage transition at the cost of increased power loss.

#### IV. CHARACTERISTICS OF THE N-IGBT

The cross-sectional view of the N-IGBT is shown in Fig. 8. The N-IGBT has same drift layer thickness and doping as P-IGBT, but the thickness, doping and life time of the field-stop buffer layer are significantly different. The 15 kV, 5 A, N-IGBT has an on-drop of 4.9 V for a current of 5 A, at room temperature, as seen in Fig. 9. Unlike the P-IGBTs, the  $+ve$  temperature co-efficient of the N-IGBTs make them inherently suitable for parallel operation.

The switching characteristics of both the IGBTs have been evaluated on a clamped inductive double pulse test setup with a discrete 20 kV SiC diode (two 10 kV didoes in series) for free-wheeling. The turn-off and turn-on characteristics of the N-IGBT are shown in Figs. 10 and 11 respectively. The gate resistances used are same as those used for the P-IGBT tests. It can be seen that the turn-off duration is much shorter for the N-IGBT. This is due to lower injection of the  $P^+$  emitter of the N-IGBT as compared to the higher injection of the  $N^+$  emitter of the P-IGBT. Thus, the N-IGBT has lower stored charge that consequently needs lesser time for complete recombination for turn-off. The lower injection is also the reason for much lower current spike or the  $dv/dt$  at the beginning of the turn-on transition.

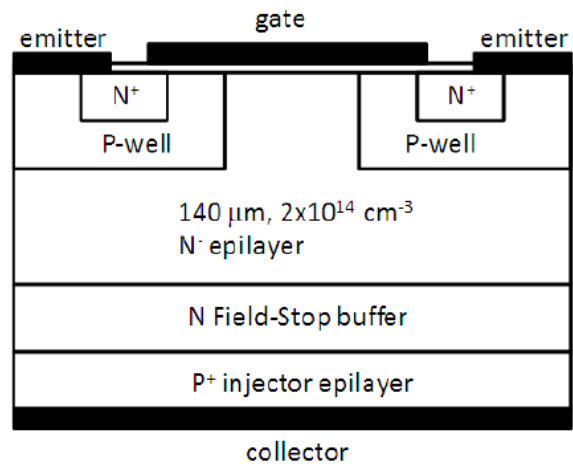


Figure 8: Cross-sectional view of the 15 kV N-IGBT

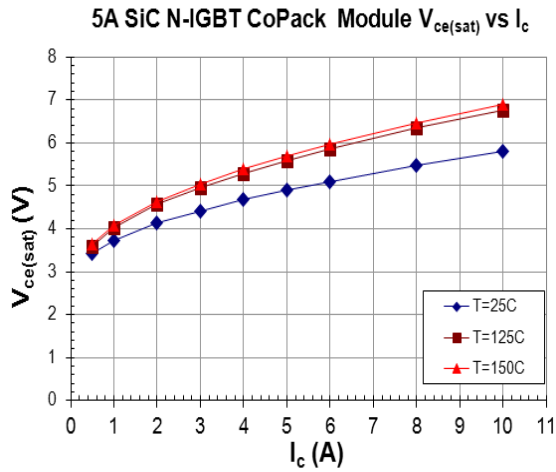


Figure 9: Forward characteristics of the 15 kV, 5 A, N-IGBT at different temperatures. ( $V_{GE} = +20$  V)

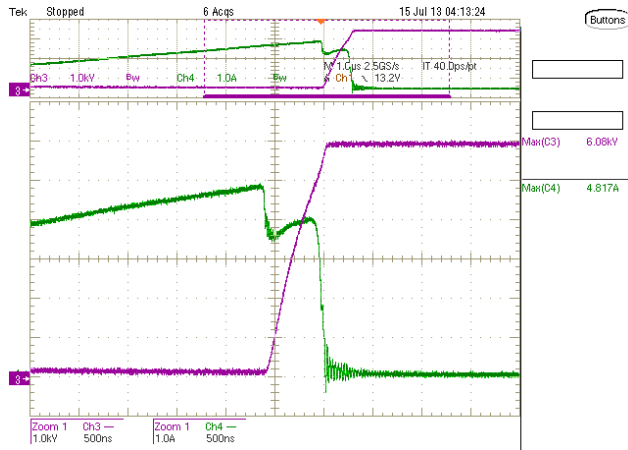


Figure 10: Turn-off transition of the 15 kV, 5 A, N-IGBT under clamped inductive load test at 6 kV and 5 A with  $R_{G(OFF)} = 10 \Omega$ . [Ch3(Magenta):  $V_{CE} = 1$  kV/div; Ch4(Green):  $I_C = 1$  A/div; Time scale: 500 ns/div].

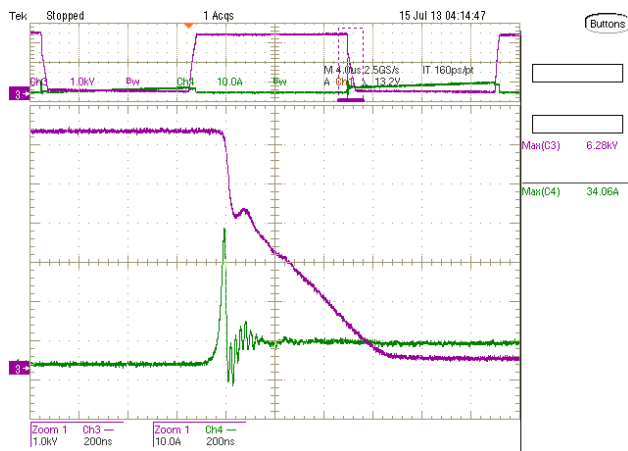


Figure 11: Turn-on transition of the 15 kV, 5 A, N-IGBT under clamped inductive load test at 6 kV and 5 A with  $R_{G(ON)} = 200 \Omega$ . [Ch3(Magenta):  $V_{CE} = 1$  kV/div; Ch4(Green):  $I_C = 10$  A/div; Time scale: 200 ns/div].

## V. COMPARISON OF THE P-IGBT AND N-IGBT

A summary of comparison of the characteristics of the P-IGBT and N-IGBT is shown in Table I. The higher conduction drop of the P-IGBT is due to higher threshold voltage and lower MOS channel mobility in comparison to the N-IGBT. The turn-off loss of the P-IGBT at 6 kV, 5 A is 21 mJ, whereas, it is 6.7 mJ for the N-IGBT. As explained earlier, the higher injection efficiency of the N+ emitter in the P-IGBT is resulting in more storage charge to be removed during the turn-off process. This is consequently leading to longer turn-off duration and more energy loss in the P-IGBT.

On the other hand, the turn-on loss of the N-IGBT is higher. It can be seen from Fig. 11 that the voltage of the N-IGBT has a sudden change in slope during the turn-on transition. The sharper region is due to discharge of its low depletion capacitance, whereas, the slower region is dictated by the high diffusion capacitance and the high  $R_{G(ON)}$  of 200  $\Omega$ , used to slow down the rate of discharge of the depletion capacitance at the beginning of the transition. From Fig. 7, it can be seen that the P-IGBT has a steep slope in voltage till it reaches about 1 kV. Thus, the turn-on  $dv/dt$  of the P-IGBT is much higher (about twice) than that of the N-IGBT. The higher  $dv/dt$  of the P-IGBT is also responsible for higher current spike due to discharge of the capacitance across the diode (this includes the inter-winding capacitance of the inductive load used for the double pulse switching tests).

So, based on the conduction, turn-off and turn-on losses information shown in Table I, it can be concluded that the N-IGBT is more efficient. Also, it is to be noted that the turn-on loss of the N-IGBT can be reduced by using a lower gate resistance that produces the same  $dv/dt$  (or current spike) seen with the P-IGBT, for a fair comparison from the perspective of a power converter.

TABLE I: Comparison of the P-IGBT and N-IGBT

Parameter	P- IGBT	N- IGBT
<b>Forward drop at 5 A</b>	5.5 V	4.9 V
<b>Turn-off loss at 6 kV, 5 A</b>	21 mJ	6.7 mJ
<b>Turn-on loss at 6 kV, 5 A</b>	6.3 mJ	12.7 mJ
<b>Turn-off <math>dv/dt</math> (in the steeper region)</b>	6 kV/ $\mu$ s	11 kV/ $\mu$ s
<b>Turn-on <math>dv/dt</math> (in the steeper region)</b>	119 kV/ $\mu$ s	62 kV/ $\mu$ s
<b>Turn-off duration</b>	2.2 $\mu$ s	650 ns
<b>Turn-on duration</b>	500 ns	700 ns
<b>Turn-on current spike magnitude</b>	66 A	34 A
<b><math>R_{G(ON)}/R_{G(OFF)}</math></b>	200 $\Omega$ / 10 $\Omega$	200 $\Omega$ / 10 $\Omega$

## VI. DISCUSSION

From the results shown in the section V, the N-IGBT is more efficient in comparison to the P-IGBT. However, the  $dv/dt$  produced by both of these devices is extremely high. This makes it challenging to design a reliable power converter owing to the ultrahigh voltage levels of these fast switching devices. As shown in Fig. 2, the high-side gate driver of the N-IGBT will be exposed to the high  $dv/dt$  that results in injection of common mode current into the control supply. This could lead to failure of the gate driver logic or disruption of the other control signals of the power conversion system.

An obvious method, as mentioned above that can overcome this problem is a two-level complementary half-bridge (Fig. 3) based topologies, where the emitters of both the devices are connected to fixed potential terminals. The absence of  $dv/dt$  (or the common mode currents) makes it easy and cheaper to design the high voltage gate drivers with extremely high reliability. In [5], it is explained that a trade-off of forward-drop and switching loss (and  $dv/dt$ ) is possible by adjusting the thickness, doping concentration and lifetime parameters of the field-stop buffer layer of the IGBTs. This opens the possibility of reducing the switching loss of the P-IGBTs to about the same level as the N-IGBTs, with a moderate increase in conduction loss and thus making them ideal to use as a complementary pair for high switching frequency applications.

The existing P-IGBTs are also promising to use as complementary pairs in soft-switching circuits like Dual Active Bridge (DAB) converters. The DAB has negligible switching loss and low  $dv/dt$  due to zero voltage switching (ZVS) transitions, except at light loads [7]. Therefore, using complementary pair in the DAB converter is an ideal option to tackle high  $dv/dt$  at light loads, without increasing the power loss at higher loads. The P-IGBTs are also promising for high step-down dc-dc (buck) converters due to simplicity in the gate driver design, whereas the N-IGBTs are suitable for high step-up (boost) dc-dc converters. In the cases where the heat sinks of the power converters are grounded, a detailed evaluation of the influence of high  $dv/dt$  produced by these fast switching IGBTs on the power circuit common mode currents needs to be performed.

## VII. EXPERIMENTAL RESULTS ON A 3 kV PROTOTYPE

The complementary half-bridge inverter (schematic shown in Fig. 12) prototype built using the 15 kV, 5 A, SiC, P-IGBT and N-IGBT is shown in Fig. 13. In Fig. 14, the high voltage gate driver used in the inverter is shown. The results of the inverter with 3 kV dc input at 5 kHz and 10 kHz switching frequencies are shown in Figs. 15 and 16 respectively. The IGBTs are exposed to a peak stress of 3 kV. At 5 kHz switching, the ac output voltage and current of

the converter are 819 V rms and 2.1 A rms respectively. The corresponding values at 10 kHz are 731 Vrms and 1.9 A.

The reduction of switching ripple with 10 kHz switching is evident from the figures. Also, the magnitude of the output voltage is reduced with 10 kHz switching, due to increased voltage drop across the filter inductance. The noticeable distortion in ac current (or voltage) at 10 kHz is due to amplified effect of the same dead-band. The modulation index of the converter is 0.8, and the resistive load and filter inductor values are 380  $\Omega$  and 75 mH respectively.

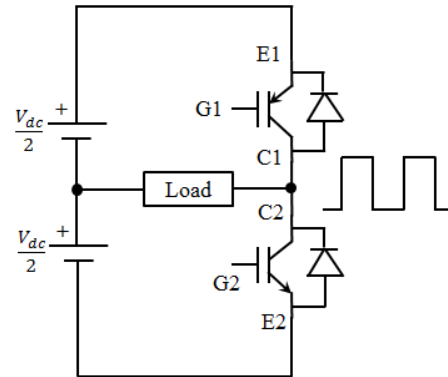


Figure 12: Schematic of the half-bridge complementary inverter.

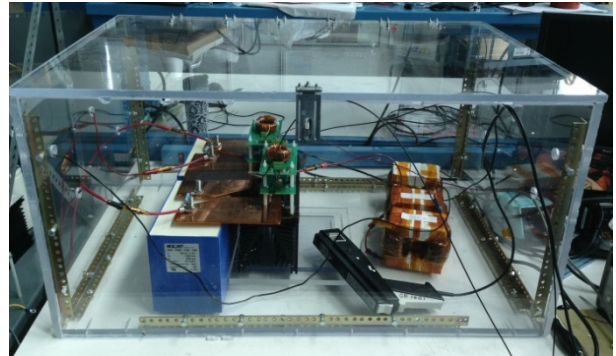


Figure 13: The prototype of the complimentary half-bridge inverter built using the 15 kV P-IGBT and N-IGBT.

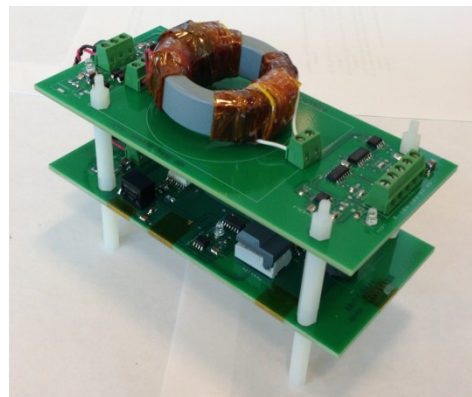


Figure 14: The high voltage gate driver used in the experimental setup.

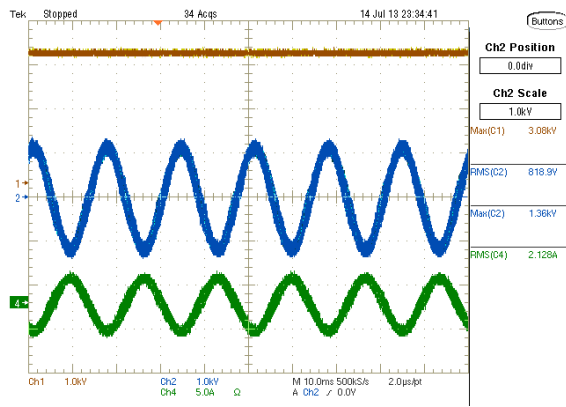


Figure 15: Experimental waveforms of the complimentary inverter with 5 kHz switching frequency. [Ch1(Brown): Input voltage – 1 kV/div; Ch2(Blue): Output voltage – 1 kV/div; Ch4(Green): Output current (polarity reversed) – 5 A/div; Time scale: 10 ms/div].

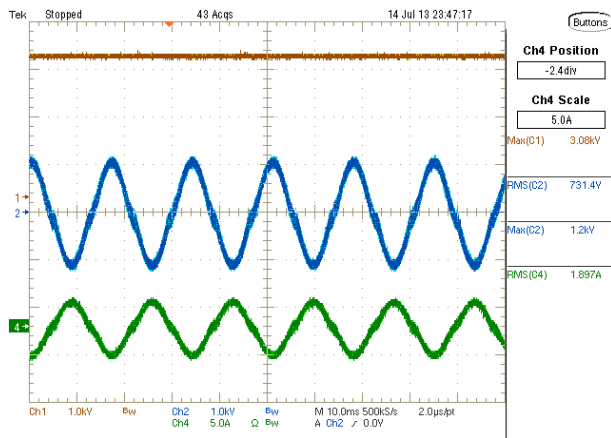


Figure 16: Experimental waveforms of the complimentary inverter with 10 kHz switching frequency. [Ch1(Brown): Input voltage – 1 kV/div; Ch2(Blue): Output voltage – 1 kV/div; Ch4(Green): Output current (polarity reversed) – 5 A/div; Time scale: 10 ms/div].

## VIII. CONCLUSION

The simple two-level complementary voltage source converter topology represents a new paradigm and new possibilities in medium voltage power conversion. Based on the experimental switching results at 6 kV and 5 A, the N-IGBTs are found to be more efficient than the P-IGBT. However, as both these devices generate high  $dv/dt$ , the use of complementary topology has the benefit of improving gate driver reliability by eliminating injection of the common-mode currents. The experimental results on a 3 kV complementary inverter prototype have been presented as a validation of the proposed concept for the high voltage SiC devices. The optimization of the field-stop buffer layer parameters of the IGBTs for better switching performance

presents a promising option of high efficiency, ultrahigh voltage power conversion. The high voltage 15 kV SiC optimized N-IGBT and P-IGBT based simple two-level complementary inverter topology can provide the desired converter reliability required for applications such as, medium voltage drives, medium voltage traction rectifier systems, solid state transformers and medium voltage dc-dc applications.

## ACKNOWLEDGMENT

This work made use of the FREEDM ERC shared facilities supported by the National Science Foundation under Award Number EEC-0812121.

## REFERENCES

- [1] A. K. Agarwal, "An overview of SiC power devices," International Conf. on Power, Control and Embedded Systems (ICPCES), 2010, pp. 1-4.
- [2] M. K. Das, et al., "10 kV, 120 A SiC half H-bridge power MOSFET modules suitable for high frequency, medium voltage applications," Energy Conversion Congress and Exposition (ECCE), 2011, pp. 2689-2692.
- [3] Q. Zhang, C. Jonas, S. Ryu, A. Agarwal and J. Palmour, "Design and Fabrications of High Voltage IGBTs on 4H-SiC," IEEE International Symposium on Power Semiconductor Devices and IC's, ISPSD, 2006, pp. 1-4.
- [4] B. J. Baliga, "Advanced high voltage power device concepts," New York: Springer-Verlag, 2012, pp. 293-294.
- [5] S. Ryu, et al., "High performance, ultra high voltage 4H-SiC IGBTs," IEEE Energy Conversion Congress and Exposition (ECCE), 2012, pp. 3603-3608.
- [6] S. Zeltner, "Insulating IGBT driver with PCB integrated capacitive coupling elements," 6th International Conference on Integrated Power Electronics Systems, CIPS, 2010, pp. 1-6.
- [7] A. K. Jain and R. Ayyanar, "PWM conitrik of dual active bridge: Comprehensive analysis and experimental verification," IEEE Trans. Power Electron., vol. 26, issue. 4, 2011, pp. 1215-1227.