SERIAL BACK-PLANE TECHNOLOGIES IN ADVANCED AVIONICS ARCHITECTURES

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Abstract

Current back plane technologies such as VME, and current personal computer back planes such as PCI, are shared bus systems that can exhibit non-deterministic latencies. This means a card can take control of the bus and use resources indefinitely affecting the ability of other cards in the back plane to acquire the bus. This provides a real hit on the reliability of the system. Additionally, these parallel busses only have bandwidths in the 100s of megahertz range and EMI and noise effects get worse the higher the bandwidth goes. To provide scalable, fault-tolerant, advanced computing systems, more applicable to today's connected computing environment and to better meet the needs of future requirements for advanced space instruments and vehicles, serial back-plane technologies should be implemented in advanced avionics architectures. Serial backplane technologies eliminate the problem of one card getting the bus and never relinquishing it, or one minor problem on the backplane bringing the whole system down. Being serial instead of parallel improves the reliability by reducing many of the signal integrity issues associated with parallel back planes and thus significantly improves reliability. The increased speeds associated with a serial backplane are an added bonus.

Introduction

Current back plane technologies such as VME, and current personal computer backplanes such as PCI, are shared bus systems that can exhibit non-deterministic latencies. This means a card can take control of the bus and use resources indefinitely affecting the ability of other cards in the back plane to acquire the bus. This provides a real hit on the reliability of the system. Additionally, these parallel busses only have bandwidths in the 100s of megahertz range and EMI and noise effects get worse the higher in bandwidth you get. To provide scalable, fault-tolerant, advanced computing systems, more applicable to today's connected computing environment and to better meet the needs of future requirements for advanced space instruments and vehicles serial back-plane technologies should be implemented in advanced avionics architectures. Serial backplane technologies eliminate the problem of one card getting the bus and never relinquishing it, or one minor problem on the backplane bringing the whole system down. Being serial instead of parallel improves the reliability by reducing many of the signal integrity issues associated with parallel backplanes and thus significantly improves reliability. The increased speeds associated with a serial backplane are an added bonus.

Background

The current backplane technologies of VME (Figure1) and PCI have inherent limitations due to their numerous signals and parallel nature.

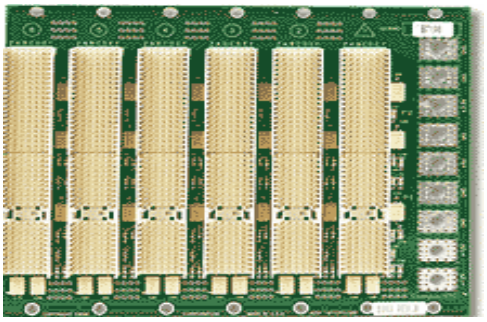

Figure 1. Typical VME Parallel Backplane

Some of these limitations are:

- Multiple card slots ***share*** a common bus;
- Each signal, on each card, is bussed together;
- As performance goes up the slot count per bus goes down;
- Limited performance -- Available bandwidth is shared among all cards;
- Architecture scales poorly -- Too many pins, too many traces, too many bridges;
- Significantly slower than upcoming serial backplane technologies;

- Requires a very large number of connectors and pins (100s);
- Limited scalability (the ability to add more boards into the back plane). Signal integrity and speed decrease with every board added;
- **Single point failure on back plane could bring entire system down;**
- The higher the speed of the back-plane the less number of board slots that can be supported;
- Standard backplanes are multi-drop, parallel bus implementations that are close to practical limits of performance;
- Only two cards can talk at any one time on the backplane, shutting out all other card communications till those two are done;
- Parallel busses use synchronously clocked data transfers that are Signal skew limited and the signal routing rules are at the limit for cost-effective technology;
- Approaches to pushing these limits to create a higher bandwidth, general-purpose I/O bus result in large cost increases for little performance gain;

Approach

Industry is converting to serial –backplanes to alleviate many of the problems associated with the parallel backplanes and significantly increase data bandwidths. Serial back planes have numerous advantages such as:

- Very high bandwidth with the fewest number of signals;
- Serial connections don't run into delay skew, in which parallel bits arrive at different times and have to be synchronized (Figure 2). Skew is the timing and phase anomalies in a transmission signal that occur when trace lengths are not matched;

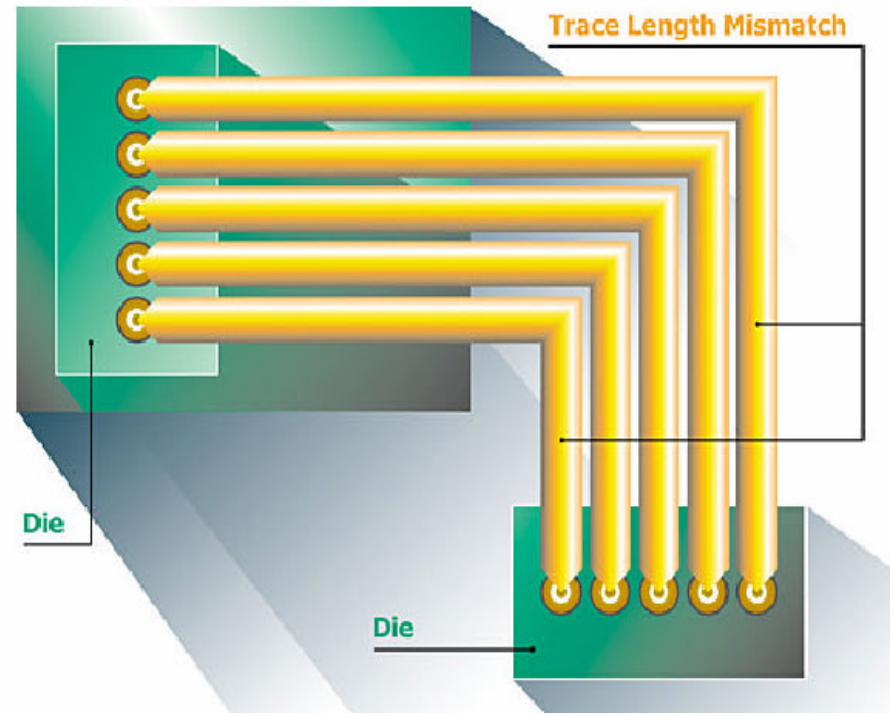

Figure 2. Example of Skew

- Serial Back-Plane technology uses a low voltage differential signaling (LVDS) transmission method for sending information. LVDS is a low noise, low power, low amplitude method for high-

speed data transmission over copper wire;

- The differential nature of this technology increases noise immunity and noise margins and allows protection to traditional single-ended noise sources including AC return paths and cross-talk aggressors. As a result, serial links do not suffer as much from crosstalk, EMI, or capacitive problems as parallel links (Figure 3);
- Cheaper to implement;
- Could implement a 'back plane' of distributed nodes outside of a normal chassis backplane;

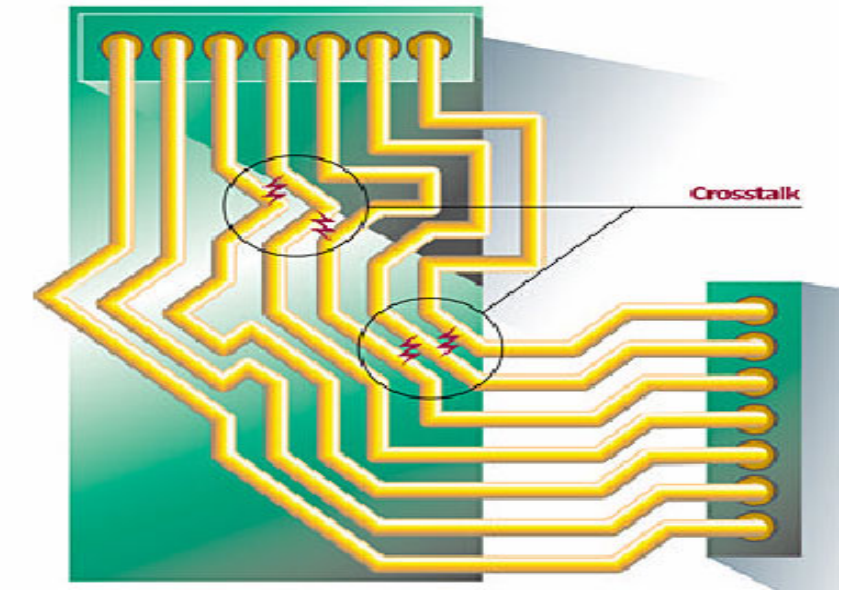

Figure 3. Cross Talk and EMI Effects of Parallel Signals in Standard Backplanes

To implement these serial backplanes, industry has come up with a variety of backplane configurations. Some use a switch fabric (Figure 4). In a switch fabric configuration, all nodes connect to one or more switch cards where the data is then routed between the source and destination nodes. Other configurations are also possible, such as completely connected point to point configurations. These configurations support simultaneous traffic between different node card pairs increasing available bandwidth.

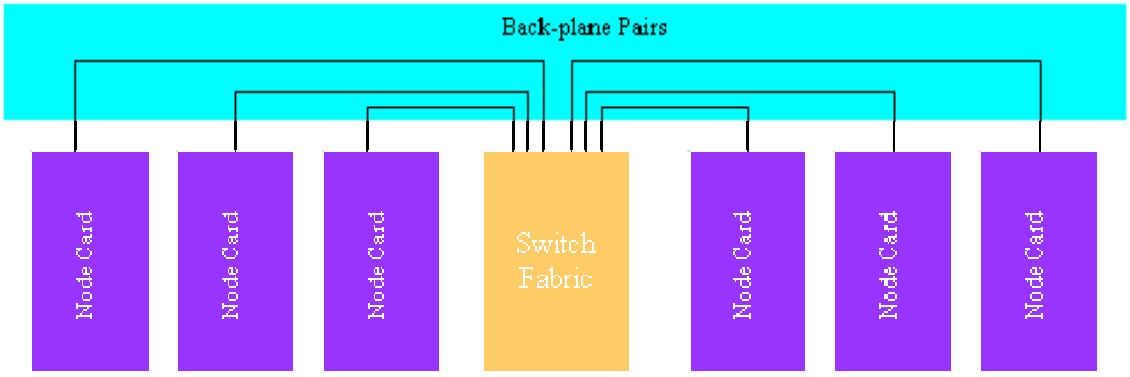

Figure 4. Block Diagram of Switch Fabric Backplane

Some of the benefits of using a switched fabric architecture are:

- With a shared bus, only one device can communicate at a time. Whereas with switched fabric, many devices can be communicating simultaneously;
- Redundancy can be built in to the switched fabric interconnections;
- the point-to-point nature of switched fabrics can enhance reliability by isolating faults to single end points in contrast to buses in which a faulty end point can bring down the entire bus;
- Point-to-point connections are inherently friendly to device insertion and removal;

Design Description

Due to the complexity and cost of industry standards such as PCI express and RapidIO, this project used the generic serial backplane protocol IP (intellectual property) provided by Xilinx for free. It takes advantage of the Rocket IO multi-gigabit transceivers embedded in the Xilinx Virtex II field programmable gate arrays (FPGA) (Figure 5). These transceivers provide a generic physical layer interface that is common to most of the industry standard protocols. Using the Aurora protocol along with the RocketIO multi-gigabit transceivers, provides a good platform for studying the benefits of serial backplanes and provides an easy path to build the industry standard protocols on top of the aurora and rocket IO transceivers.

Regardless of the particular industry protocol, all serial backplanes have similar features at the physical layer interface. These are typically, LVDS interface, the use of 8B/10B encoding, and CRC for reliability.

Utilizing the Xilinx Aurora protocol, which takes advantage of the Rocket IO transceivers on the Xilinx chips, all of the features in the block diagram of the Rocket IO transceiver (Figure 5) are taken care of.

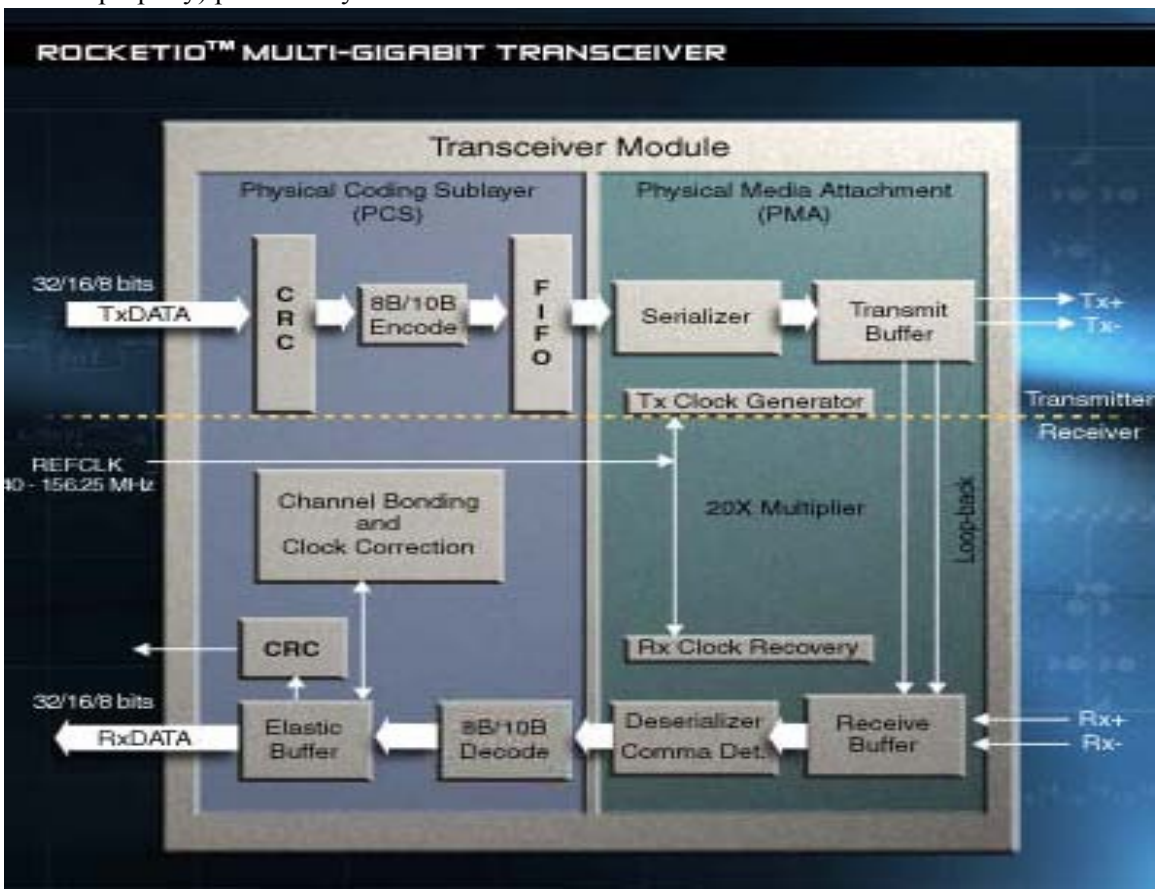

Figure 5. Block Diagram of the Physical Layer Protocol Features of the Serial Transceivers

The benefits of LVDS are many:

- The differential data transmission method used in LVDS is less susceptible to common-mode noise than single-ended schemes (Figure 6);
- Differential transmission uses two wires with opposite current/voltage swings;
- The advantage of the differential approach is that if noise is coupled onto the two wires as common-mode (the noise appears on both lines equally) and is thus rejected by the receivers, which looks at only the difference between the two signals;
- The differential signals also tend to radiate less noise than single-ended signals due to the canceling of magnetic fields;
- The current-mode driver is not prone to ringing and switching spikes, further reducing noise;
- Because differential technologies such as LVDS reduce concerns about noise, they can use lower signal voltage swings. This advantage is crucial, because it is impossible to raise data rates and lower power consumption without using low voltage swings. The low swing nature of the driver means data can be switched very quickly;

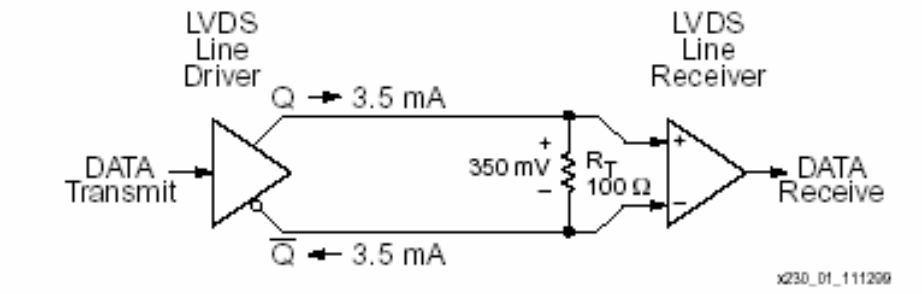

Figure 6. Low-Voltage Differential Signaling (LVDS)

8B/10B Encoding

One of the main features of serial backplane protocols is that the clock is embedded in the data stream. To accomplish this successfully, the phase locked loops (PLL) require a certain number of transitions per unit time. 8B/10B encoding is a method of achieving this minimum transition requirement. The 8B/10B encoding serves two purposes: 1) it makes sure there are enough transitions in the serial data stream so the clock can be recovered easily from the embedded data. 2) Since it transmits the same number of ones as zeros, it maintains a d-c balance. This is important for transporting data between several chassis that may have different ground potentials or different power supplies.

Cyclic Redundancy Check (CRC)

Cyclic Redundancy Check (CRC) is a procedure to detect errors in the received data. Using this technique, the transmitter appends an extra n- bit sequence to every frame called a Frame Check Sequence (FCS). The FCS holds redundant information about the frame that helps the transmitter detect errors in the frame. The CRC is one of the most used techniques for error detection in data communications. The technique has three advantages:

- Extreme error detection capabilities;
- Little overhead;
- Ease of implementation;

System Design

The design took several steps. The first step was to acquire the Aurora protocol intellectual property (IP) from Xilinx. This basically takes the form of VHDL code that can be put into an integrated design environment and combine it with custom logic to control it. This took some time and effort due to the IP being new and so many documents to go through to implement this properly. Once the complete design for the Xilinx

chips were done, the rest of the custom board was designed. This consisted of a digital signal processor from Texas Instruments from the C6000 family and plenty of memory. All the other circuits necessary to clock the Xilinx chips, and power the individual components were designed and a board level schematic was ready for layout.

The custom board was designed to be a flexible, reconfigurable board that would provide a significant amount of functionality and also provide a good test platform for implementing and controlling various serial backplane standards. The one implemented in the Xilinx chips for this round of testing was the Aurora protocol from Xilinx with the logic to control this protocol designed in house by EI31. The custom card allows the flexibility of programming standards other than the Aurora protocol in the reconfigurable Xilinx chips such as PCI express, and Rapid IO.

Additionally the custom board provides the ability to test individual chips on the board for stuck at faults and loose pins by using the Joint Test Action Group's (JTAG) interface and special hardware and software purchased for this project.

Below is a block diagram (Figure 7) of the custom card. This highlights how a serial backplane can be included in a normal computing, or digital signal processing node. The serial backplane logic can be embedded in the Xilinx field programmable gate array (FPGA). As many channels as necessary can be embedded to implement higher bandwidths, or redundancy.

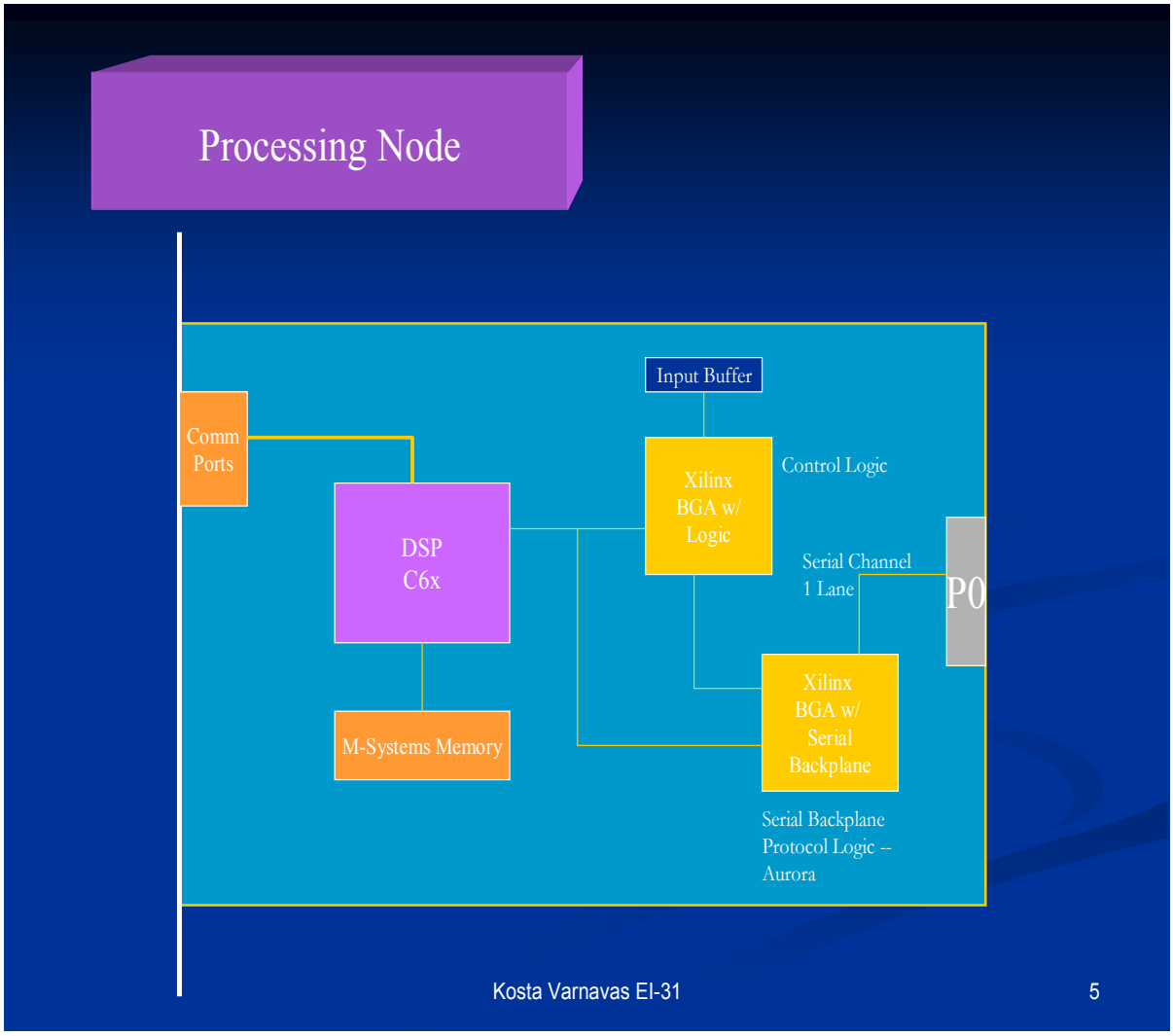

Figure 7. Block Diagram of Custom Card to Implement Serial Backplane Standards

There are many additional features of this custom board that go well beyond the scope of the original research effort:

- Provides latest digital signal processor from Texas Instruments: TMS320C6711;
- Two in-system reprogrammable Xilinx chips and a unique design make this board reconfigurable for multiple applications;
- Xilinx chips have one embedded Power PC405 per chip;
- This allows up to three processors to work on data intensive algorithms without a single board design change;
- 4 multi gigabit transceivers (Rocket IO) that are reconfigurable, can implement numerous serial backplane protocols such as Xilinx's Aurora, RapidIO, PCI Express, Infiniband and others by simply reconfiguring the board. No hardware board change necessary;
- 64 MByte disk on chip device acts like an on board hard disk drive for significant data storage;
- 16 bit buffered data path coming from off board into the reconfigurable Xilinx chips provide an interface to outside data streams such as A/D cards;
- First use of Ball Grid Array (BGA) package style components;
- Multiple voltages on one board. Main power 3.3 volts but Xilinx and DSP use different voltages for internal operations vs. their IO voltages;

The reconfigurable nature of this board and the significant features of the components on the board allow this board to be a good development platform for the research areas of interest as well as numerous other areas of advanced avionics architectures:

- Serial Backplane protocols .Main research focus area;
- Board level testability using JTAG techniques. Main research focus area;
- Multiple reconfigurable methods for running various algorithms on incoming data. Outside research focus area;
- Embedded hardware pipeline in FPGAs to run algorithms. Outside research focus area;
- Multiprocessing of data streams using Xilinx Power PC devices, one in each Xilinx chip, and the digital signal processor. Outside research focus area;
- High density and high reliability data storage using the M-systems disk on chip component. Outside research focus area;

Applications and Observations

The intended applications of this technology is to replace the current parallel backplanes with the higher speed and more reliable, fault tolerant serial backplane version being incorporated by industry. The research has provided a set of custom cards and COTS hardware to implement and characterize various serial backplane protocols for space applications. The research has increased NASA's capabilities in this technology tremendously. The current application is a test platform in the lab for testing, and implementing various protocols. The custom cards are working well in the lab. Data transfer software written to test the serial channels proves the backplane works well in loop back mode on each of the custom cards as well as communicating between the cards. The next step would be to characterize the communications and compare speed and reliability to the current parallel backplanes. However, due to early withdrawal of previously committed research funds, the next steps will have to be taken under a different task.

What This Means to NASA

NASA reliability requirements are very stringent. Even for applications where NASA doesn't need extreme speed, the reliability of systems will go up significantly due to:

- Significantly fewer number of pins
- Improved signal integrity
- Multiple board pairs can talk to each other simultaneously.
- The improved signal integrity will allow more boards to be in a back-plane without suffering signal degradation;

- Current back-plane difficulties due to signal integrity such as clock skew, glitches, cross-talk, and impedance mismatches will practically be eliminated;
- EMI/EMC compatibilities should be greatly improved;
- The back-plane will be significantly simpler resulting in lower cost and weight;
- The fault tolerance of the serial back-plane is important;
- With current back-planes, a problem on just one pin can bring the whole system down;
- With current back-planes, redundant boards have to be in a separate chassis resulting in more cost, weight, and complexity;
- With serial-back-planes, a board could have a catastrophic failure but not bring any of the other boards down;
- With serial-back-planes, redundant boards can reside in the same chassis, reducing complexity, cost and weight;

Summary

Industry is moving to these serial standards and as pointed out in the report, the benefits to NASA are numerous. Serial backplane protocols are complex**.** Even the free intellectual property from Xilinx took time to compile and the documentation and available tech support was minimal.

As with any commercially available product, visibility into the design was very minimal making troubleshooting difficult. However, once technical difficulties were overcome and the design was implemented, the serial channels worked well. The results appear to be repeatable, having gone thru the entire implementation process a number of times on two separate boards.

Future Work

Currently there are two boards in the lab for testing. Figure 8 shows one of them.

Figure 8. Picture of Custom Designed Serial Backplane Test Board

The next steps to developing this technology for NASA use will be:

- Run parallel bus style access cycles across the serial backplane and compare to actual parallel bus access times and other issues;
- Use reconfigurability of the boards to implement various industry standard protocols in the Xilinx FPGAs such as PCI-Express, and RapidIO.