A High IIP3, $50\,\mathrm{GSamples/s}$ Track and Hold Amplifier in $0.25\,\mu\mathrm{m}$ InP HBT Technology

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***Abstract*—A 50 GSamples/s track and hold amplifier (THA) is designed and fabricated in a $0.25\,\mu$m InP HBT technology. High speed switching functionality in the amplifier is achieved using base-collector diodes rather than switched-emitter-followers (SEF). Operating with -5 V and -2.5 V supplies, it achieves IIP3 more than $+16$ dBm up to 22 GHz. An HD3 of -30.3 dB is measured at $+7.5$ dBm input power which is P1dB point of THA at 15 GHz. Time domain measurement verifies the sampling rate of 50 GSamples/s in the THA.**

***Index Terms*—Mixed analog digital integrated circuits, Indium Phosphide, Analog-digital conversion, Sampled data circuits.**

I. Introduction

The usage of digital receivers in optical transceivers and millimeter-wave radios is growing rapidly and consequently requiring high speed analog-to-digital converters (ADCs) [1]. The overall performance of these systems is strongly dependent on the performance of ADCs in terms of bandwidth, sampling rate, resolution and linearity. Therefore, these ADCs needs to be designed carefully. Design of a high speed track and hold amplifier (THA) is one of the challenging bottlenecks in the design of high sampling-rate ADCs.

Recently reported high sampling-rate THAs which are either SiGe-based [1]-[3] or InP-based [4],[5] have been designed using a switched emitter followers. The THA presented in this paper uses a base-collector diode rather than a switched emitter follower stage. Here we present a THA which operates at $50\,\mathrm{GSamples/s}$ and shows an IIP3 greater than $+16\,\mathrm{dBm}$ for RF input signal frequencies up to $22\,\mathrm{GHz}$. This THA has the fastest sampling rate among the reported THAs [4],[5] in the InP HBT technology. We briefly describe InP HBT process used in this work in Section II. Then, the circuit diagram and its operation is explained in Section III. Finally, the measurement results are presented in Section IV.

II. $0.25\,\mu$m Indium Phosphide HBT Process

The THA IC reported in this paper uses the $0.25\,\mu\mathrm{m}$ InP HBT technology with a $\sim 4.5\,\mathrm{V}$ breakdown voltage. A single HBT has a peak bandwidth of $f_{max} = 700\,\mathrm{GHz}$ and $f_T = 400\,\mathrm{GHz}$.

A four-metal interconnect stack is used in the fabrication of the circuit. Compact, stacked interconnect vias provide access from the top layer of metal interconnect for signal ($3\,\mu\mathrm{m}$ thick) to the three lower layers (each $1\,\mu\mathrm{m}$ thick).

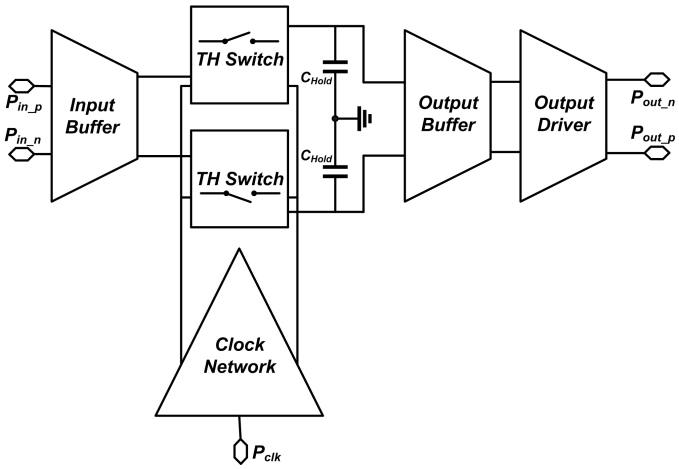

Fig. 1. Conceptual block diagram of the presented THA.

Interconnects are separated by $1\,\mu\mathrm{m}$ BCB interlayer dielectric layers. MIM capacitors are $0.3\,\mathrm{fF}/\mu\mathrm{m}^2$ and thin-film resistors are $50\,\Omega/\mathrm{square}$.

III. Track and Hold Amplifier Design

The conceptual block diagram of the THA presented in this paper is shown Fig. 1 where the track and hold switches are operating with the sampling rate defined by the clock network. $50\,\Omega$ match in the input and output is provided by the input buffer and the output driver stages. The input buffer is also designed to provide the high linearity in the input (IIP3) of the amplifier.

Figure 2 represents the schematic of the input buffer, two track and hold switches and the output buffer. The main core of the input buffer ($Q_{1\text{-}6}$) consists of two degenerated differential pairs where the linearity error caused by V_{BE} modulation of $Q_{1,2}$ is compensated by the one of $Q_{5,6}$ and consequently a high linearity buffer is achieved.

The design of track and hold switches is benefited of using high speed base-collector (BC) diodes rather than base-emitter (BE) in the form of switched emitter follower stages for the following reasons:

1) Fast HBTs in this technology are fabricated using thin and highly doped BE junctions which degrades the break-down voltage [6],[7].

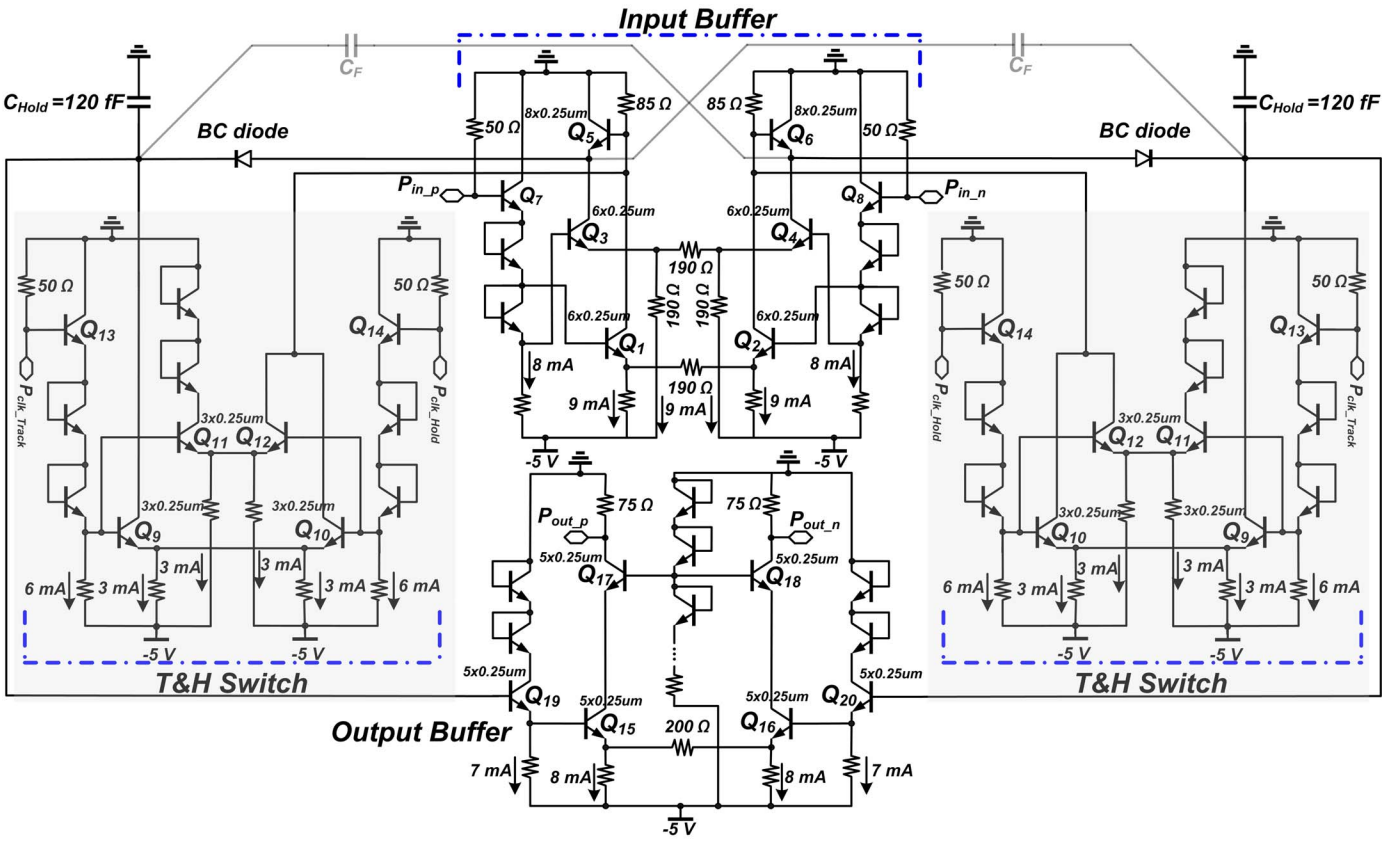

Fig. 2. Circuit schematic of the input buffer cascaded with two T&H switches and the output buffer.

2) The time constant of $R_{on}C_{off}$ (where R_{on} is the forward bias resistance of the diode and C_{off} is the depletion region capacitance) in the BE diode is much larger than the one in the BC diode which makes the BC diode a faster switch.
3) BC diode in DHBT technology has minority carrier storage time approximately equal to base transit time (in the order of $40\,\mathrm{fs}$) which is much smaller in contrast to homojunction (BJTs) and single HBTs where the BC junction suffers from large hole minority carrier storage time in the subcollector, resulting in a large reverse recovery time. For this reason, the BC diode is of advantage in the InP/InGaAs DHBT technology, but would perform poor in GaAs/AlGaAs SHBT and SiGe/Si bipolar processes.
4) The Track & Hold switch designed by BC diode does not suffer from instability issues of emitter followers and consequently reduces the excessive peaking in the AC response of the THA circuit.

The operation of the track and hold switches can be explained as follows:

- In the track mode, transistor Q_9 is conducting and its $6\,\mathrm{mA}$ current is drawn from the BC diode which cause the input signal to appear across the hold capacitance (C_{hold}). The value of MIM hold capacitance is selected as $120\,\mathrm{fF}$ based on the design methodology reported in [2].
- In the hold mode, Q_{10} and Q_{12} are conducting and a total current of $12\,\mathrm{mA}$ is drawn from the $85\,\Omega$ load resistor of the input buffer and provides a voltage drop of $1\,\mathrm{V}$ across the resistor. This voltage drop completely turns off the BC diode whose $V_{BE\text{-}on}$ is $0.8\,\mathrm{V}$. The reason to choose such a large voltage drop is to have a large dynamic range for all the various sampling rates specially for sampling rates lower than the Nyquist rate where the large signal swings in the output of the input buffer can turn on the BC diode if it is not fully turned off. The values of the feedthrough cancellation capacitors (C_F) are selected equal to the value of the BC diode capacitance in this design.

Since the goal of this work was to design a Sample & Hold circuit where two master and slave THAs are cascaded and operate in opposite modes, by turning off the output buffer in the hold mode, the valid data in the output of the master THA becomes inaccessible for the slave THA to be read. Therefore, the output buffer of THA is designed to be always in the on state in the price of having signal droop during the hold mode.

The core of the output driver [shown in Fig.1] is a degenerated differential pair with $50\,\Omega$ loads and a $120\,\Omega$ degeneration resistor with the tail current of $35\,\mathrm{mA}$ while another differential pair with a $35\,\mathrm{mA}$ tail current is preceding that.

The clock network of THA is designed by cascading a Cherry-Hooper amplifier with the differential common emitter stages and it converts the single-ended $150\,\mathrm{mV_{p\text{-}p}}$ clock signal to a $300\,\mathrm{mV_{p\text{-}p}}$ differential signal which is applied to the track and hold switches.

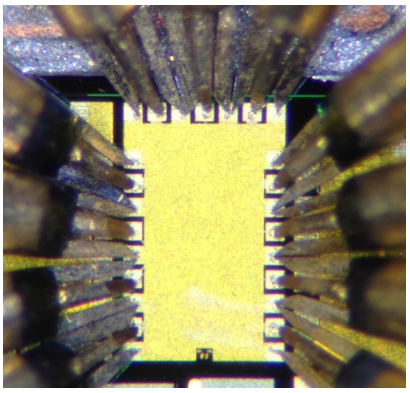

Fig. 3. Die-photo of the THA ($0.675 \times 1.075\,\mathrm{mm}^2$)

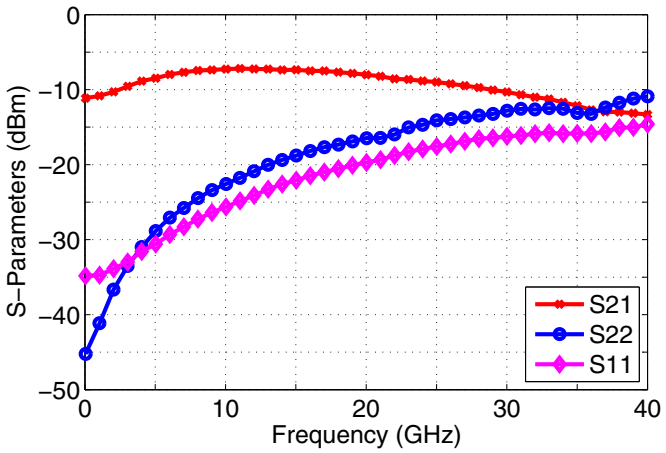

Fig. 4. Measured single-ended THA input return loss (S_{11}), output return loss (S_{22}) and transmission (S_{21})

IV. Measurement Results

The THA chip shown in Fig. 3, consumes $130\,\mathrm{mA}$ and $220\,\mathrm{mA}$ from power supplies of $-5\,\mathrm{V}$ and $-2.5\,\mathrm{V}$, respectively. The clock network and the output driver are drawing $150\,\mathrm{mA}$ and $70\,\mathrm{mA}$ respectively, from the $-2.5\,\mathrm{V}$ supply.

2-port RF measurements of the THA were performed from $100\,\mathrm{MHz}$ to $40\,\mathrm{GHz}$ using an Agilent PNA-X N5245 network analyzer after LRRM calibration. The non-stimulated input and output ports were terminated by a $50\,\Omega$ termination. The single-ended S-parameters in the track mode are shown in Fig. 4.

Time-domain measurements were conducted using Rohde & Schwarz SMF 100A signal generator for the input signal and Agilent E8257D-M50 $50\,\mathrm{GHz}$ signal generator for the clock source. Figure 5 which has been captured by an Agilent 86100A wide-band Oscilloscope, shows a differential output signal at $10\,\mathrm{GHz}$ which is being sampled by $50\,\mathrm{GSamples/s}$ sampling rate.

Figure 6 shows the spectral content of a two tone test at $18\,\mathrm{GHz}$. Using a Rohde & Schwarz FSU $20\,\mathrm{Hz}$-$46\,\mathrm{GHz}$ spectrum analyzer, the fundamental signal powers and their corresponding third-order intermodulation products were cap-

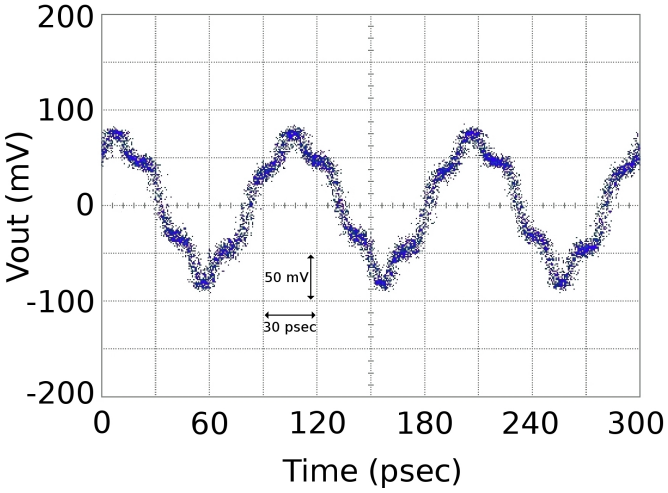

Fig. 5. Measured differential output of a $10\,\mathrm{GHz}$ RF input signal sampled with a $50\,\mathrm{GSamples/s}$ sampling rate

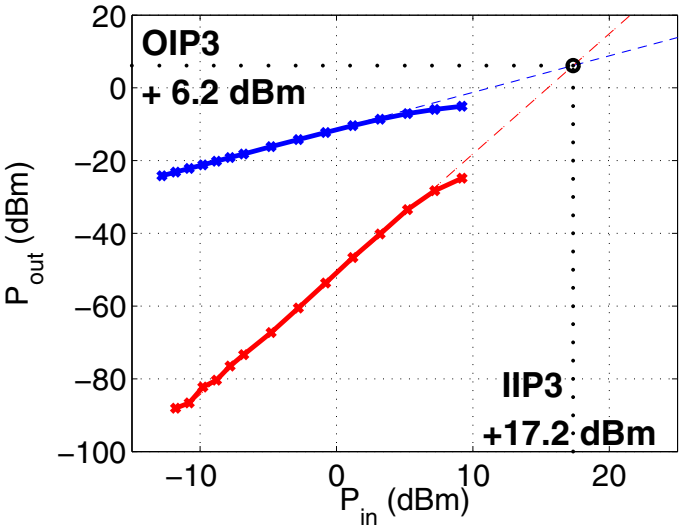

Fig. 6. Results of IP3 measurement by applying two frequency tones at 18 and 18.100 GHz. The output power (P_{out}) has been measured using the Spectrum Analyzer with the settings of RBW = 10 kHz VBW = 10 kHz, Ref. Level = 0 dBm and RF Attn. = 0 dB.

tured by sweeping the input power over the range of -10 to $+10\,\mathrm{dBm}$. The extrapolated IIP3 and OIP3 are $+17.2\,\mathrm{dBm}$ and $+6.2\,\mathrm{dBm}$, respectively. Using the same measurement methodology, IIP3 and OIP3 of the THA has been extracted and shown in Fig. 7 over the input frequency range of 2 to $22\,\mathrm{GHz}$. Fig. 7 shows an IIP3 more than $+16\,\mathrm{dBm}$ up to $22\,\mathrm{GHz}$ which verifies the high linearity of the THA circuit.

The harmonic distortion of the THA has been investigated by measuring the spectral content of the single-ended output for a $15\,\mathrm{GHz}$ input signal by sweeping its input power up to the P1dB level of the THA at this frequency. Figure 8 shows an HD2 and HD3 of $-15.5\,\mathrm{dB}$ and $-30.3\,\mathrm{dB}$, respectively at the input power of $+7.5\,\mathrm{dBm}$ which is the P1dB compression point of the THA at $15\,\mathrm{GHz}$.

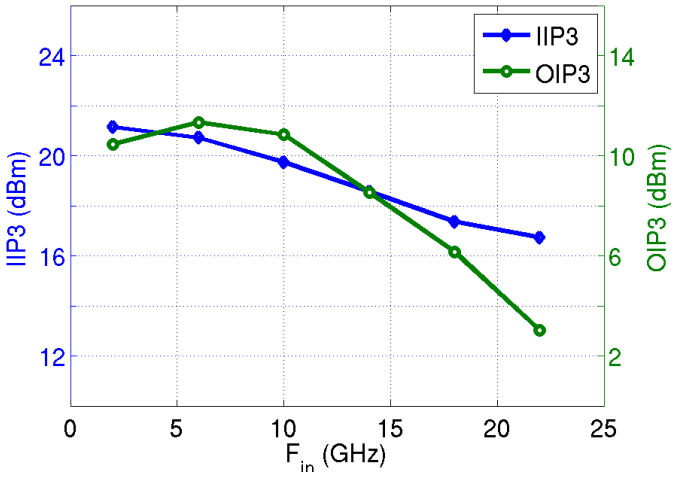

Fig. 7. Measured IP3 versus RF input signal frequency.

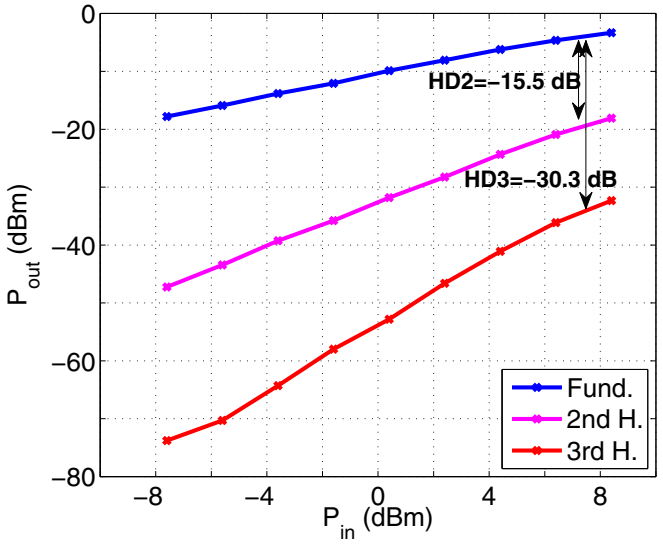

Fig. 8. Single-ended spectral characterization at the input signal frequency of 15 GHz.

Figure 9 presents the spectral characteristics of a beat frequency test with $f_{in} = f_s + \Delta f$ where $f_s = 40\,\mathrm{GHz}$ and $\Delta f = 2\,\mathrm{MHz}$ at an input power of $+3\,\mathrm{dBm}$ with the 3^{rd}-order harmonic distortion of $-38.8\,\mathrm{dB}$.

V. Conclusion

A $50\,\mathrm{GSamples/s}$ THA has been designed using fast base-collector diodes and fabricated in $0.25\,\mu\mathrm{m}$ InP HBT technology. The reported THA has the fastest sampling rate among the reported THAs [4],[5] in the InP HBT technology. Time-domain measurement at $50\,\mathrm{GSamples/s}$ sampling rate is presented for a $10\,\mathrm{GHz}$ signal. The THA achieves IIP3 more than $+16\,\mathrm{dBm}$ up to $22\,\mathrm{GHz}$ of the input signal frequency which makes it a proper choice for high speed ADC applications. An example of spectral characterization at $15\,\mathrm{GHz}$ shows an HD3 of $-30.3\,\mathrm{dB}$ at the P1dB input power of THA which is $+7.5\,\mathrm{dBm}$. Finally, the beat frequency test at $40\,\mathrm{GHz}$ with $\Delta f = 2\,\mathrm{MHz}$ exhibits an HD2 of $-38.8\,\mathrm{dB}$.

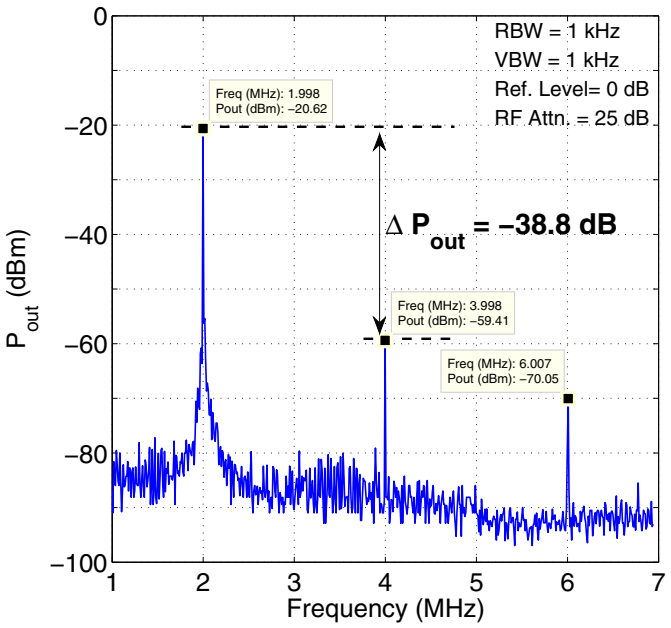

Fig. 9. Beat frequency test where a $40.002\,\mathrm{GHz}$ input signal is being sampled by $40\,\mathrm{GSamples/s}$ sampling rate.

Acknowledgments

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