

Near-Junction Thermal Management for Wide Bandgap Devices

Avram Bar-Cohen, John D. Albrecht

Defense Advanced Research Projects Agency
3701 North Fairfax Drive, Arlington, VA 22203, U.S.A.

Joseph J. Maurer

Booz Allen Hamilton Inc.
3811 North Fairfax Drive, Arlington, VA 22203, U.S.A.

Abstract— Near-junction thermal management is critical to achieving the promise of electronic and photonic devices using wide bandgap materials. In such devices, including GaN HEMTs in PAs, the thermal resistance associated with the “near-junction” region dominates the heat removal path and is often as large as the thermal resistance of all the other elements in the resistance chain. As part of DARPA’s portfolio in Thermal Management Technologies (TMT), efforts are underway to develop transformative, paradigm-changing cooling techniques. This paper will briefly review the thermal management needs of WBG devices and DARPA’s Thermal Management Technologies portfolio, with emphasis on the goals and status of these efforts relative to the current State-of-the-Art. Attention will then turn to promising options in near-junction cooling and the challenges inherent in realizing their potential for WBG device thermal management.

Keywords- Gallium Nitride, WBGS, compound semiconductors, power amplifiers, Near-junction thermal transport, thermal management technologies.

I. INTRODUCTION

Over the past several years, the Defense Advanced Research Projects Agency (DARPA) has made a sustained investment in advancing the state-of-the-art of GaN-related material and devices such as light emitting diodes, lasers, and MMICs. For electronics applications, the Wide Band Gap Semiconductors for RF Electronics (WBGS-RF) program [1] resulted in devices that simultaneously met or exceeded all of the program objectives in the initial and intermediate phases. The on-going program is developing WBGS MMICs and will demonstrate their utility in DoD system applications. A related effort, the Nitride Electronic NeXt Generation (NEXT) technology program has also been funded to develop further enhanced nitride transistor technology [1].

The performance improvements available from GaN-based devices result from material characteristics that allow high electron sheet charge densities in transistor channels and very high electrical breakdown fields. In GaN electronics applications, the use of relatively high thermal conductivity SiC substrates has provided enhanced thermal management capability compared to that achieved with Si and Sapphire substrates. GaN-on-SiC based transistors enable power amplifiers that have significantly higher output power, power added efficiency (PAE), and power density than is presently

available from amplifier circuits based on other materials, such as GaAs or InP. However, despite the thermal improvement offered through the use of SiC substrates, GaN power devices are often thermally limited. For example, GaN HEMTs have been demonstrated with output power densities over 30 W/mm at high bias [1], but are typically limited to power densities approaching 7 W/mm when in a realistic GaN PA architecture at moderate bias [4].

The primary thermal bottleneck in these GaN devices occurs in a region within 100 μm of the electronic junction, or the so-called “near-junction” region, often consisting of an epitaxial layer of several microns on a thicker substrate, typically SiC, Si, or Sapphire, where the local heat flux exceeds that encountered on the surface of the sun. Thus, as noted by Garven and Calame [5], within an individual HEMT conductive channel, the localized heat fluxes can exceed 1 MW/cm², over a 150 μm wide by 0.5 μm gate, and a MMIC-with 50 μm gate-to-gate spacing - could experience average heat fluxes of 10 kW/cm² over the transistor footprint.

This paper will present a brief summary of DARPA’s Thermal Management Technologies Portfolio including a preview of the Near Junction Thermal Transport effort. It will then review the current thermal reality of GaN devices including a close examination of the thermal resistance of the epitaxial layer in these devices and the challenge this layer poses to potential thermal enhancements. It will present possible approaches to near junction thermal transport of GaN electronic devices and some of the associated challenges of these approaches.

II. THERMAL MANAGEMENT TECHNOLOGIES PORTFOLIO

Significant enhancements in fundamental device materials, technologies, and system integration have led to rapid increases in the total power consumption of DoD systems. In many cases, power consumption has increased while system size has decreased, leading to an even steeper increase in dissipated heat density. Thermal management often imposes the main obstacle to further enhancements of DoD electronic systems.

The overarching goal of the DARPA Thermal Management Technologies (TMT) portfolio is to explore and optimize new nanostructured materials and other recent advances for use in thermal management systems. The program is divided into five technical thrusts: Thermal Ground Plane (TGP),

Microtechnologies for Air-Cooled Exchangers (MACE), NanoThermal Interfaces (NTI), Active Cooling Modules (ACM), and Near Junction Thermal Transport (NJTT). A schematic of the typical thermal resistance chain from the junction to the heat exchanger – reflecting the potential impact of the TMT program - is shown in Figure 1.

The TGP thrust is focused on high-performance heat spreaders capable of operating at high g-loads while using phase-change processes to replace thermal conduction in conventional solid metal and ceramic spreaders. The goal of the MACE thrust is to enhance air-cooled exchangers by reducing the thermal resistance through the heat sink to the ambient, increasing convection through the system, improving heat sink fin thermal conductivity, optimizing and/or redesigning the complimentary heat sink blower, and increasing the overall system (heat sink and blower) coefficient of performance. The NTI thrust is focused on novel materials and structures that can provide significant reductions in the thermal resistance of the thermal interface layer between the backside of an electronic device and the next layer of the package, while maintaining high mechanical compliance. The fourth thrust of the TMT program is ACM, which is investigating active cooling of electronic devices using techniques such as thermoelectric coolers and compact Sterling cycle refrigerators. The fifth and final thrust of TMT is a new effort, NJTT, which is focused on achieving a 3x improvement in power handling from GaN power amplifiers through improved thermal management within 100 μm of the electronic junction. NJTT represents the most difficult thermal challenge in the TMT portfolio, but offers the opportunity for large gains in performance from GaN electronic devices.

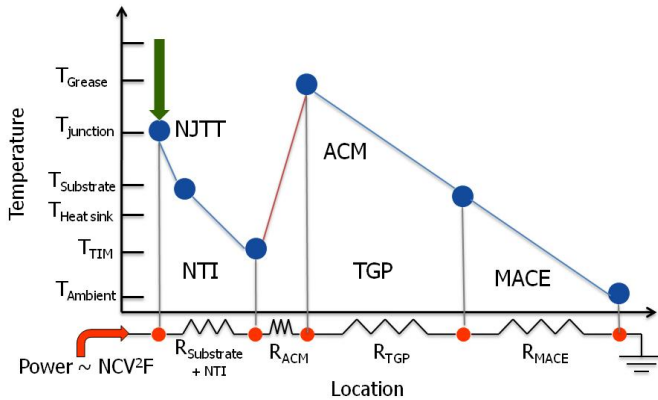


Figure 1. A schematic of the potential impact of the TMT portfolio on the various thermal resistances in a representative device.

III. THERMAL LIMITATIONS OF CURRENT GAN DEVICES

GaN HEMTs have been demonstrated with output power densities over 30 W/mm at high bias [1], but are typically limited to power densities approaching 7 W/mm when in a realistic GaN PA architecture at moderate bias [4]. This limitation is due in large part to the challenge of thermally managing the large local heat fluxes that are created in the near junction region of these devices. In order to attempt to address the near junction thermal management of GaN devices, the sources of thermal resistance in the current device stacks must

be examined. Figure 2, shows a schematic of the thermal resistance chain of a GaN-on-SiC HEMT device. Starting from the bottom is the SiC substrate. SiC substrates offer an improvement in thermal conductivity with $k = 400 \text{ W/mK}$, as compared to Si, $k = 150 \text{ W/mK}$, and Sapphire, $k = 35 \text{ W/mK}$. However, the full benefit of the SiC substrate is not realized, due to the impact of the thermal boundary resistance, or TBR, of the GaN-SiC interface [6]. In their work Sarua et al found that the TBR of $\sim 3.3 \times 10^{-4} (\pm 15\%) \text{ cm}^2\text{K/W}$ for the GaN-SiC and GaN-Si interface, resulted in an increase in the GaN HEMT channel temperature rise by about 30% for GaN-on-SiC and 10% for GaN-on-Si as compared to a near-perfect interface with a negligible TBR. For GaN-on-Sapphire, for which the conduction in sapphire governs thermal transport away from the GaN transistor, the impact of the TBR at the GaN-Sapphire interface is minimal despite an even higher TBR of $1.2 \times 10^{-3} \text{ cm}^2\text{K/W}$, with only a 2-4% increase in the temperature rise relative to a stack with a negligible TBR.

To better understand the occurrence of the TBR at the GaN-substrate interface, it is instructive to focus on the AlN nucleation layer, NL, used to stimulate the GaN growth and the adjacent epitaxial layers of GaN. The influence of this layer on a variety of GaN-on-SiC stacks was closely investigated by Manoi et al [7]. In this work, the AlN thermal conductivities were found to range between 1.5 to 23 W/mK, which is between one and two orders of magnitude lower than single crystal AlN, $k = 319 \text{ W/mK}$. There was a corresponding trend of the effective k of the NL to improve as it was made thicker, $k = 2.2 \text{ W/mK}$ for 40 nm thick NLs and 14.3 W/mK for 200 nm thick NLs. However, since the layer thermal resistance is proportional to the ratio of thickness to conductivity, it was found that the k of the AlN NL did not increase fast enough with the thickness to make this an effective strategy for reducing the TBR. The variation in TBR due to these NLs ranged from $1.5 \times 10^{-4} \text{ cm}^2\text{K/W}$ to $5 \times 10^{-4} \text{ cm}^2\text{K/W}$, which would result in an additional channel temperature rise of 10%-40% compared to the negligible TBR case.

Based on the results presented in [6-7], it is clear that the full benefit of the SiC substrate is not being realized in current devices and that any improvement in the near-junction thermal transport from GaN transistors will require taking into account the TBR of this nucleation layer

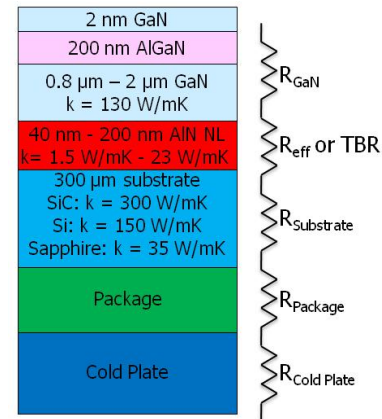


Figure 2. A schematic of a representative GaN device thermal stack with its associated thermal resistances.

IV. CANDIDATE APPROACHES TO NJTT

In order to successfully deal with average heat fluxes of 10 kW/cm² and local heat fluxes approaching 1 MW/cm², we consider several possible approaches, including high thermal conductivity diamond substrates, microchannel liquid cooling, and on-chip thermoelectric coolers that could address near junction thermal management.

A. High Conductivity Substrates

The use of a higher conductivity substrate such as diamond is seemingly the most straightforward path to NJTT. Diamond has an intrinsic thermal conductivity of 2000 W/mK at room temperature [8]. There have been many attempts to utilize diamond as a substrate for GaN HEMT devices [9-11], but none of these has as yet been able to deliver on the full promise of a diamond substrate. Successful implementation of a GaN-on-diamond approach requires minimizing the aforementioned TBR at the GaN-diamond interface, achieving the intrinsically high thermal conductivity of the diamond in a thin layer, and growing a sufficiently thick layer of diamond to provide effective heat transfer without undue wafer bow.

Due to its higher intrinsic conductivity, minimizing the TBR of the GaN-diamond interface is even more critical to realizing the promise of diamond substrates [9, 11]. If the GaN epitaxy is to be transferred to a diamond substrate from another carrier, it is possible to remove the AlN layer and adjacent GaN buffer layer by etching or other processes. However, an additional interfacial thermal resistance is created by bonding the diamond substrate to the GaN. Indeed, to this point, GaN-on-Diamond devices have had both a full GaN epitaxial layer and an adhesive layer. While few details are available regarding the specific materials and thicknesses used to bond the diamond substrates to the GaN, following [12] it is possible to approximate the bond resistance based on one-dimensional conduction as δ/k - where δ is the thickness of the adhesive material and k is the thermal conductivity of the adhesive. Assuming an allowable bond-layer resistivity of 1×10^{-4} cm²K/W, an adhesive layer with $k = 1, 10, \text{ or } 100$ W/mK, would be limited to a maximum thickness of $\delta = 10, 100, \text{ and } 1,000$ nm respectively.

Another challenge is producing diamond with sufficiently high thermal conductivity to warrant transferring the GaN epitaxy. Indeed in several reports of GaN-on-Diamond devices, the CVD-grown diamond substrates have been limited to $k = 1200$ W/mK. In looking closely at CVD diamond [13], it was found that the thermal properties of CVD diamond strongly depend on the microstructure of the material, which is highly sensitive to factors such as the ratio of methane to hydrogen. Moreover, the diamond conductivity has been found to be anisotropic, with k in the z direction being greater than k in the lateral direction, and also thickness dependent, with k increasing as the diamond becomes thicker [14]. In order for the potential benefits of diamond substrates to be realized, the growth process of the diamond must be carefully selected and controlled.

An additional concern is the growth of sufficiently thick diamond with minimum wafer bow over a large diameter

wafer, preferably 50mm (2") or greater. Wafer bow has stymied attempts to conventionally process GaN-on-Diamond devices requiring that they be fabricated with electron beam lithography or other non-standard methods. Indeed a wafer bow of 50 μm over 1 cm² was reported in one of the best performing GaN-on-Diamond HEMT devices to-date, which had to be fabricated using e-beam lithography using a 25 μm thick, 15 x 15 μm substrate [9]. Recently, the first reported GaN-on-Diamond HEMT was fabricated using conventional device processing techniques, on a 130 μm thick, 30 mm (~1") diamond wafer [11].

B. Microchannel Liquid Cooling

The use of copper and SiC microchanneled coldplates for thermal management of GaN PA's has been simulated and demonstrated at the package level for GaN-on-SiC devices [15-16] and also for other types of power electronics [17-18]. These studies have, however, focused on lower heat fluxes than targeted for today's wide bandgap devices, reporting results for typical peak heat fluxes in the range of 0.5 to 5 kW/cm². Moreover, these studies have generally not attempted to address the TBR and/or bonding resistances between the GaN layer and substrate.

To meet the thermal management challenge of wide bandgap devices, significant enhancement of these first-generation liquid cooling approaches will need to be considered. Use of a higher thermal conductivity material in the microchanneled coldplate than the commonly considered copper and SiC, ranging from a graphite/metal composite to graphite in its various forms to graphitic diamond and onto high conductivity diamond, offering as much as a factor of 4 improvement in thermal conductivity relative to SiC, can all be expected to contribute to lower thermal resistances between the HEMT's and the liquid coolants. It is to be noted that the use of a hybrid diamond/silicon microchannel cooler bonded to a GaN-on-SiC chip, is explored in [15,16], showing improved thermal performance relative to a copper cooler, but at the expense of additional mechanical stress in the SiC substrate.

It should also be recognized that the convective heat transfer coefficients in the microchannel coolers can be improved by the use of so-called "manifold microcoolers" relying on local re-distribution of the fluid into relatively short "entry length" microchannels capable of providing a factor of 2 enhancement in the local heat transfer coefficients [19-21]. Further reductions in the convective thermal resistance could, perhaps, be achieved by use of unconventional coolants, such as liquid metals, slurries, and nanofluids [22]. Substantial additional enhancements in heat transfer and significantly lower pumping power losses could result from utilizing phase-change cooling in the microchannels - leading to higher heat transfer coefficients than single-phase convection - and reducing the operating temperature of the coolant to conventional refrigeration levels (-5 °C to -20 °C) or down to the cryogenic liquid nitrogen temperature range of perhaps -270 °C.

To fully exploit the microcooler performance enhancements that could be realized by these means, attention will also have to be devoted to reducing the "die-attach" thermal resistance, between the MMIC and the microcooler. Successful

completion of the DARPA NTI program, described above, will result in reducing this resistance by an order-of-magnitude relative to the COTS thermal interface materials to values approaching $0.01\text{cm}^2\text{K/W}$. However, for the target MMIC heat flux of $5\text{--}10\text{kW/cm}^2$, even these improved TIMs will create an unacceptable temperature rise of $50\text{--}100\text{K}$ across the die-attach layer.

To deal with this parasitic thermal resistance, it is possible to directly liquid cool the MMIC, microchanneling the Si or SiC substrate and pumping single phase or evaporating liquid, a refrigerant, or cryogen thru the miniature passages. This approach, implemented by dielectric evaporative cooling of an LED submount, is described in detail by Kim et al [23] who report experimental two-phase, area-averaged heat transfer coefficients of the dielectric FC-72 reaching $10\text{ kW/m}^2\text{K}$, and reducing the overall junction-to-coolant resistance by a factor of two, from 12.95 K/W to less than 6 K/W [23]. Alternatively, the substrate – with or without finned protrusions – could be directly cooled by immersion in a quiescent pool or a pumped, though unconfined, flow of a dielectric liquid, refrigerant, or cryogen. The application of this approach to thermal management of high heat flux, 3D silicon chip stacks, with the commercial dielectric liquid FC-72 circulating through the inter-chip interconnect gaps, revealed that more than 2kW/cm^3 could be extracted from the chip stack with flow boiling [24].

C. On-Chip Thermoelectric Coolers

In much the same way as liquid cooling, direct on-chip application of thermoelectric cooling can be expected to help address, singly or in conjunction with the other techniques described, the near junction thermal management of wide bandgap devices. Conventional thermoelectric coolers can only provide a cooling heat flux of about 10 W/cm^2 , but recent advances in miniaturized TECs have led to Bi_2Te_3 -based miniaturized TECs that are just 10's of microns thick and capable of removing 100's of W/cm^2 of dissipated heat [25]. Such TECs have been applied to the cooling of high power silicon chips, connecting through a mini-contact pad which concentrates the thermoelectric cooling power on a small area of the chip. It has been shown that when properly optimized these mini-contact enhanced, miniaturized “bulk” TECs can yield hot spot temperature reductions in excess of 15°C for sub-millimeter-sized hot spots with heat fluxes approaching the kW/cm^2 -level [26–28]. Even higher “hot spot” heat fluxes, but – thus far – only modest temperature reductions, could be achieved by relying on the inherent thermoelectric properties of the common substrate materials [29–30].

V. CONCLUSIONS

A review of the thermal management challenges facing current wide bandgap devices, specifically GaN HEMT devices, has focused attention on the large magnitude of the local and average heat flux at the base of such devices and the constraints imposed by the Thermal Boundary Resistance (TBR), the anisotropy of the high-conductivity substrates, and current microchanneled coldplates. It is suggested that the introduction of techniques for low thermal resistance bonding

to high conductivity substrates, use of enhanced single-phase and two-phase microcoolers, and integration of advanced thermoelectric coolers into the thermal stack could materially raise the thermal limits on wide bandgap device performance. The thermal benefits of embedding thermal management in the MMIC have also been discussed. These efforts are placed in the context of ongoing DARPA programs in RF wide bandgap devices and thermal management technologies.

ACKNOWLEDGMENT

The authors acknowledge the support of the government team and the outstanding achievements of performers who are involved in DARPA’s Thermal Management Technologies program portfolio.

Disclaimer: The views, opinions, and/or findings contained in this article/presentation are those of the author/presenter and should not be interpreted as representing the official views or policies, either expressed or implied, of the Defense Advanced Research Projects Agency or the Department of Defense.

Distribution Statement A, Approved for Public Release, Distribution Unlimited.

REFERENCES

- [1] M. J. Rosker, C. Bozada, H. Dietrich, A. Hung, D. Via, S. Binari, E. Vivieros, E. Cohen, and J. H. Hodiak, “The DARPA Wide Band Gap Semiconductors for RF Applications (WBGs-RF) Program: Phase II Results,” *CS Mantech*, 2009.
- [2] J.D. Albrecht, T-H. Chang, A.S. Kane, M.J. Rosker “DARPA’s Nitride NeXt Generation Technology Program”, *IEEE CS/ICS*, 2010.
- [3] Y.F. Wu, A. Saxler, M. Moore, R.P. Smith, S. Sheppard, P.M. Chavakar, T. Wisleder, U.K. Mishra, P. Parikh, “ 30--W/mm GaN HEMTs by Field Plate Optimization”, *IEEE Electron Device Letters*, v. 25, pp. 117–119, 2004.
- [4] E. Reese, D. Allen, C. Lee, T. Nguyen. “Wideband Power Amplifier MMICs Utilizing GaN on SiC”, *IEEE IMS*, 2010.
- [5] M. Garven and J.P. Calame. “Simulation and Optimization of Gate Temperatures in GaN-on-SiC Monolithic Microwave Integrated Circuits”. *IEEE Transactions on Components and Packaging Technologies*, v. 32, pp. 63–72, 2009.
- [6] A. Sarua, H. Ji, K.P. Hilton, D.J. Wallis, M. J. Uren, T. Martin, M. Kuball, “Thermal Boundary Resistance Between GaN and Substrate in AlGaIn/GaN Electronic Devices.” *IEEE Transactions on Electron Devices*, v. 54, pp. 3152–3158, 2007.
- [7] A. Manoi, J.W. Pomeroy, N. Killat, M. Kuball. “Benchmarking of Thermal Boundary Resistance in AlGaIn/GaN HEMTs on SiC Substrates: Implication of the Nucleation Layer Microstructure.” *IEEE Electron Device Letters*, v. 31, pp. 1395–1397, 2010.
- [8] R. Berman, F.E. Simon, J. Wilks. “Thermal Conductivity of Dielectric Crystals: The ‘Umklapp’ Process.” *Nature*, v. 168, pp.277–280, 1951.
- [9] J.G. Felbinger, M.V.S Chandra, Y. Sun, L.F. Eastman, J. Wasserbauer, F. Faili, D. Babic, D. Francis, F. Ejeckam. “Comparison of GaN HEMTs on Diamond and SiC substrates.” *IEEE Electron Device Letters*, v. 28, pp. 948–950, 2007.
- [10] J.W. Zimmer, G. Chandler. “Advances in Large Diameter GaN on Diamond Substrates”, *CS Mantech Conference*, 2008.
- [11] K.D. Chabak, J.K. Gillespie, V. Miller, A. Crespo, J. Roussos, M. Trejo, D.E. Walker, Jr., G.D. Via, G.H. Jessen, J. Wasserbauer, F. Faili, D. I. Babic, D. Francis, F. Ejeckam. “Full-Wafer Characterization of AlGaIn/GaN HEMTs on Free-Standing CVD Diamond Substrates.” *IEEE Electron Device Letters*, v. 31, pp. 99–101, 2010.
- [12] H.C. Nohetto, N.R. Jankowski, A. Bar-Cohen, “Modeling the Impact of the GaN/Substrate Thermal Interfacial Resistance on the Performance of a HEMT Device.” *IMECE*, 2011. *In preparation*.

- [13] Y. Yang, S.M. Sadeghipour, W. Liu, M. Asheghi, M. Touzelbaev. "Thermal Characterization of the High Thermal Conductivity Dielectrics." In S. L. Shinde, J. Goela (Eds.), *High Thermal Conductivity Materials*, Ch. 3, pp. 69-118, Springer 2005.
- [14] J.E. Graebner, S. Jin, G.W. Kammlott, J.A. Herb, C.F. Gardinier. "Large Anisotropic Thermal Conductivity in Synthetic Diamond Films." *Nature*, v. 359, pp. 401-403, 1992.
- [15] J.P. Calame, R.E. Myers, F. N. Wood, S.C. Binari. "Simulations of Direct-Die-Attached Microchannel Coolers for the Thermal Management of GaN-on-SiC Microwave Amplifiers." *IEEE Transactions on Components and Packaging Technologies*, vol. 28, pp. 797-809, 2005.
- [16] J.P. Calame, R.E. Myers, S.C. Binari, F.N. Wood, M. Garven. "Experimental Investigation of Microchannel Coolers for the High Heat Flux Thermal Management of GaN-on-SiC Semiconductor Devices." *International Journal of Heat and Transfer*, vol. 50, pp. 4767-4779, 2007.
- [17] N.R. Jankowski, L. Everhart, B.R. Geil, C. Wesley Tipton, J. Chaney, T. Heil, W. Zimbeck. "Stereolithographically Fabricated Aluminum Nitride Microchannel Substrates for Integrated Power Electronics Cooling." *ITHERM*, pp. 180-188, 2008.
- [18] P. Wang, F.P. McCluskey, A. Bar-Cohen. "Isothermalization of an IGBT Power Electronic Chip." *IMECE*, pp. 1-11, 2010.
- [19] L. Everhart, N. Jankowski, B. Geil, A. Bayba, D. Ibitayo, P. McCluskey. "Manifold Microchannel Cooler for Direct Backside Liquid Cooling of SiC Devices." *ICNMM*, pp. 285-292, 2007.
- [20] L. Boteler, N. Jankowski, B. Geil, P. McCluskey. "A Micromachined Manifold Microchannel Cooler." *IMECE*, pp. 61-68, 2009.
- [21] E. Kermani, S. Dessiatoun, A. Shoostari, M.M. Ohadi. "Experimental Investigation of Heat Transfer Performance of a Manifold Microchannel Heat Sink for Cooling of Concentrated Solar Cells." *Electronic Components and Technology Conference*, pp. 453-459, 2009.
- [22] P. Keblinski, J.A. Eastman, D.G. Cahill. "Nanofluids for Thermal Transport." *Materials Today*, pp. 36-44, June 2005.
- [23] D-W. Kim, E. Rahim, A. Bar-Cohen, B. Han. "Direct Submount Cooling of High Power LEDs." *IEEE Transactions on Components and Packaging Technologies*, vol. 33, 2010.
- [24] A. Bar-Cohen, K.J.L. Geisler. "Cooling the Electronic Brain". *Mechanical Engineering*, pp. 38-41, April 2011.
- [25] A. Bar-Cohen, "Thermal Management of On-Chip Hot Spots and 3D Chip Stacks." *COMCAS*, pp. 1-8, 2009.
- [26] P. Wang, B. Yang, A. Bar-Cohen, "Mini-Contact Enhanced Thermoelectric Coolers for On-Chip Hot Spot Cooling." *Heat Transfer Engineering*, v. 30, pp. 736-743, 2009.
- [27] B. Yang, P. Wang, A. Bar-Cohen, "Mini-Contact Enhanced Thermoelectric Cooling of Hot Spots in High Power Devices." *IEEE Transactions on Components and Packaging Technologies*, v. 30, 2007.
- [28] I. Chowdhury, R. Prasher, K. Lofgreen, G. Chrysler, S. Narasimhan, R. Mahajan, D. Koester, R. Alley, R. Venkatasubramanian. "On-Chip Cooling by Superlattice-based Thin-Film Thermoelectrics." *Nature Nanotechnology*, v. 4, pp. 235-238, 2009.
- [29] P. Wang, A. Bar-Cohen. "On-Chip Hot Spot Cooling Using Silicon Thermoelectric Coolers." *Journal of Applied Physics*, v. 102, pp. 034503-1-11, 2007.
- [30] P. Wang, A. Bar-Cohen, "Self-Cooling on a Germanium Chip." *IEEE Transactions on Components and Packaging Technologies*, *In preparation*, 2011.