2001 Annual Report Conference on Electrical Insulation and Dielectric Phenomena

Metrology Development at NIST for Characterizing Wear-out and Reliability of Thin Gate Dielectrics

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Abstract The effect known as Time-Dependent-Dielectric-Breakdown (TDDB) occurs when thin gate silicon dioxide (SiO_2) films catastrophically break down without warning during normal operation. Recently, the reliability of gate oxides has become a critical concern as the thickness of the gate oxide is reduced. Thinner films result in higher gate electric fields and direct tunneling currents passing through the gate dielectric advancing dielectric wear-out and device failure. NIST has played a key role in conducting experiments to validate the physical models of dielectric breakdown. NIST also leads standards organizations in developing new test procedures used during production monitoring and process qualification to characterize the integrity and reliability of ultra-thin gate oxides. In this paper, metrology issues relating to the reliability testing and lifetime projection of thin gate oxides will be discussed as well as the role of NIST in the development of metrology for a new generation of advanced gate dielectric materials.

Introduction

The Metal Oxide Semiconductor Field Effect Transistor (MOSFET) is the fundamental building block in complex integrated circuits. One of the most important failure mechanisms affecting microelectronic devices involves the thin gate dielectric film used to insulate the gate electrode from the channel in the MOSFET. The effect known as Time-Dependent-Dielectric-Breakdown (TDDB) occurs when a voltage is applied to the thin silicon dioxide (SiO_2) film and it catastrophically breaks down without warning during normal operation.

TDDB can be characterized by conducting accelerated stress tests on test devices by using voltages and temperatures larger than those used for device operating conditions. A typical stress test involves applying a constant voltage on the gate dielectric film and noting the time at which it ruptures and conducts excessive current. The failure time data is used to extrapolate device lifetime from accelerated conditions to use conditions. The accuracy of the extrapolation depends on the validity of the assumed physical model of breakdown. Therefore, it is essential that the physical failure model be known over the range of stress voltages and temperatures used in the accelerated stress tests and in normal operating conditions.

The success of miniaturizing microelectronic devices is due in part to the ability to scale down the thickness of the SiO_2 used as the gate dielectric. Current microprocessor technologies utilize gate dielectrics thinner than 2 nm. The reliability of gate oxides at or below this thickness is a critical concern since devices operate at higher gate electric fields, and less stress-induced defects are required to initiate breakdown since the film is so thin.

A major difficulty in characterizing the reliability of ultra-thin films is detecting the breakdown event during a stress test. The breakdown event can be masked or hidden by the large tunneling currents passing through the gate dielectric during the test. Breakdown also becomes "soft" because the power dissipation required to produce a highly conductive path is limited due to the use of lower gate voltages.

Although the exact thickness limit for SiO_2 is not known, at MOSFET channel lengths below 70 nm the use of SiO_2 as the gate dielectric will no longer be possible due to excessive tunneling current. Eventually, a suitable replacement gate dielectric with a high permittivity (κ) must be used that exhibits a low leakage current and possesses the same performance and reliability of SiO_2.

This paper will discuss how NIST played a key role in validating the correct physical model for dielectric breakdown by conducting a comprehensive set of long-term TDDB experiments. The role of NIST in the development of new test procedures used during production monitoring and process qualification to characterize the integrity and reliability of ultra-thin gate oxides will be presented. How NIST is responding to the challenge of developing metrology for a new generation of advanced gate dielectric materials will also be presented.

Physics of Oxide Wear-Out

The confidence of gate oxide reliability predictions based on highly accelerated stress tests relies on the choice of the physical model for wear-out and

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breakdown. Several models were developed to explain the oxide breakdown mechanism. Two of the most

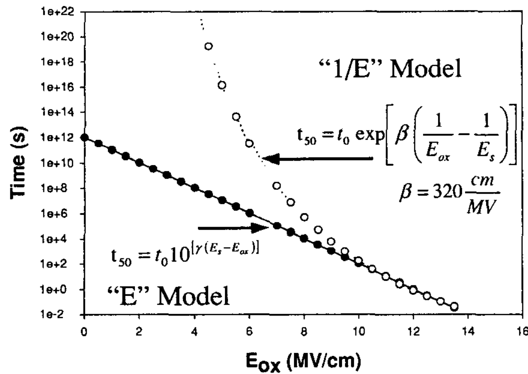

Figure 1: Plot illustrating the large differences in extrapolating oxide life using the linear "E" model and the reciprocal "1/E" model.

popular models include the linear electric field or "E" model [1,2] that assumes a thermodynamic process of defect creation, and the reciprocal "1/E" model [3,4] that assumes that the injection of holes from the anode region causes defects that eventually lead to breakdown. Figure 1 illustrates the differences in the prediction of oxide lifetime for both models. Note that the predictions of both models are similar for electric fields greater than 10 MV/cm, where most stress tests are conducted. However, there are over 10 orders of magnitude difference in the oxide lifetime at lower electric fields.

To determine the most physically correct model, NIST conducted long-term TDDB tests where high temperatures were used to accelerate failure [5]. This allowed tests to be conducted at much lower electric fields, where the differences in the two models could be observed. Figure 2 shows the results of these experiments.

Tests were conducted on 22-nm thick gate oxides over a wide range of stress electric fields and temperatures. A special water-cooled probe card was developed to facilitate wafer-level testing at temperatures up to 400 °C. The figure shows that there is very small difference between the two models at stress electric fields above 7 MV/cm; however, a deviation from the 1/E dependence is observed for stress electric fields below 7 MV/cm. Later studies [6-8] also verified a linear dependence of the log of the time-to-breakdown on electric field and voltage. It should be mentioned that the observed dependence on electric field does not necessarily validate a particular physical model, but does provide the functional form for reliability extrapolations.

Based on collaborations with several members of the U.S. Semiconductor Industry, NIST was able to

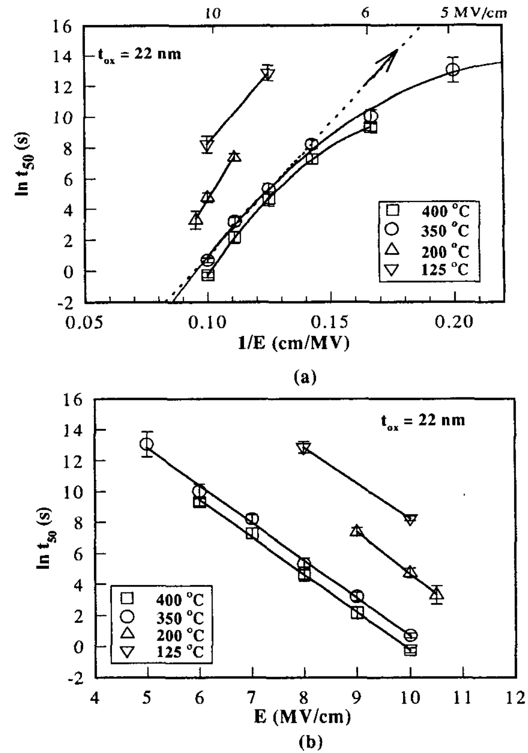

Figure 2: The natural log of oxide lifetime data plotted as a function of inverse stress electric field (a) and electric field (b) illustrating a deviation from the "1/E" model below 7 MV/cm shown as dashed lines.

conduct tests on many different oxide samples of varying thicknesses and processes. The tests yielded a consistent set of field and temperature acceleration parameters shown in Figures 3 and 4, respectively. Industry uses these parameters to make accurate predictions of device and product lifetime at normal

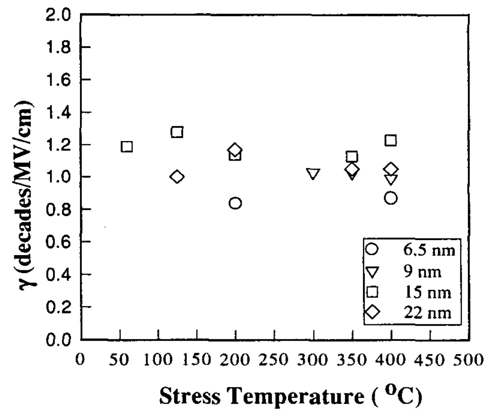

Figure 3: Electric field acceleration parameter plotted as a function of stress temperature obtained from a variety of oxide samples having different thicknesses and fabrication processes.

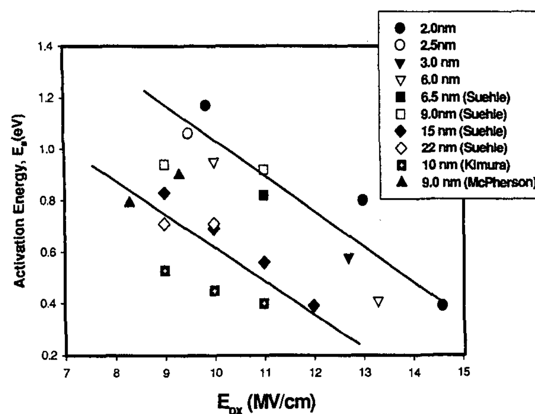

Figure 4: Plot showing the thermal activation energy versus gate electric field and compared to values reported for several different oxides. The straight line is only a viewing guide and does not imply a specific functional dependence.

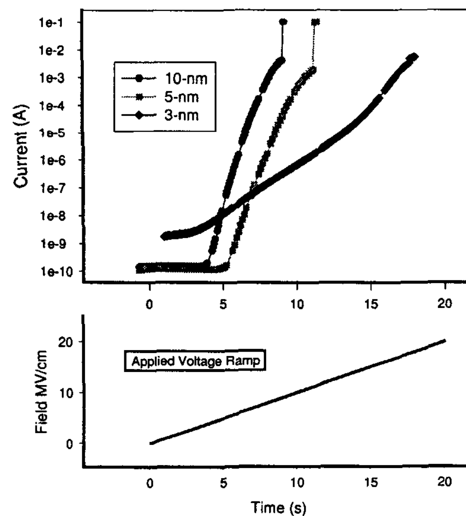

Figure 5: Current versus voltage characteristics for a 3 nm, 5 nm, and 10 nm thick oxide subjected to the JEDEC/ASTM ramped voltage breakdown test. Breakdown in the 3 nm sample cannot be observed and requires a new criterion for detection.

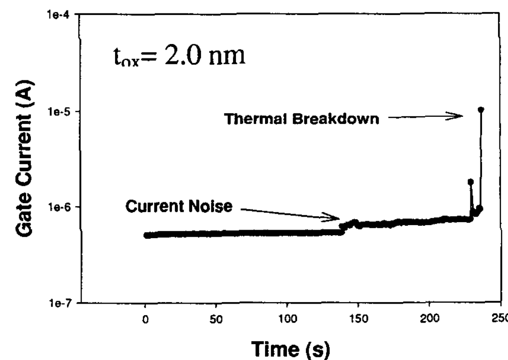

Figure 6: Tunneling current as a function of stress time for a 2.0 nm thick SiO_2 film. Note that soft breakdown is first observed.

operating voltages and temperatures.

Ultra-Thin Oxides: Measurement Dilemma

Characterizing the integrity and reliability of ultra thin SiO_2 films has become extremely challenging due to the difficulty in detecting breakdown in soft and noisy breakdown characteristics. There have been numerous reports that "soft" or "quasi" breakdown modes dominate as film thickness is scaled below 5 nm. Soft breakdown is attributed to limited thermal damage due to decreased stored energy [9] on the gate of the device or power dissipation [10] available during the breakdown process.

An example of soft breakdown is shown in Figure 5 for a JEDEC (Joint Electron Device Engineering Council)/ASTM (American Society for Testing of Materials) standard ramped voltage breakdown test. The figure shows the current passing through three SiO_2 samples having different thicknesses as the voltage is ramped. The breakdown event is clearly marked by a sudden surge in current for the 5 nm and 10 nm thick samples. However, there is no detectable current jump in the 3 nm thick sample. A second example is shown in figure 6 for a 2.0 nm device subjected to a constant voltage stress test. In this case, small fluctuations in the current passing through the dielectric is first observed followed by a surge in current indicating a hard thermal breakdown [11].

Previous methodologies adopted for detecting breakdown in standard reliability tests are no longer effective, necessitating a revision to the standard test procedures. A better methodology for detecting breakdown monitors an increase in current noise (defined as the variance of a defined number of consecutive current measurements). The current noise has been observed to increase by over four orders of magnitude while the measured current has only increased by 10%. NIST chairs the Working Group in JEDEC responsible for developing new test procedures that will eventually incorporate detection algorithms based on current noise.

Advanced Gate Dielectric Materials

The continual shrinking of MOSFETs requires the scaling of the SiO_2 dielectric thickness to maintain a value of capacitance to keep device drive current at an acceptable level and to eliminate undesirable short

channel effects. As the gate dielectric thickness is thinned, the tunneling current will approach a level that will preclude the use of SiO_2 as the gate dielectric.

Intensive research is underway to develop a suitable replacement gate dielectric or stack of dielectrics with a high permittivity (κ). The major challenges in developing such a gate dielectric include thermodynamic stability with Si, poor interfacial properties, and process integration issues. New analysis technique and test methodologies are being studied to characterize dielectric systems that include several interfaces. The reliability and wear-out mechanisms of advanced gate dielectric materials have not been adequately studied or characterized.

The NIST program includes developing standards, measurements, and models to increase the fundamental understanding of optical and electrical characterization of advanced gate dielectric materials. Figure 7 shows an example of a techniques being developed at NIST that allows the characterization of interfacial defects at multiple interfaces in a stacked gate dielectric using the charge pumping technique (technique used to measure a current which is proportional to the number of interfacial defects) [12]. The figure shows the magnitude of the charge pumping current for three interfaces in a three-layer gate stack. Such measurements techniques will be critical in the development of advanced gate dielectric materials.

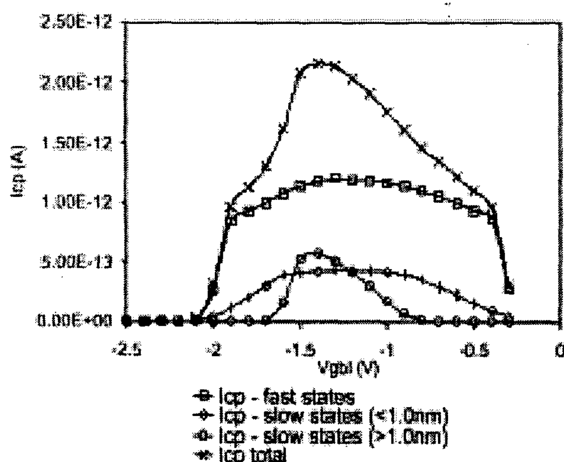

Figure 7: Charge pumping current shown as a function of gate bias for a three layer gate stack system. The magnitude of each curve represents the number of interfacial defects at each interface.

Conclusions

The reliability of the SiO_2 gate dielectric is becoming a critical concern as the oxide thickness is continually scaled down in advanced microelectronic technologies. Understanding the physical mechanism of breakdown is crucial when extrapolating product life from accelerated stress tests. NIST has played a key role in conducting experiments to validate the physical models of dielectric breakdown.

For devices with ultra-thin gate oxides, soft breakdown becomes a dominant failure mode and makes breakdown detection very difficult. Failure detection algorithms in accelerated breakdown tests must be modified for ultra-thin dielectrics. In collaboration with national standard organizations like JEDEC and ASTM, NIST is developing new detection techniques based on current or voltage noise.

The development of a new generation of advanced gate dielectric materials presents new metrology challenges for electrical and reliability characterization.

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