

Research on High-Frequency Asymmetric Pulse Power Supply of Current Source

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Abstract—In order to meet the requirements of the surface treatment of material, in this paper the 50kHz asymmetrical pulse power supply of current source is developed. The power supply adopts a two-stage construction. The front stage, in which current closed-loop control is employed, is high-frequency isolated DC/DC converter. The latter stage, on the contrary, is non-isolated asymmetric high-frequency pulse generator and uses open-loop control. After analyzing the topological principle, the important effect of the methods of series LC filter in the front stage is discussed. The 1kW experimental prototype is built and relevant experiments are carried out. Theoretical analysis and experimental results show that the circuit can meet the requirements of the surface treatment of material, and the circuit has the advantages of simple structure, easy control and low cost.

Keywords- current source; asymmetric pulse power supply; high-frequency switching-mode power supply

I. INTRODUCTION

Pulse power supply, especially the asymmetric pulse power in which a small amplitude negative pulse is superposed on a positive forward pulse, is widely used in all kinds of material surface treatment equipment. This paper studies a new high-frequency asymmetric pulse power of current source that adopts a two-stage structure. The front stage, a high-frequency DC/DC converter of constant-current control, is used to realize positive pulse amplitude adjustment. The latter stage is an asymmetric pulse converter of which the frequency varies from 20 kHz to 50 kHz and the duty cycle ranges from 10% to 80%. Under the circumstances of the load of resistive and inductive load, the output is the asymmetric voltage pulse. The pulse amplitude can change along of the load, which is very suitable for the requirements of surface treatment technology

of materials like magnetron sputtering and so on. After analyzing the topological principle, an experimental prototype was built. Based on the theoretical analysis and experimental results, it is concluded that the circuit can meet the requirements of the surface treatment of material, and the converter has a good application prospect.

II. THE HIGH-FREQUENCY ASYMMETRIC PULSE POWER OF CURRENT SOURCE

In order to reduce the volume and cost of power, and improve its efficiency of power supply, two-stage structure is used, the front stage is DC/DC high-frequency converter and the latter stage is asymmetric pulse converter. Below is an overall block diagram of the converter^[1]:

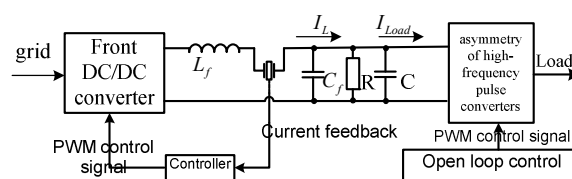


Figure 1. Overall block diagram of the high-frequency asymmetric pulse power of current source

Adding a capacitor C and a large resistor R to the latter stage's input portions, the asymmetric pulse amplitude can be controlled by regulating the frequency and duty cycle of the latter stage. Generally, the capacitor is a small high-frequency no-sense capacitor. The high-frequency components of the input current can be filtered so that the output pulse will be smooth. The large resistor R can offer protection when the load is light. The current of the large resistor R is about 10% of the minimum current output of the power. The output filter

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of front stage is $L_f C_f$ series filter. Since C_f is usually an electrolytic capacitor, the low-frequency components of the input current of the latter stage can be filtered. Also, due to the filtering inductor, the influence which the latter stage input has on the front stage output will be reduced. The inductance is shown as follow^[2]:

$$L_f = \frac{V_{o\max} T_{off}}{I_{Lf\max}} = \frac{V_{o\max} T_{off}}{2I_{o\min}} \quad (1)$$

$V_{o\max}$ is the maximum output dc voltage of front stage circuit, T_{off} is the cut-off time of rectifier diode and $I_{o\min}$ is the minimum output dc current of front stage circuit. Considering the output voltage ripple, the capacitance is like follow^[3]:

$$C_f = \frac{V_{o\max}(1-D)T_s^2}{8L_f\Delta V_o} \quad (2)$$

D is the output duty cycle of DC-DC circuit, T_s is the switching cycles, and ΔV_o is the peak voltage of output voltage.

Figure 2 shows the traditional two-way asymmetric pulse circuit topology. By changing the output of voltage source V_1 in figure 2^[4], the positive pulse amplitude can be changed,

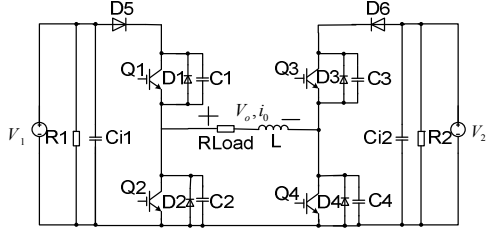


Figure 2. Traditional two-way asymmetric pulse circuit topology

In the same way, the negative pulse amplitude can be changed by changing the output of voltage source V_2 . The voltage of load is V_1 , when the switch device Q_1 and Q_4 is on. The voltage of load is V_2 , when the switch device Q_3 and Q_2 is on. Since this topology requires two sets of voltage source, the cost and complexity of the power is high. This paper studies a new high-frequency asymmetric pulse power circuit topology^[5], the load is resistance and inductance load. Compared to the common full bridge topology, this topology reduces a switch (Q_2). In figure 3(a), I_{in} is an ideal current source, R is a false load and C is a filter capacitor. Using complementary PWM control mode. Q_1 and Q_4 are open at the same time, while Q_3 and Q_1 , Q_4 are opened complementary.

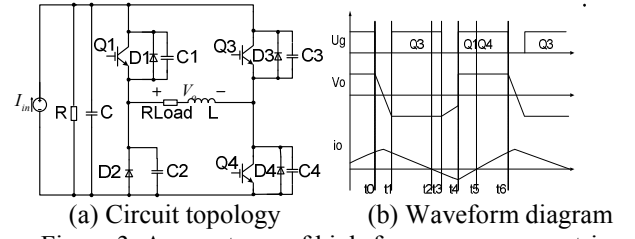


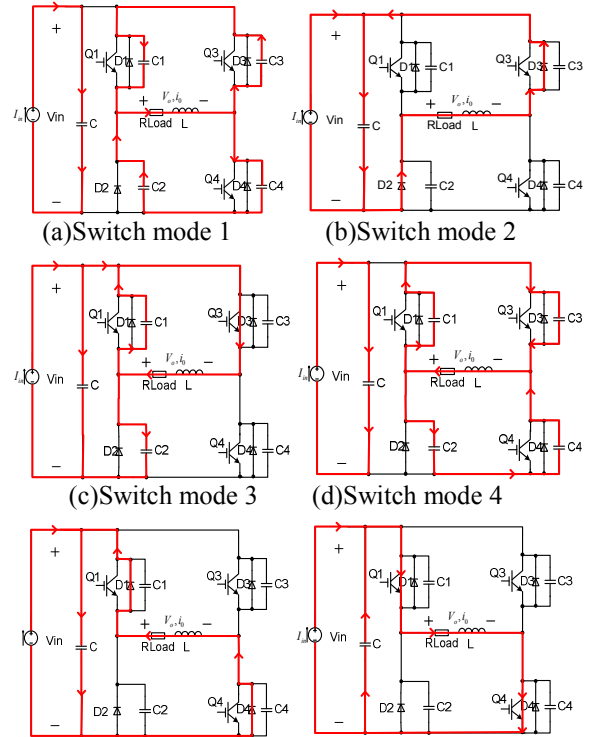
Figure 3. A new type of high-frequency asymmetric pulse power circuit topology and waveform diagram

In figure 3(b), u_g is switch device drive waveform, V_o is load voltage waveform and i_o is load current waveform. The following assumptions are made:

- (1) All switch devices and diodes are ideal device.
- (2) All the capacitors and resistors are ideal device, besides the values of capacitance and resistance are large enough to reduce the value of the current flowing through the resistance. At the same time, capacitor voltage is the constant V_{in} .

$$(3) C_1 = C_3 = C_4 = \frac{4}{3}C_{oss}$$

Converter has six working modes in one cycle. Switch mode 1: Q_1 and Q_4 are in the on-state till t_0 . $V_o = V_{in}$, $i_o = i_{L\max}$, $u_{C1} = u_{C4} = 0$, and $u_{C2} = u_{C3} = V_{in}$. At t_0 , Q_1 and Q_4 are off. Because L is large enough, $i_o = i_{L\max}$. Under the constant-current i_o , capacitor C_4 and C_1 are charged while capacitance C_2 and C_3 are discharged.



(e) Switch Mode5 (f) Switch Mode6

Figure 4. Equivalent circuit of converter in various modes

Switch mode 2: when $t = t_1$, C_1 and C_4 is charged to V_{in} , C_2 and C_3 is discharged to zero, the output voltage is $V_o = -V_{in}$ and $u_{g3} > 0$. After loading the inductor freewheeling, switching tube Q_3 does not conduct, while diode D_2 and D_3 do. The equivalent circuit is shown in Figure 4(b).

Switch mode 3: when $t = t_2$, $i_o = 0$ and switching tube Q_3 zero-voltage is on. C_1 is discharged, C_2 is charged and $u_{c2} = 0$.

Switch mode 4: when $t = t_3$, switching tube Q_3 is off, and the inductor current approximately reached the minimum value i_{Lmin} , $i_o = i_{Lmin}$. C_2 and C_3 are charged with nearly constant current i_{Lmin} while C_1 and C_4 are discharged. Equivalent circuit is demonstrated in Figure 4(d).

Switch mode 5 : when $t = t_4$, C_2 and C_3 are charged to V_{in} , C_1 and C_4 are discharged to zero, the output voltage $V_o = V_{in}$, $u_{g1} > 0$ and $u_{g4} > 0$. After loading the inductor freewheeling, switching tube Q_1 and Q_4 are off and the body diode D_1 and D_4 are on, The equivalent circuit is shown in Figure 4(e).

Switch mode 6: when $t = t_5$, load current is zero and switching tube Q_1 and Q_4 Zero-voltage is on. The equivalent circuit is shown in Figure 4(f). When $t = t_6$, switching tube Q_1 and Q_4 shutdown, coming back to modal 1 and it has come to the end of a work cycle

By the analyzing, during the switching Q_1 and Q_4 turn-off time, capacitor C_4 and C_1 are charged under the constant-current i_o , whereas capacitor C_2 and C_3 are discharged. And if the capacitor is large enough, there is still a certain voltage V_{c2} when discharge process is finished. As Q_3 conducts, the voltage of the load is $V_{in} - V_{c2}$ and the converter can output amplitude asymmetric negative pulse. The key is the selection of capacitor. In order to output amplitude asymmetric negative pulse, the selection of capacitor should make the resonant frequency f_0 less than pulse switching frequency f . The selection formula of capacitor is :

$$f > f_0 = \frac{1}{2\pi\sqrt{LC_2}} \quad (3)$$

If $f > f_0$, which means that capacitor C is very large in the case of constant inductor L , then when tube Q_3 is open, the voltage of C_2 is V_{in} and negative pulse output is zero. Otherwise, C_2 is very small. And when tube Q_3 is open, the voltage of C_2 is zero. Diode D_2 conducts and negative pulse output reaches maximum V_{in} .

III. POWER CONTROL THEORY

The later stage employs open-loop control, the front stage of DC/DC converter must be closed-loop control in order to make the input of the later stage stable. In this way the output voltage amplitude can be adjusted as required. Concerning the DC/DC converter, high-frequency asymmetric pulse converter is a special non-linear load. It directly affects the front stage DC/DC converter property. And it further affects the output results of the later stage converter. The high-frequency asymmetric pulse power of current source block diagram is shown in Figure 1.

In a cycle of the later stage converter, when the switching device is turned off, capacitor C is charged with the constant current I_L . When the later stage switching device is turned on, capacitor C is discharged to the load. At this time the load current is equal to the sum of the DC/DC converter constant current output I_L and the capacitor discharge current. During a cycle, the average current through the capacitor should be zero. If the average current consumed by the false load R is ignored, the average current I_{Load} of flowing through the load is equal to the front stage DC/DC constant output current I_L . Therefore, the later stage load current can be constant by keeping the front stage's output current constant. Therefore, as long as the front stage current is constant, the average current flowing through the load will not change. However the voltage of the capacitor will change with the duty cycle of the later stage converter. The greater the duty cycle, the shorter the capacitor's charging time. Also, the discharge time will be longer and as a result, the capacitor voltage will be lower; on the contrary, the smaller the duty cycle, the longer the charging time for the capacitor, the shorter the discharge time and the higher the capacitor voltage.

IV. EXPERIMENT RESULTS AND ANALYSIS

A 1kW experimental prototype of which the pulse frequency is 20 kHz~50 kHz was built to verify the circuit principle. The DC/DC converter of the front stage is the current model and the current can be regulated from 0.3A to 1A. Filtering inductor $L_f = 8mH$. capacitor $C_f = 10\mu F$, the false load $R = 10k\Omega$ and the filter capacitor is the high-frequency with no-sense capacitance

$C_f = 1\mu F$. Switch device FGA25N120ANTD is used in the later stage. $C_1 = C_3 = C_4 = 1nF$. $C_2 = 10nF$. Diode DSEI12-12A is used and switch frequency is 50 kHz. Dead time is $1\mu s$. Resistance and inductance load are adopted, of which the value is 50Ω and $1.55mH$ respectively. UC3843 and UC3715 are used to make the open loop control in the later stage. Figure 5 and Figure 6 are the voltage and current waveforms of the load. The duty cycle is 10% in Figure 5 while it is 80% in Figure 6.

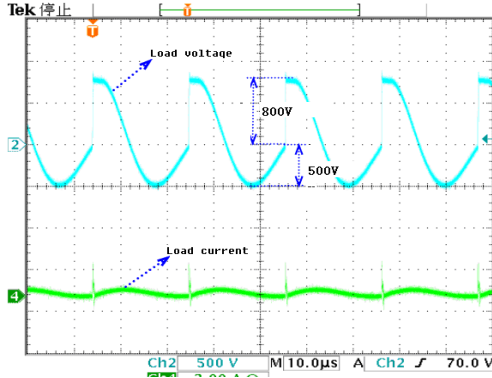


Figure 5. Voltage and current waveforms, the duty cycle is 10%

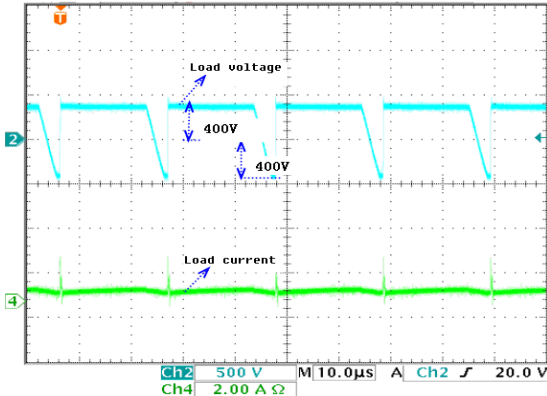


Figure 6. Voltage and current waveforms, the duty cycle is 80%

By the figure, voltage amplitude of the load is very stable and it meets the control requirements. Experimental waveforms are almost the same with theoretical analysis waveforms. The positive and negative amplitude of output voltage can be adjusted and the pulse duty cycle can also be adjusted in a certain range. The circuit can meet the requirements of high-frequency asymmetric pulse power.

V. CONCLUSION

This paper has presented a kind of new high-frequency asymmetric pulse power current source topology and its control method. Both positive and negative asymmetric pulse voltage can be produced and the amplitude of the pulse can be adjusted. While the duty cycle of the positive pulses can be adjusted from 10% to 80%, the frequency of the pulse ranges from 20 kHz to 50 kHz. Theoretical analysis has been validated by the experiment results. The topology, which has the advantages of simple structure, easy to control and low cost, is considered to be suitable for the surface treatment of material.

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