

SNS Programmable Voltage Standard

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Abstract — Superconductor-Normal-Superconductor (SNS) junctions have been used in the design and fabrication of a 1-V rapidly programmable voltage standard. The superconducting circuit is a series array of 32 768 Nb-PdAu-Nb junctions with taps that divide the array into a binary sequence of smaller array segments with a minimum segment size of 128 junctions. The 16-GHz drive frequency is set by the characteristic frequency of the junctions. A computer-controlled 8-channel bias system controls the current in each segment and allows the rapid selection of any one of 513 discrete voltage levels. The system is designed for fast dc measurements and the synthesis of precise ac waveforms.

I. INTRODUCTION

This paper describes a programmable Josephson voltage standard (JVS) in which the output voltage $V = N f / K_J$ is defined by digitally programming the step number N [1]. Here f is the applied microwave reference frequency and $K_J = 2e/h = 483597.9 \text{ GHz/V}$ is the Josephson constant. In a programmable JVS, an array of nonhysteretic junctions is divided into a binary sequence of array segments, as shown in Fig. 1a. The microwave excitation for each junction is set to equalize the amplitude of the $n=0$ and $n=1$ steps, as shown in Fig. 1b. Each segment of the array can be set to the $n=-1$, 0, or $+1$ step by applying a bias current ($-I_s$, 0, $+I_s$) at the appropriate nodes. The combined step number N for the whole array can thus be set to any integer value between $-M$ and $+M$, where M is the total number of junctions in the array [1].

The rapid settling time and inherent step stability of the JVS in Fig. 1 make it potentially superior to a conventional zero-bias JVS for dc measurements. (We define a dc measurement to be one in which the transient associated with changing N can be excluded from the measurement.) Such measurements include calibration of dc reference standards and digital voltmeters, and the characterization of A/D and D/A converters. The circuit of Fig. 1 can also be used to generate a staircase approximation to a sine wave by selecting appropriate step numbers in rapid succession. The resulting waveform has a computable rms value and can be used as an accurate source of ac voltage. Present standards for ac voltage are based on devices that compare the heating effect

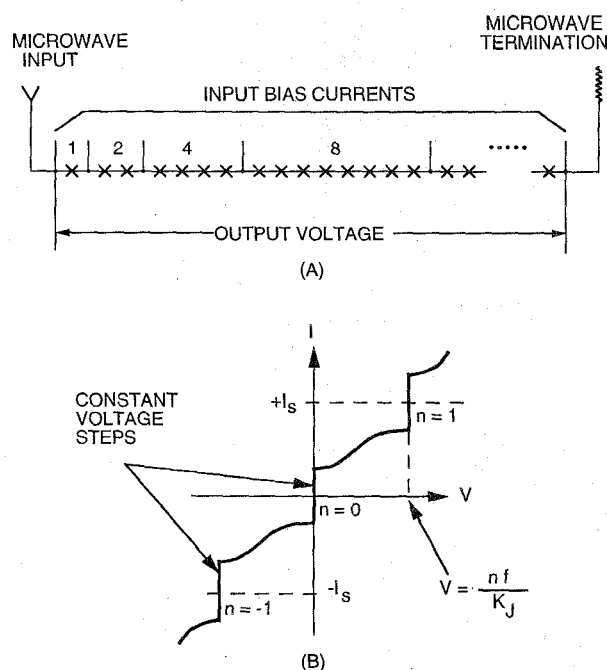


Fig. 1(A) A schematic circuit for a programmable voltage standard and (B) the I - V curve for a single junction of the array.

of ac and dc voltages. The programmable Josephson voltage standard provides the first direct and independent check of the ac/dc difference of these thermal voltage converters.

II. SNS JUNCTIONS

Theoretical analyses [2]-[4] have shown that the best combination of bias margin, stability, and microwave drive power for a programmable JVS is achieved when the step voltage f/K_J is approximately equal to $I_c R_N$, where I_c is the junction critical current and R_N is the normal state resistance of the junction. Noise immunity also demands that I_c be as large as possible. These two requirements suggest the use of Superconductor-Normal-Superconductor (SNS) junctions because their $I_c R_N$ products of 5-30 μV lead to a convenient operating frequency of 2.5-15 GHz. It has also been shown that SNS junctions maintain the desired nonhysteretic I - V curve for values of I_c up to 10 mA. The critical current of SNS junctions is limited only by the microwave power that is required to induce the constant voltage steps and/or heating effects. Step amplitudes of several milliamperes are easily achieved in typical 2.5 μm diameter junctions. Large critical

Manuscript received August 26, 1996.

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This work was supported in part by the US Army as CCG Project 346.

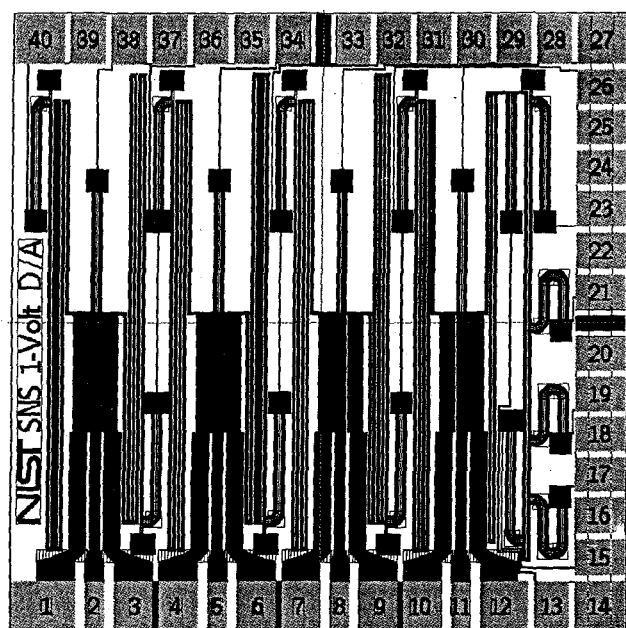
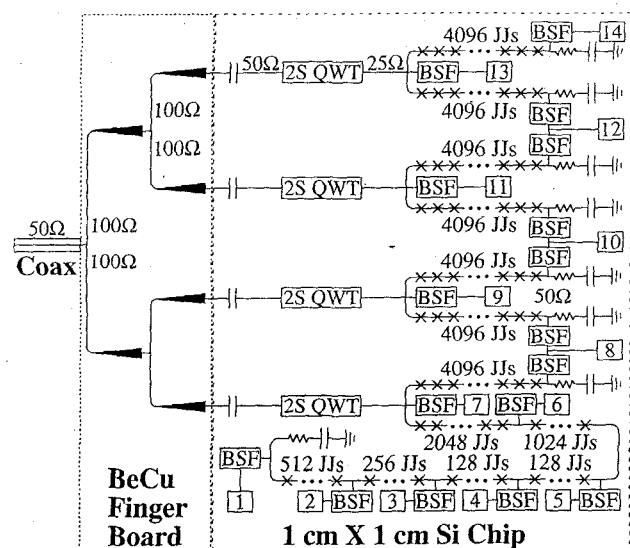


Fig. 2(A) The circuit of a 32 768 junction programmable array and (B) the physical layout of the circuit.

currents are essential to achieve the noise immunity that is required when the array has wide-bandwidth connections to room temperature devices. For this reason, the SNS junction geometry is the preferred design for programmable voltage standards.

Fig. 2a is a schematic of a programmable JVS chip with 32 768 SNS junctions and Fig. 2b shows the physical layout of the chip. The 16 GHz drive power is transmitted into the Dewar on a 50 Ω semirigid coaxial cable. At the termination of the cable it is launched into a coplanar waveguide network that is etched onto a 2 x 8 cm BeCu-clad FR-4 printed circuit board. Two tees and six tapers divide the signal into 4 identical 50 Ω feeds. The ends of the BeCu coplanar strips form spring fingers that contact matching pads (numbers 1-12) on the chip. At each feed on the chip a two-stage

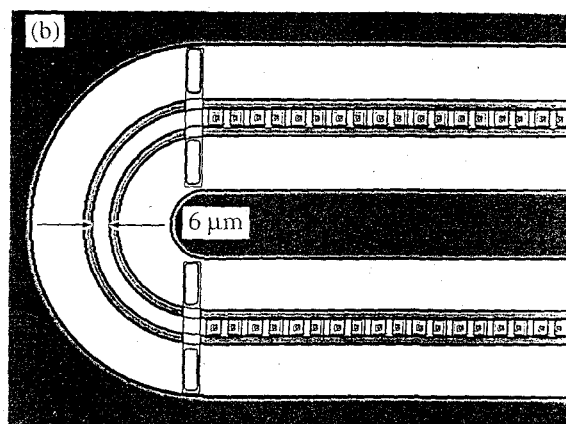


Fig. 3. A section of coplanar line showing the distribution of junctions along the center conductor.

quarter-wave transformer (2SQWT) again divides the signal so that all together there are eight 50 Ω feeds into 8 array segments of 4096 junctions each [5]. The junctions are arranged in series along the center conductor of the coplanar waveguide, as shown in Fig. 3. With a normal-state resistance of only about 0.004 Ω , the junctions are a very minor perturbation on the line. In contrast to the more typical stripline designs, the coplanar design eliminates two fabrication levels. Also, because of the larger ratio of line impedance to junction resistance, it is possible to maintain the required rf power uniformity through a larger number of junctions. Power uniformity also requires that the dc taps on the array cannot create reflections that would lead to standing waves. Each dc tap therefore includes a bandstop filter (BSF) at the 16 GHz design frequency. These filters are made with a quarterwave section of 85 Ω coplanar line terminated by a 10 pF capacitor. The capacitors are the square elements shown in Fig. 2b. At 16 GHz the capacitor looks like a short so that the quarter-wave section appears open where it contacts the junction array. One of the eight 4096 junction array segments is further divided into segments of 2048, 1024, 512, 256, 128, and 128 junctions. The size of the bandstop filters prevents continuing the division all the way down to a single junction. This limitation can be eliminated with a larger chip or a more compact design. Each of the eight 4096-junction array segments is terminated with a 50 Ω resistor and a 10 pF capacitor to ground.

III. BIAS CIRCUIT DESIGN

The bias circuit of Fig. 4 has been developed for evaluating and optimizing the performance of programmable Josephson arrays. Under the control of the system computer it can individually measure the I - V curve of each array segment to confirm functionality and to select the optimum bias points for the -1 and +1 steps. With the optimum bias current values latched into the D/A converters, any specified dc value Nf/K_j is generated by setting the analog switches to bias the appropriate array segments into the +1, 0, or -1

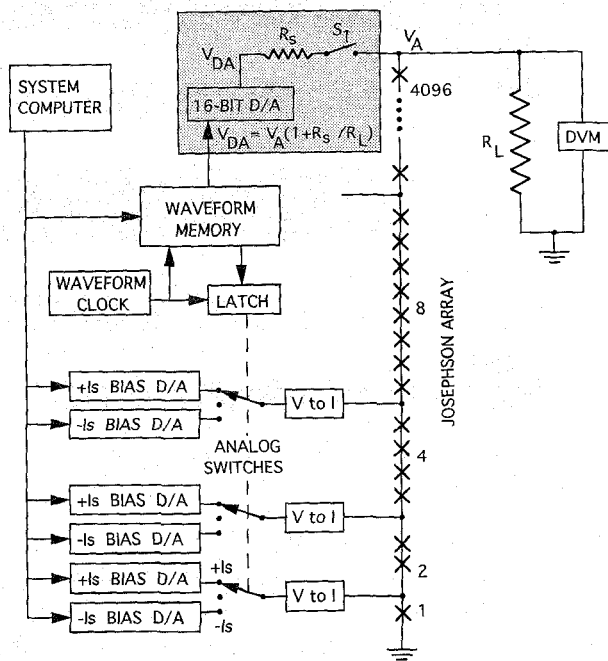


Fig. 4 A block diagram of the bias system used to control the programmable voltage standard.

states. To synthesize an ac waveform, the computer loads the waveform memory with the required state $(-1, 0, +1)$ of each array segment for up to 65 536 time steps of the specified waveform. When the waveform clock is started, the memory steps through the time sequence and its outputs drive the analog switches that select the bias appropriate to the -1 , 0 , or $+1$ steps for each array segment. The outputs of the analog switches control fast constant-current drivers for the array bias lines. A latch on the digital inputs to the analog switches ensures that all switches change state within a few nanoseconds. The settling time of the bias-current drivers is 400 ns.

The voltage across the Josephson array is accurately controlled only if the bias point for each junction remains within the bounds of the constant-voltage step. Thus the load current is limited to about half of the step width, or about 10-1000 μA , depending on the junction technology used. This output current may be inadequate for applications such as the measurement of the ac/dc difference of thermal voltage converters. When switch S_1 is closed, the 16-bit D/A converter in the shaded portion of Fig. 4 can provide a substantial amplification of the available output current. This increased output capacity results because the D/A converter is programmed to provide the predicted load current and the Josephson array need only supply the difference from the predicted value. If the prediction is accurate to 1%, then the circuit can multiply the available output current by a factor of 100.

When the programmable Josephson array is used to synthesize a sine wave, the transient associated with step transitions is included in the rms value and may lead to an

unacceptably large uncertainty. If R_s is of order 1-10 Ω , then the shaded circuit will also suppress the transients that occur when the Josephson array switches between steps. Consider the transition from $N=127$ to $N=128$. In this case six array segments with a total of 127 junctions will make a transition from 1 to 0 and one segment with 128 junctions will make a transition from 0 to 1. For the worst-case timing error with S_1 open, the voltage during the transition could be as small as 0 or as large as $255 f/K_J$. With S_1 closed however, the array voltage is clamped to within about 0.1% of the D/A converter output while the array settles to the new step voltage. Thus the load voltage is controlled by the array between transitions and by the 16-bit D/A converter during transitions. State-of-the-art 16-bit D/A converters are capable of reducing the transient to about 60 pV s. Assuming the worst case in which all of the transient errors add constructively, the resulting RMS error in a 1 V, 60 Hz sine wave approximation with 256 transitions would be about 1 part in 10^6 (1 ppm).

IV. EXPERIMENTAL RESULTS

The SNS junctions that we use have a palladium-gold barrier for which the $I_c R_N$ product is typically 5-30 μV [6]. Using the condition that $f/K_J \approx I_c R$ as described above leads to an optimum drive frequency near 8 GHz. The arrays work nearly as well at frequencies up to 16 GHz so we use this higher frequency to increase the output voltage range. At 16 GHz, the step separation is approximately 33 μV , and 30 000 junctions are required to reach 1 V. Fortunately the SNS junction fabrication process yields large arrays of highly uniform 2.5 μm diameter junctions with critical currents near 5 mA [5]. With such high critical current density (200 000 A/cm²) and the corresponding high bias currents, we have encountered difficulty with breakdown of wiring contacts in the circuit. Also, for $I_c > 5$ mA, the rf power dissipated in each junction ($P \approx I_c f / K_J$) leads to excessive chip heating for very large arrays [3]. Figure 5 shows I - V curves of the segments 512, 1024, 2048, 4096, and all 8192 junctions of an 8-segment SNS junction array operated at 11 GHz. (The maximum voltage is 186 mV.) The $n=-1$, 0 , and $+1$ steps are all larger than 1 mA and occur over identical bias current ranges for every segment. This precise matching of the I - V curves of thousands of junctions is one of the critical requirements of a programmable array.

An important goal of this circuit is the direct measurement of the ac/dc difference of a thermal voltage converter (TVC). Since the array can be programmed to generate either ac or dc, this measurement can be made without switching between sources. A variety of difficulties including junction yield, flux trapping, and circuit contact breakdown has limited these measurements to an array of 4096 junctions operating at 13.2 GHz to generate a maximum voltage near 0.1 V. The transient suppression circuit of Fig. 4 is designed to minimize transients at the load, but, because of delay and mismatch in

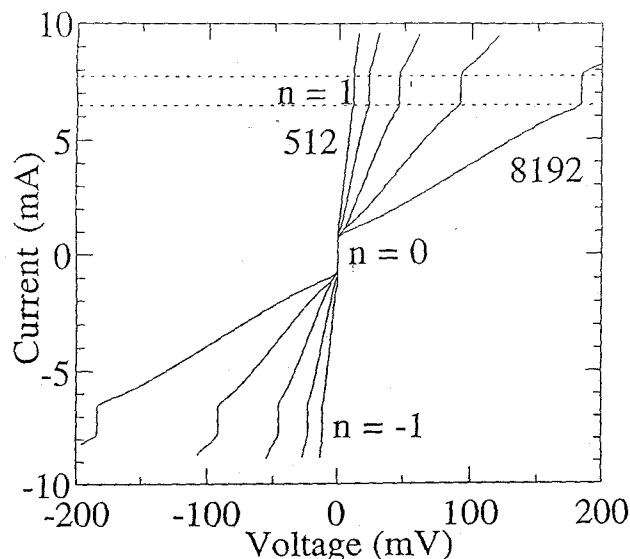


Fig. 5 Experimental I-V curves for arrays of 512, 1024, 2048, 4196, and 8192 junctions. The applied microwave power is the same for all five curves.

the transmission line to the Josephson array, this circuit can generate flux-trapping current spikes at the array. Since our present devices are susceptible to flux trapping, it was necessary to disconnect the transient suppression circuit and to increase the bias current risetime. In the best result to date we compared the output of a 100 Ω multijunction thermal converter (E_{ac} or E_{dc}) for a 112 mV dc input, a -112 mV dc input and a ± 112 mV, 50 Hz square-wave input. We compute E_{dc} as the average of the +dc and -dc measurements that are symmetrically positioned around an ac measurement. This particular TVC generates only about 96 μ V for a 112 mV input, so 387 measurements were averaged to obtain a small uncertainty for the ac/dc difference. Assuming a square-law response ($n=2$) we find the ac/dc difference $\delta = (E_{ac} - E_{dc}) / n E_{dc} = -18$ ppm with a standard deviation of the mean of ± 2 ppm. Most of this difference can be explained by the risetime transient of the square wave signal. To estimate this correction we made an accurate oscillograph of the transient and numerically computed its RMS contribution relative to a perfect square wave. The resulting correction is -22 ± 5 ppm. Thus, with the correction, we have $\delta = 4 \pm 7$ ppm. This is consistent with previous calculations of δ based on detailed modeling of the known sources of ac/dc difference. The uncertainty in this measurement needs to be improved by about an order of magnitude to match the state-of-the-art for other indirect

methods of measuring δ . This can be achieved with larger arrays that can generate voltages above 1 V.

V. CONCLUSION

The feasibility of programmable Josephson voltage standards for fast dc measurements and waveform synthesis has been demonstrated. A new SNS junction technology is being developed to make high critical current, self-shunted junctions, that have the noise immunity, $I_c R_N$ product, and output drive capability that are required to achieve practical waveform synthesis. Present devices are limited by the fabrication technology to a maximum output voltage of about 300 mV and are susceptible to transient induced magnetic flux trapping. We expect the flux trapping problem to be solved by improving the critical currents of wiring films and contacts within the circuit. As the fabrication yield improves, output voltages of 1-10 V should be possible. Sine waves synthesized from a programmable Josephson array will bypass the usual thermal methods and provide an ac standard that is derived directly from the international realization of the volt. In the near term, it is likely that programmable Josephson voltage standards will find their greatest use in fast automated dc measurements and in ac measurements at low voltages or frequencies where the performance of thermal voltage converters declines.

ACKNOWLEDGMENT

The authors acknowledge many helpful discussions with R. L. Kautz.

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