Microwave Properties of Voltage-Tunable $YBa_2Cu_3O_{7-\delta}$ / $SrTiO_3$ Coplanar Waveguide Transmission Lines

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Abstract—**To explore the electrical characteristics of monolithic microwave circuits with integrated high-temperature superconductor and ferroelectric materials, we fabricated a series of coplanar waveguide transmission lines in laser-deposited $YBa_2Cu_3O_{7-\delta}$ and $SrTiO_3$ thin films. We characterized the voltage-tunable two-port microwave response of the transmission lines at cryogenic temperatures using a calibrated network analyzer system. Total phase shifts and phase tuning in these devices increased for increasing ferroelectric film thickness with only moderate increases in transmission loss.**

I. Introduction

Incorporating thin film ferroelectric materials with thin-film high-temperature superconductors (HTS) provides a means of producing low-loss, voltage-tunable monolithic microwave circuits with reduced length scales [1,2]. These tunable devices are useful in several communication applications such as phased-array antenna systems and frequency agile microwave radio transceivers [3-7]. Previous work [4-6] has demonstrated operational HTS-ferroelectric capacitors and delay lines that could be used in such functions and reported on the tunable properties of high-permittivity ferroelectrics such as thin film $SrTiO_3$. The signal losses and range of tuning in this class of devices depend on the placement and thickness of the thin film ferroelectric layers as well as their material parameters. Therefore, efficient device design requires optimized configurations and fabrication processes. Accurate microwave metrology of various device configurations is necessary to provide these design guidelines and can also verify emerging mathematical models [6,7] that predict multi-layer device performance.

The purpose of this work has been to fabricate low-loss, tunable coplanar waveguide (CPW) transmission lines of different geometries and thin-film configurations and, for the first time, to apply on-chip calibration to study the microwave properties of this class of device. This paper presents the fabrication process and specific microwave performance of $YBa_2Cu_3O_{7-\delta}$-$SrTiO_3$ (YBCO-STO) transmission lines and reports trends in microwave properties with changes in film placement, thickness, and planar geometry. The results clearly demonstrate that STO inclusion produces dramatic changes in phase velocities and allows tuning with only modest increases in transmission loss.

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II. Device Fabrication

This study used two coplanar waveguide transmission line designs as standard test devices. Both were 5 mm long, but of two different line widths. The photograph in Fig. 1 shows the top view of a completed chip of the wider line. Center conductor width (s) to gap size (w) ratios (see Fig. 2) were calculated to give a characteristic impedance (Z_0) of 50 Ω for infinitesimally thin conductors on a semi-infinite dielectric slab of $LaAlO_3$ (LAO) [8]. Since a voltage bias was to be placed between the center conductor and ground planes for the tuning measurements of HTS-ferroelectric devices, gap widths needed to be narrow enough to generate measurable tuning, but wide enough to limit signal losses. Line geometries of s = 53 μm, w = 100 μm and s = 26 μm, w = 50 μm were chosen as the compromise for the two CPW designs. These designs were then used to measure the influence of ferroelectric inclusion against the baseline response of the 50-Ω YBCO-LAO transmission lines; they were not designed to give optimal tuning and impedance matching for structures containing ferroelectric layers. The drawing in Fig. 2 defines the cross-sectional geometry for the two ferroelectric-superconductor arrangements investigated: F-S and S-F.

During testing, signal launchers made contact to gold pads at both ends of the chip. Since the launchers were much wider than the transmission lines, exponential tapers were included on the chips to provide smooth transitions between the two geometries. The dimensions at the launcher pads and along the taper were designed to present a constant 50-Ω impedance along the transitions of the YBCO-LAO test chips. A multiline

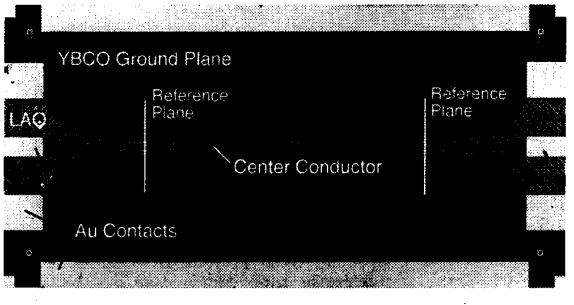

Fig. 1. Photograph of the YBCO coplanar waveguide test structure used in this study: length = 10 mm, width = 5 mm.

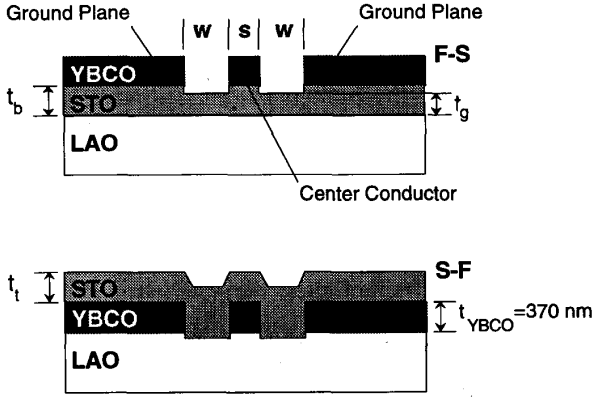

Fig. 2. Cross-sectional representation of two different thin film configurations with definitions of the geometrical parameters.

calibration described in the following section placed the electrical reference plane on the chip at the ends of these transitions, so the electrical parameters of just the straight section of transmission line were determined.

Test devices for each of the two CPW line widths were made in the two thin-film configurations depicted in Fig. 2. We fabricated one device of both film configurations with s = 53 μm and a series of F-S devices with varying STO thicknesses and s = 26 μm. The devices are listed in Table I, with values of the geometrical parameters defined in Fig. 2.

$YBa_2Cu_3O_{7-\delta}$ and $SrTiO_3$ thin film layers were deposited on 0.5-mm thick LAO substrates using pulsed-laser deposition (PLD) techniques previously reported [4]. The YBCO film thickness was nominally 370 nm for all devices. Critical temperatures ranged between 89-91 K, and surface resistance values measured with a dielectric-loaded cavity at 24.6 GHz and 76 K fell between 6-8 mΩ. This verifies that good film quality was maintained for all the structures examined here, even for the 370-nm YBCO film grown on 600 nm of STO.

The two film configurations were deposited in slightly different ways. For F-S bilayers, thin-film STO was deposited at a substrate temperature of 745 °C in an oxygen pressure of 53 Pa (400 mTorr) [9]. The substrate temperature and O_2 pressure were then raised to 762 °C and 80 Pa (600 mTorr) for YBCO growth. The films then cooled as the chamber was back-filled with O_2 to atmospheric pressure. For S-F devices, thin film superconductor was deposited on the substrate first, using the same YBCO deposition conditions as above. Devices were then fabricated in this layer. Afterwards, the films were placed in the PLD system and heated to 745 °C in 53 Pa (400 mTorr) flowing O_2 for deposition of the top STO layer. A shadow mask prevented STO growth on regions where contact metallization would later be deposited.

Patterning of the YBCO layer used standard photolithography and Ar ion-milling. Milling followed a timed sequence based on etching rates determined in separate control runs, which lead to some over-milling as seen later with profilometry (see Fig. 2 and the t_g values in Table I). Contact metallization was deposited on a photoresist lift-off pattern using electron-beam evaporation. The exposed YBCO first underwent a four-minute O_2 plasma cleaning in the electron-beam system. Without breaking vacuum, a 20-nm Ti adhesion layer was deposited directly onto the YBCO, followed by 130 nm of Au. After the lift-off, the chips were diced for testing. No packaging was required, since the chips were mounted in a spring-loaded test fixture.

III. Electrical Characterization

The coplanar waveguide devices were characterized in a cryogenic environment using an automated microwave test system. Devices were placed in brass chip carriers and loaded into a test fixture at the end of a cryogenic probe. The carriers supported the chips at the edges along the length, leaving an open volume 9 mm deep under the bottom surface of the substrate. A Be-Cu spring lifted the carrier and pressed the chip against the center conductor electrodes of the launchers. Two Be-Cu spring contacts provided ground connections at each launcher, and brass retaining clips along the chip edges provided additional low-impedance ground contacts. Semi-rigid coaxial cables ran from the test fixture stage to the top of the probe. For testing, the probe was inserted into a cryostat, and the top, which extended outside the cryostat, was connected to an automated network analyzer.

Just before each set of S-parameter measurements, we calibrated the microwave test system using a two-tier procedure. First, a room temperature SOLT (short-open-load-thru) calibration was conducted at the end of the cryogenic probe where the test fixture would normally be connected. Afterwards, a multiline TRL (thru-reflect-line) calibration was performed at 76 K using DEEMBED software [10] and YBCO on LAO cali-

TABLE I
SUMMARY OF YBCO/STO COPLANAR WAVEGUIDE DEVICE PARAMETERS

Device	t_t (nm)	t_b (nm)	t_g (nm)	s/w (μm/μm)	α^b (dB/mm)	$\varepsilon_{r\,eff}{}^b$	$-\Delta\phi^c$ (deg)	$\%v_p$
CPW0[a] —	—	—	—	53/100	0.014	12.4	—	—
CPW1 S-F	600	—	490	53/100	0.04	17.1	3.0	0.3
CPW2 F-S	—	600	—	53/100	0.36	19.7	1.9	0.2
CPW3 F-S	—	150	70	26/50	0.05	13.0	<0.5	0.06
CPW4 F-S	—	350	150	26/50	0.28	14.6	0.8	0.09
CPW5 F-S	—	500	380	26/50	0.12	18.3	4.0	0.42
CPW6 F-S	—	600	490	26/50	—	—	8.3	—

[a]YBCO on LAO
[b]At 10 GHz
[c]Maximum change in phase at T = 76 K, f = 18.5 GHz, and Bias = 39 V

bration standards. This TRL test set consisted of three coplanar waveguide transmission lines of different lengths (0, 1.68 and 5.00 mm) and two short-circuited lines (0 mm offset). The standard lines, with s = 53 μm and w = 100 μm, were fabricated from YBCO on LAO following the procedures described above. Each standard was loaded into the test fixture, cooled to 76 K in liquid nitrogen, and measured. During cooling and measurement, the cryogenic probe positioned the chips just above the liquid surface to maintain a low-permittivity surrounding. The DEEMBED software then acquired data, calculated the calibration factors, and loaded these factors into the network analyzer for subsequent measurements.

While calibrating the test system, DEEMBED also computed average electrical parameters of the calibration lines and a statistical figure of merit. These data showed that the TRL procedure provided a good calibration from 2 to 20 GHz, with significant improvements over a single SOLT calibration conducted at room temperature, and at the same time furnished baseline data on the lines without ferroelectric layers (CPW0 in Table I).

After the TRL calibration, test devices were loaded into the fixture and cooled to 76 K in the same manner used during calibration. Calibrated S_{21} magnitude and phase data from device CPW1 are shown in Fig. 3 as an example of the results obtained in this study. The attenuation constant (α) was determined by dividing the S_{21} magnitude by the length of the line (5 mm), and the effective relative permittivity ($\varepsilon_{r\,eff}$) was calculated by squaring the ratio of the CPW phase shift to the phase shift that would occur for wave propagation in vacuum ($\varepsilon_{r\,eff} = (\phi_{CPW}/\phi_{vac})^2$). Values for each of the devices measured are included in Table I. Ideally, a separate set of TRL calibration lines would have been fabricated for each of the different CPW configurations in order to minimize measurement uncertainty. Since this would have significantly increased the work required to examine the number of devices investigated here, all ferroelectric device data were collected using the YBCO-LAO lines with s = 53 μm.

Bias-dependent measurements of the devices were conducted in an uncalibrated mode at 18.5 GHz after the calibrated S-parameter measurements. This provided a means of acquiring high-resolution phase shift information for a device that had already been fully characterized. The bias from a high-voltage supply was applied to the center conductor of the test cables with the internal bias tees of the network analyzer, which limited the maximum applied voltage to 40 V.

Change in phase values ($\Delta\phi$) as a function of applied bias were collected in a systematic manner for voltages of both polarities. These experiments generated curves like those depicted in Fig. 4 for the bilayer device CPW6. Since the permittivity (ε_r) of STO decreases with applied voltage bias, the total phase shift also decreases with increasing voltage magnitude. The data recorded here represent the negative of the actual phase shift. The maximum $\Delta\phi$ at 18.5 GHz, 76 K, and 39 V, and the percent change in phase velocity that this represents are recorded in Table I.

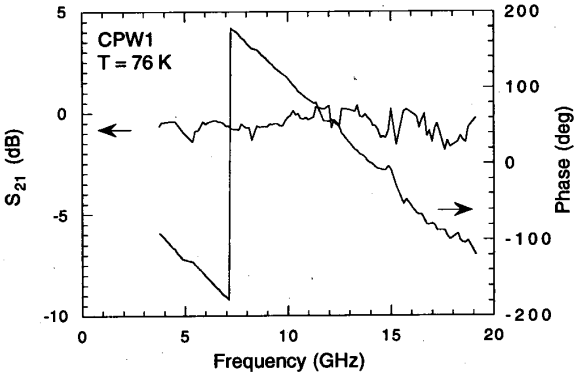

Fig. 3. Calibrated S_{21} data collected from the coplanar waveguide device CPW1.

IV. Discussion

The calibrated S-parameter results demonstrate that tunable devices with small microwave losses can be fabricated. Though a consistent trend is not observed in Table I, attenuation constants are generally larger in the devices with thicker ferroelectric layers. However, the addition of thin STO layers to YBCO coplanar waveguides increases signal attenuation only moderately over devices not containing ferroelectrics, even though the dielectric losses in bulk STO are known to be relatively large [11]. The attenuation constant of CPW1 is 0.04 dB/mm at 10 GHz, a modest increase over the value of 0.014 dB/mm obtained from the YBCO calibration lines (CPW0) when also considering the increase in electrical length.

Unlike signal attenuation, CPW phase velocity ($vp=c/\varepsilon_{r\,eff}^{1/2}$, where c is the speed of light in vacuum) decreased significantly with the inclusion of high-ε_r layers. Here $\varepsilon_{r\,eff}$ increases monotonically as a function of STO film thickness. For CPW2, the effective relative dielectric constant is 19.7, more than 50% larger than the value of 12.4 measured for the TRL calibration lines. The increase in $\varepsilon_{r\,eff}$ changed the characteristic impedance of the lines as well, producing return loss values as large as -12 dB in the frequency range 2-20 GHz. This emphasizes the need for empirical data and verified mathematical models to accurately design multi-layer ferroelectric devices.

Since the phase-frequency response of the CPW transmission lines is nearly linear and the signal attenuation is a weak function of frequency (Fig. 3), these devices perform as low-dispersion delay lines. Based on the data at 10 GHz, group delays range from 11.7 ps/mm for the lines not containing STO layers to 14.8 ps/mm for CPW2, and the signal loss per delay time for CPW1 is 2.9 dB/ns.

Through the addition of high-permittivity ferroelectric material, the delays in CPW transmission lines can be tuned. The amount of phase change indicates the tunability, which increases for thicker STO layers and narrower gap widths

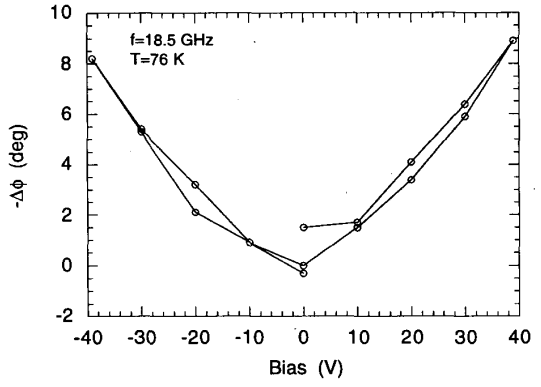

Fig. 4. Change in phase shift *vs.* applied bias for CPW6.

(Table I). While larger absolute phase shifts are obtained for thicker STO, the relative change in v_p also increases, particularly for the w=50 μm lines. The maximum phase shift in the 5 mm lines varies from less than 0.5° for CPW3 to as much as 8.3° for CPW6. Since the gap widths of the CPW transmission lines studied in this research are an order of magnitude larger than the coplanar capacitors presented in [4], narrower devices with correspondingly higher voltage tunability should be possible.

V. Conclusions

In summary, we have fabricated and characterized a series of ferroelectric-$YBa_2Cu_3O_{7-\delta}$ coplanar waveguide delay lines of various geometrical configurations and applied on-chip calibration measurements to this class of device for the first time. A key finding is that tunability increases rapidly with ferroelectric thickness, while the losses increase only moderately. We have made 5 mm long coplanar waveguide transmission lines with 8.3° phase tuning at 18.5 GHz and a 40 V bias, while maintaining small attenuation constants. Since the test devices used in this research were not optimized for tuning or impedance matching, even larger tuning with low transmission losses should be attainable.

The S_{21} responses from 2-20 GHz also reveal that HTS-ferroelectric transmission lines operate as broadband delay lines. Delay increases for thicker STO films and smaller CPW gap widths. These findings also identify trade-offs between characteristic impedance and tunability, since Z_0 is inversely related to $\varepsilon_{r\,eff}^{1/2}$.

This study has demonstrated that ferroelectric layers can be incorporated in HTS coplanar structures to provide a useful degree of tuning while controlling signal loss, and presented quantified trends in electrical properties useful as general guidelines for tunable device design and mathematical model verification. While ferroelectric layers provide voltage tuning in CPW devices, they also increase the total delay significantly, providing a means of miniaturizing microwave circuits with moderate increases in signal loss.

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