

## AUTOMATED JOSEPHSON INTEGRATED CIRCUIT TEST SYSTEM \*

C. J. Burroughs and C. A. Hamilton  
National Institute of Standards and Technology  
Division 814.03, Boulder, CO 80303

**Abstract**—We have developed an automated test system for complex superconductive integrated circuits. Its low speed capability consists of 96 identical I/O channels which are controlled by a PC-486 computer. Each channel is capable of driving currents and reading voltages at frequencies up to 40 kHz. Integrating this low speed I/O capability with high speed test equipment controlled over the IEEE 488 bus allows measurements at frequencies up to the limits of the test equipment. The system can automatically set biases, display I-V curves, measure parameter margins, plot threshold curves, extract experimental circuit values, and collect statistical data on parameter spreads and error rates. Issues of noise suppression, ground loop handling, and auto-calibration are discussed.

## I. INTRODUCTION

Testing a superconductive integrated circuit involves a hierarchy of ever more complex measurements beginning with simple I-V curves and ending with high speed functional tests and margin analysis. Two or four wire I-V measurements on test structures are typically used to compare values of critical current, resistance and inductance with target values. The device under test (DUT) is then checked for functionality at low speed and the input and power supply margins are determined. Finally, the DUT is tested at high speed. The system described in this paper is designed to perform all of these tests automatically.

As shown in Fig. 1, the system is controlled by a PC-486 computer and has separate low and high speed parts. Low speed tests are made using 96 identical I/O ports which operate at frequencies up to 40 kHz. High speed tests typically involve a digital sampling oscilloscope and various signal generators which are controlled over the IEEE bus. Since the hardware used in high speed tests is usually circuit dependent, this paper describes the low speed capability and its application to a wide range of circuits.

Automated testing of superconductive circuits is a challenge because these circuits operate with very low voltages and

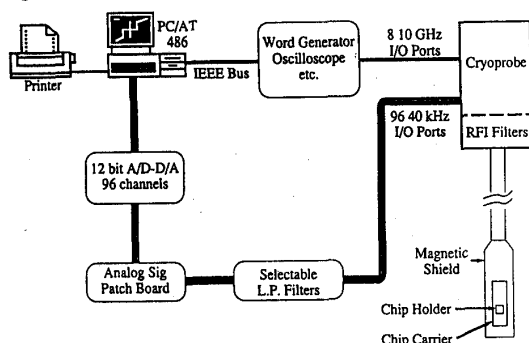


Fig. 1 A block diagram of the test system for Josephson integrated circuits.

Manuscript received August 24, 1992.

U.S. Government work not protected by U.S. copyright.

are therefore especially sensitive to noise. Protecting the superconductive circuit from the noise generated by the PC-486 controller requires careful shielding and grounding, and extensive use of RFI filters. Voltage drops across lead and ground resistance can cause significant errors in the circuit measurements. This paper will describe the hardware and software of the test system and explain how these issues are resolved.

## II. HARDWARE

A schematic of two I/O ports connected to a sample circuit is shown in Fig. 2. Each I/O port has a current driver and a voltage sensor. Josephson devices are inherently sensitive to electromagnetic interference. Without appropriate shielding and EMI filtering on the lines that connect to a circuit, that circuit may not function properly. The shielding and filtering requirement is met by enclosing the chip in an rf-tight compartment (the metal frame of the cryoprobe). Low speed lines penetrate this compartment by passing through screw-in EMI filters with a minimum attenuation of 38 dB above 10 MHz. Optional RC filters with a cutoff of 50 kHz can be added ahead of the cryoprobe filters when a lower cutoff frequency is required. We have found these additional filters to be essential in automated measurements of single flux quantum (SFQ) logic. With both filters in place, the test system is able to make I-V curve measurements with a noise level similar to that achieved with an analog oscilloscope. The cryoprobe used with the test system has 78 low speed lines and 8 high speed (10 GHz) lines. It is an advanced version of a design described previously [1]. Any connections to the unfiltered high speed lines must be well shielded and have a noise level below about 1  $\mu$ A.

The voltage sensor on each I/O port is a 12-bit differential A/D converter with its negative input tied to a common reference ground wire. This reference ground lead must be separate from the ground return path for the DUT input and power supply currents. Without this separation, voltage drops

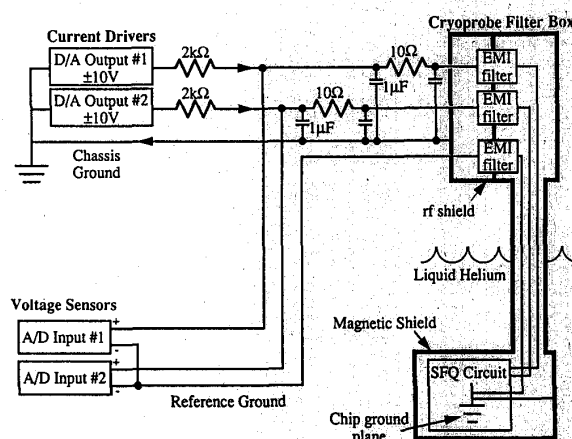


Fig. 2 Two ports of the test system connected to make a 4-wire I-V measurement of a single junction on the chip.

caused by the return currents lead to substantial errors in the voltage measurements. The two grounds are tied together only at the superconducting ground plane on the chip. The A/D input voltage range on each port is independently software selectable to  $\pm 10$  mV,  $\pm 20$  mV, or  $\pm 80$  mV. These correspond to LSB resolutions of  $\approx 5\mu\text{V}$ ,  $\approx 10\mu\text{V}$ , or  $\approx 40\mu\text{V}$  respectively. Programmable gain allows the system to have good resolution in low voltage (3 mV) measurements such as SFQ SQUID readouts and high voltage (1 V) measurements such as series array test structures.

The current driver on each I/O port is implemented with a 12-bit bipolar D/A converter with  $V_{\text{out}} = \pm 10$  V. A 2 k $\Omega$  resistor converts the D/A output to a current  $I_{\text{out}} \approx V_{\text{out}}/2$  k $\Omega$  with a range of  $\pm 5$  mA and an LSB of  $\approx 2.5\mu\text{A}$ . Since the voltages in Josephson circuits are typically no more than a few millivolts, the error in the current due to the load voltage is typically less than 1%. If a more accurate current measurement is required, we can read the voltage on the line and compute the current as  $I_{\text{out}} = (V_{\text{out}} - V_{\text{load}})/2\text{k}\Omega$ . Adjusting  $V_{\text{out}}$  to compensate implements a constant current source in software. The current return path for all D/A converters is through the probe frame and cable shields.

The filters and probe wiring add about 10  $\Omega$  to the current path. The effect of this resistance on both the output current and the measured voltage is compensated in software. The compensation constants are determined in a calibration mode in which every port is connected first to a voltage reference and then to a known impedance. When very high accuracy measurements are required (0.1%) separate I/O ports are used for the current drive and voltage measurement. Since the current return path and the voltage measurement ground point are separate this implements a 4-wire measurement.

The hardware just described allows I-V curves to be taken on every I/O port and I-I, I-V, and V-V curves to be obtained for any I/O port with respect to any other. All I/O ports can be used for either 2-wire measurements individually or 4-wire measurements in pairs. All voltage sensors and current drivers

can calibrate themselves to compensate for the series resistance of the probe and EMI filtering network.

### III. SOFTWARE

An important feature of the test system is the use of identical I/O ports for all connections to the chip. This standardizes the hardware for all tests and reduces all measurements to software algorithms. A software table assigns each drive current or voltage measurement to the appropriate I/O port. Repeating measurements, such as SQUID threshold curves, at many points in a circuit can be done by just changing the assignments in this table.

Figures 3-5 are displays of typical test system data for a 16-stage SFQ binary counter [2]. Each stage of this counter consists of a flip-flop SQUID coupled to a read SQUID. The critical current of the read SQUID indicates the flux state of the flip-flop SQUIDS. Figure 3 shows the I-V curves of all 16 read SQUID's. The 16 000 data points (1000 per I-V curve) are acquired in about one second. One can immediately see that stage 5 is shorted, stage 16 is open, stage 6 has excessive contact resistance, and stages 1, 4, 5, 12, and 13 are asymmetric indicating probable trapped flux. Figure 4 maps the overlap of the 0 and 1 flux state of the stage-1 flip-flop SQUID. The vertical axis is the current bias and the horizontal axis is the flux bias. The open squares indicate bias regions common to both the 0 and 1 flux states. Data like those in Fig. 4 for both positive and negative bias currents are used to extract all of the inductance and critical current parameters of the flip-flop SQUID. Figure 5 plots the current bias (vertical) and flux bias (horizontal) margins of stages 12-15. The open squares represent correct flip-flop operation and the numbers around the border code the mode of failure. Each of the approximately 125 trial points in these plots represents a sequence of more than 100 I/O commands.

The test system has also been used to confirm the operation and measure the margins of a large number of elements of the RSFQ logic family [3-4].

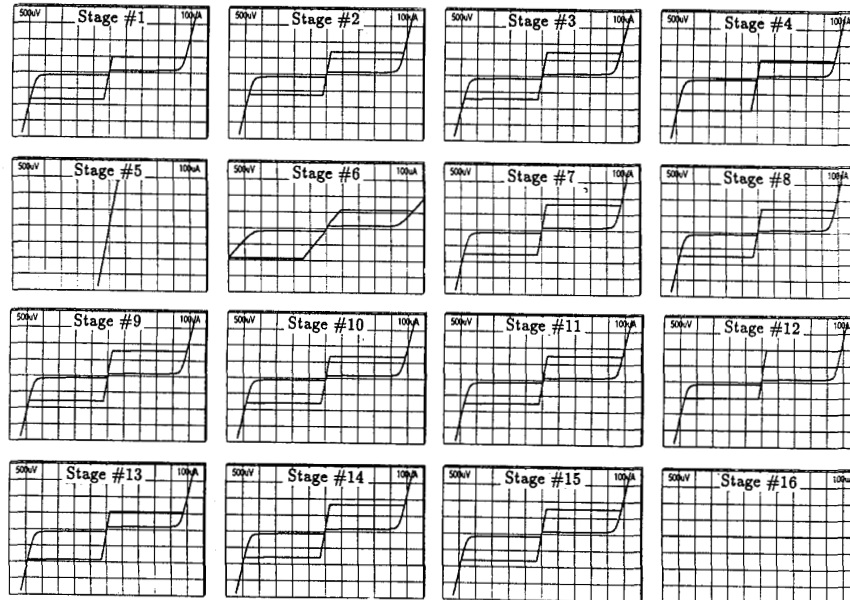


Fig. 3 Computer display of 16 I-V curves. The computer monitor can simultaneously display 16, 8, 4, or 1 oscilloscope-like graphic outputs.

## IV. SUMMARY

We have developed an automated test system for Josephson integrated circuits. It has 96 identical I/O ports which can simultaneously drive currents and measure voltages appropriate to Josephson circuits. All ports are bipolar with 12-bit resolution. Careful shielding, filtering of all I/O lines, and attention to ground return paths give the system noise and resolution comparable to traditional analog measurements. Automating the test process allows rapid and accurate functional tests, parameter extraction, and statistical analysis.

## REFERENCES

- [1] C.A. Hamilton, "High-Speed, Low-Crosstalk Chip Holder for Josephson Integrated Circuits," *IEEE Trans. Instrum. Meas.*, vol. IM-31, pp. 129-131, 1982.
- [2] C.A. Hamilton and Frances L. Lloyd, "100 GHz binary counter based on DC SQUID's," *IEEE Electron Dev. Lett.*, vol. EDL-3, pp. 335-338, 1982.
- [3] K. K. Likharev and V. K. Semenov, "RSFQ/Memory Family: A New Josephson Junction Technology for Sub Terahertz Clock-Frequency Digital Systems," *IEEE Trans. Appl. Supercon.*, vol. 1, pp. 3-28, 1991.
- [4] S. P. Benz, C. J. Burroughs, C. A. Hamilton, "Experimental results on single flux quantum logic," paper EM-8 submitted to this conference (ASC '92).

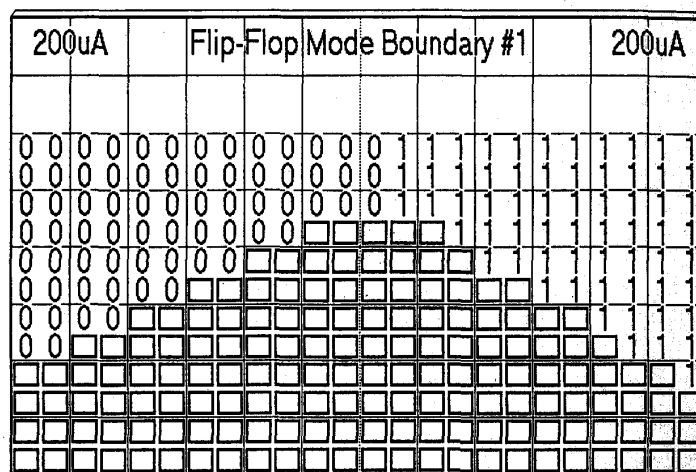


Fig. 4 A map showing the overlap of the 0 and 1 flux states of a SQUID flip-flop circuit.

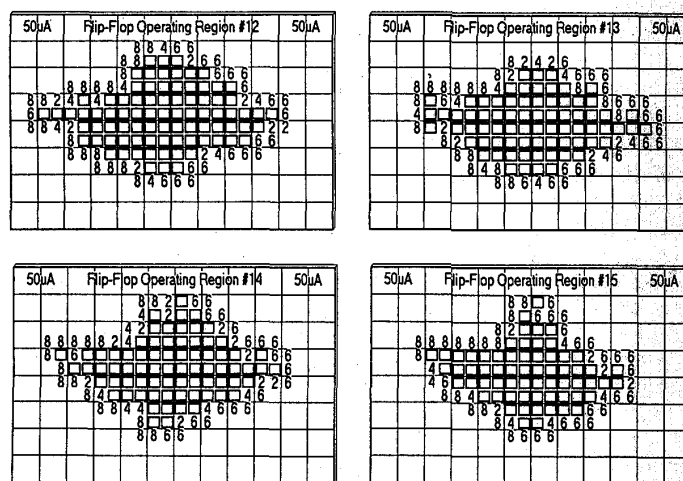


Fig. 5 A map of the current bias and flux bias operating margins of four stages of a single flux quantum binary counter.