

Analytical Voltage Dependence of an Unsaturated MESFET's Gate Capacitance

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Abstract—Using a one-dimensional gradual channel analysis we derive an analytical expression for the gate-source capacitance of an unsaturated MESFET as a function of the applied drain and gate voltages. Experimental measurements of the dependence of the gate-source capacitance on drain voltage show good agreement with theory when the device is biased below saturation. As the MESFET is biased into saturation the measured capacitance decreases with increasing drain voltage at a slightly faster rate than that predicted by the gradual channel theory due to high-field effects. These results show that the derived analytical expression may be useful for the analysis of the characteristics of MESFET's that are biased in the linear region.

I. INTRODUCTION

SCHOTTKY-barrier field-effect transistor (MESFET) technology is critically important for the development of high-speed GaAs digital and microwave integrated circuits. In order to facilitate circuit design, accurate device models and circuit simulation programs are necessary. A number of device simulators based on analytic MESFET models [1]–[4] have been reported; however, the dependence of the intrinsic gate-source capacitance c_g on the applied drain voltage has not been accurately modeled. The voltage dependence of the intrinsic gate-source capacitance has been modeled [3], [5] assuming a linear dependence of the depletion depth along the channel. This assumption results in an analytical expression for the gate capacitance which is independent [5] of drain-source voltage V_D . This result is incorrect. Experimental results [6], [7] show that c_g decreases with increasing V_D when the device is biased below current saturation. After current saturation, c_g increases as V_D is increased. The reported rates of increase of c_g in the saturated region, differ significantly [6], [7]. In some circuit designs GaAs MESFET's are employed as gate-controlled variable resistors. In such cases, and also for the analysis of MESFET low-frequency noise characteristics [8], detailed accurate knowledge of the dependence of the gate-source capacitance on the applied drain and gate voltages in the linear region is essential.

In this paper we report the derivation of an analytical expression for the gate-source capacitance as a function of

the applied gate and drain voltages. The analysis, which is based on a one-dimensional gradual channel approximation, is valid for normally on MESFET's that are biased below saturation. MESFET capacitance measurements confirm the validity of the derived expression when the MESFET is biased in the linear regime and show approximate agreement with theory even when the device is biased into saturation.

II. THEORY

Fig. 1 shows a schematic of the approximate MESFET channel geometry for the case where the drain-source voltage $V_D < V_S$, the voltage needed to induce current saturation. A two-dimensional numerical analysis of the electrostatic potential at a metal-semiconductor interface [9] shows that the charge depletion caused by the fringing fields at the edges of the gate contributes a fringing component to the intrinsic gate capacitance c_g ($\approx 1.8 \times 10^{-12}$ F/cm gate width), which is independent of the gate voltage V_g . It can be shown that for a biased MESFET this fringing capacitance is essentially independent of V_D also. Therefore, in calculating the voltage dependent component of c_g we ignore the charge depletion associated with the fringing fields at the edges of the gate.

We make the following assumptions: the electron density $n = 0$ in the depletion region, n changes abruptly at the depletion layer boundary as well as at the active layer/substrate interface, and n is constant in the channel. Using the gradual channel approximation, the channel current I satisfies the relationship [10]

$$Idy = g(W) dW = -(ne\sigma b/\epsilon)(a - b) db \quad (1)$$

where dy is an incremental length along the direction of current flow in the channel, $g(W)$ is the channel conductance/unit length/unit width, W is the electrostatic potential relative to the gate at some point in the channel, e is the electron charge, and σ , ϵ , and a are the conductivity, dielectric constant, and thickness of the semiconductor active layer, respectively. The channel height at some point (see Fig. 1), denoted b , is given by [10]

$$W = W_0 \left(1 - \frac{b}{a}\right)^2 \quad (2)$$

where $W_0 = nea^2/2\epsilon$ is the channel potential needed to completely deplete the channel. The total charge Q_c in the channel under the gate is obtained by integrating over the

Manuscript received January 5, 1991; revised February 6, 1991.
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IEEE Log Number 9144436.

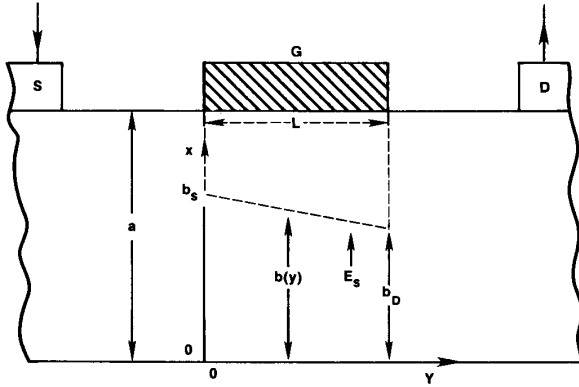


Fig. 1. Schematic of the approximate MESFET channel geometry used to calculate the voltage-dependent component of the gate-source capacitance, $c_g(V_D)$.

gate length L :

$$Q_c = Ze \int_0^L nb(y) dy = \frac{-Zne\sigma}{I\epsilon} \int_{b_s}^{b_D} ab^2 - b^3 db \quad (3)$$

where b_s and b_D , the channel heights at the source and drain ends of the channel, respectively, are given by

$$b_s = a[1 - (W_s/W_0)^{1/2}] \quad (4)$$

$$b_D = a[1 - (W_D/W_0)^{1/2}]. \quad (5)$$

W_s and W_D are the potentials relative to the gate at the source and drain ends of the channel, respectively. The respective gate and drain applied potentials relative to the source, V_g and V_D , are related to W_s and W_D by the relations

$$W_s = |V_b| - V_g \quad (6)$$

$$W_D = W_s + V_D. \quad (7)$$

V_b is the Schottky-barrier built-in potential. Integrating (1) and (3) we obtain

$$Q_c(V_g, V_D) = neZLF_3/F_1 \quad (8)$$

$$F_1 = \frac{ab_s^2}{2} - \frac{b_s^3}{3} - \frac{ab_D^2}{2} + \frac{b_D^3}{3} \quad (9)$$

$$F_3 = \frac{ab_s^3}{3} - \frac{b_s^4}{4} - \frac{ab_D^3}{3} + \frac{b_D^4}{4}. \quad (10)$$

Using (4), (5), and the identity

$$\frac{db_s}{dV_g} = \frac{\epsilon}{ned} \quad (11)$$

the voltage-dependent capacitance is obtained from (8):

$$c_g = \frac{dQ_c}{dV_g} = \frac{\epsilon ZL}{d} \frac{(F_1 F_2 - F_3 F_4)}{F_1^2} \quad (12)$$

$$F_2 = ab_s^2 - b_s^3 - ab_D^2(W_s/W_D)^{1/2} + b_D^3(W_s/W_D)^{1/2} \quad (13)$$

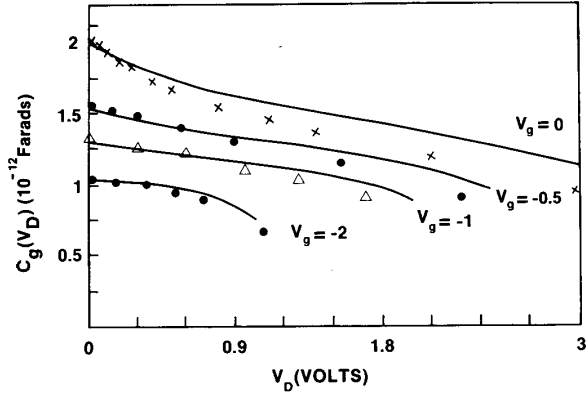


Fig. 2. Plots of the measured and calculated (shown by the lines) gate-source capacitance c_g of the 10- μ m gate-length MESFET as a function of drain-source voltage V_D , for various gate-source voltages V_g .

$$F_4 = ab_s - b_s^2 - ab_D(W_s/W_D)^{1/2} + b_D^2(W_s/W_D)^{1/2}. \quad (14)$$

Note that for $V_D = 0$, (12) reduces to the well-known result $c_g = \epsilon ZL/d$.

The effect of the parasitic series resistance can be modeled in the linear region by using the approximation

$$V_D = V_{Dx} R_c / (R_c + R_p) \quad (15)$$

where V_{Dx} is the potential of the drain contact relative to the source contact, R_c is the channel resistance in the linear region, and R_p is the total series parasitic resistance. The intrinsic c_g can be obtained from the measured gate-source capacitance c_{gx} using

$$c_{gx} = c_g \left(1 - R_s \frac{dI}{dV_{gx}} \right) \quad (16)$$

where R_s is the series parasitic resistance in the source end of the channel and V_{gx} is the potential of the gate contact relative to the source contact.

III. EXPERIMENTAL RESULTS

Capacitance measurements were carried out on 1- μ m and 10- μ m gate-length MESFET's which were fabricated from molecular-beam-epitaxy (MBE-) grown wafers with an active layer thickness of 0.27 μ m. The devices have a gate width of 200 μ m. From capacitance-voltage measurements we determine that the carrier density $n = 8 \times 10^{16} \text{ cm}^{-3}$ for $d \geq 0.1 \mu$ m (corresponding to $V_g \leq -0.1$ V) and that n decreases gradually for $d < 0.1 \mu$ m. From the current-voltage characteristics we determine that the pinchoff voltage $W_0 = 4$ V and that $V_s = 3.1$ and 0.9 V for the long and short gate-length MESFET's, respectively. A Boonton 1-MHz capacitance meter was used to measure the gate-source capacitance with a resolution of 10^{-15} F. The voltage-independent component of the gate-source capacitance (which included the fringing and the bonding pad components of the gate capacitance) was determined by biasing the MESFET into the pinchoff regime.

The measured and calculated (shown by the lines) voltage-dependent component of the gate-source capacitance is plot-

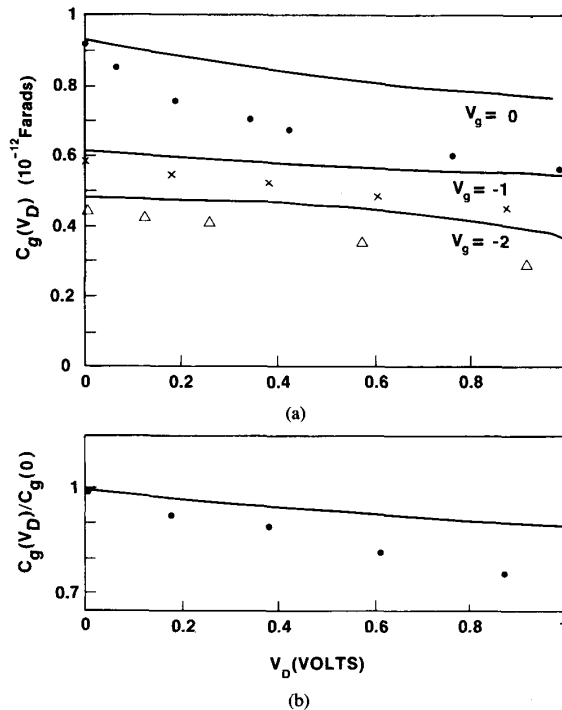


Fig. 3. (a) Plots of the measured and calculated (shown by the lines) gate-source capacitance of the 1- μ m MESFET as a function of drain-source voltage V_D , with gate-source voltage V_g , as a parameter. (b) Plot of the measured and calculated (shown by the line) ratio $c_g(V_D)/c_g(V_D = 0)$ as a function of V_D for the 1- μ m MESFET with $V_g = -1$ V.

ted as a function of V_D (taking into account the potential drop across the parasitic resistance), with V_g as a parameter, in Figs. 2 and 3(a) for the 10- and the 1- μ m MESFET, respectively. The measured dependence of c_g on V_g with $V_D = 0$ shows excellent agreement with theory for the 10- μ m MESFET and reasonable agreement with theory for the case of the 1- μ m device. In the latter case the small differences between theory and experiment can be attributed to the approximation that the depletion-layer boundary is sharp and the experimental error associated with measuring the small gate capacitance. For small V_D and $V_g \leq -0.5$ V, Figs. 2 and 3(a) show that the measured c_g decreases with increasing V_D in accordance with theoretical predictions. Note that for small V_D and $V_g = 0$, Fig. 2 shows that c_g decreases with increasing V_D at a faster rate than our theory, which assumes uniform carrier density, predicts. This is caused by the

observed nonuniform carrier density in the surface region $d < 0.1$ μ m. For average channel electric fields, $E \approx V_D/L > 2000$ V/cm, we find that c_g decreases with increasing V_D faster than our calculated results, which are based on the gradual channel approximation which is valid under low-field conditions. Nevertheless we obtain reasonable agreement between theory and experiment over a wide range of V_D . Experimental and theoretical values of c_g differ by 10% when $E = 2000$ V/cm and by 20% when the MESFET's are biased into saturation. This result is seen more clearly in Fig. 3(b), which shows a plot of the measured and calculated ratio $c_g(V_D)/c_g(V_D = 0)$ as a function of V_D with $V_g = -1$ V for the 1- μ m MESFET.

In concluding, we point out that while a two-dimensional numerical analysis is more accurate than the analysis presented here, our results suggest that the derived analytical expression for the gate capacitance may be used for the analysis of device characteristics in view of the complexities of a two-dimensional device simulation.

ACKNOWLEDGMENT

The authors thank R. Moerkirk for materials characterization and M. Lloyd-Saunders for processing support.

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