Nanofabrication with Proximal Probes

ERIC S. SNOW, PAUL M. CAMPBELL, AND F. KEITH PERKINS

Invited Paper

In this paper, we describe the use of proximal probes, such as the atomic force microscope (AFM) and the scanning tunneling microscope (STM), for nanofabrication. A resistless proximal probe-based lithographic technique has been developed that uses the local electric field of an STM or conductive AFM tip that is operated in air to selectively oxidize regions of a sample surface. The resulting oxide, typically 1–10 nm thick, can be used either as a mask for selective etching or to directly modify device properties by patterning insulating oxides on thin conducting layers. In addition to this resistless approach, we also describe the use of the STM/AFM to modify the chemical functionality of self-assembling monolayer films. Such modified films are used as a template for the selective electroless plating of metal films. The above processes are fast, simple to perform, and well suited for device fabrication. We apply the anodic oxidation process to the fabrication of both semiconductor and metal-oxide devices. In these latter structures, sub-10 nm-sized device features are easily achieved, and we describe the fabrication of the smallest possible device, a single, atomic-sized metallic point contact by using in situ-controlled AFM oxidation.

Keywords— *Lithography, MIM devices, semiconductor device fabrication.*

I. INTRODUCTION

Proximal probes such as the scanning tunneling microscope (STM) and the atomic force microscope (AFM), originally developed to image surfaces with atomic resolution, have recently been used to modify surfaces at the nanometer scale and have even achieved the manipulation and positioning of single atoms on a surface [1]. This suggests that proximal probes may exceed the limits of electron-beam lithography and perhaps achieve the ultimate goal of atom-by-atom control of materials modification. This potential has motivated researchers to attempt to implement this level of control into actual device fabrication [2]–[4]. However, this task has not been easy due to the irreproducibility of the modifications, the slow "write" speed, and the difficulty of transferring such fine manipulations into a functioning semiconductor or metallic device. The challenge has been to overcome these limitations and achieve a reliable process for device fabrication.

Recent advances in proximal probe nanolithography have lead to a number of techniques that are useful for device fabrication, and such techniques are now capable of fabricating unique nanometer-scale devices that are difficult to fabricate by conventional lithographic techniques. In the most widely employed process, an electrically conducting AFM (or STM) tip that is operated in air is used to anodically oxidize selected regions of a sample surface [5], [6]. This process is analogous to conventional electrochemical anodization; however, in this case the cathode of the electrochemical cell is replaced by an AFM/STM tip, and water from the ambient humidity serves as the electrolyte. When an electrical bias is applied to such a system, the sample surface is locally oxidized over lateral dimensions of 10–100 nm and to a depth of 1–10 nm, the size depending on the type of sample, the shape of the tip, and the exposure conditions.

This and other more recently developed AFM/STM lithographic processes can be used for a variety of applications such as fabricating masks for selective etching [7], patterning growth templates by using self-assembling monolayer films (SAM's) [8], directly patterning the conduction path through thin conducting films [9], [10], and mechanically machining thin resist layers [11]. In all such applications the fine resolution and unique imaging properties of proximal probes can be utilized to achieve a unique lithographic tool that is well suited for device fabrication [12]–[15]. In addition, recent advances in micro-electromechanical device manufacturing make possible the fabrication of large parallel arrays of AFM's [16]. Such advances, when combined with the various AFM lithography techniques, have the potential for high-throughput nanofabrication. These unique features, whether utilized by the bench scientist for prototyping individual devices or potentially by a fabrication facility for high throughput nanolithography, make the AFM a valuable new tool for nanostructure fabrication.

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The authors are with the Naval Research Laboratory, Washington, DC 20375 USA.

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II. Proximal Probe Nanolithography

A. Oxidation and Selective Etching: Resistless Nanolithography

The application of STM/AFM surface modifications to device fabrication has proven difficult, in part because such probes perform best when modifying very thin layers of material which, for the most part, are not sufficiently robust for pattern transfer into a semiconductor or metallic structure. Such thin layers are necessary in order to attain fine resolution with probe tips that act as a diverging source of charge or electric field. This restriction does not apply to conventional electron-beam lithography systems that can achieve fine lateral resolution by exposing relatively thick resists with a focused beam of high energy electrons. One key to proximal probe-based nanofabrication has been the development of a fast, reliable exposure process that produces a local surface chemical modification that can be used for pattern transfer by selective etching. Because the exposure process modifies only the top few monolayers of material, and because extremely selective etches are available, both high resolution and effective pattern transfer are easily accomplished with this technique.

In the anodic oxidation process an electrically conducting AFM (or STM) tip that is operated in air is electrically biased with a negative polarity relative to a sample surface. The ambient humidity serves as an electrolyte such that the biased tip anodically oxidizes a small region of the surface. This exposure process has been investigated by a number of researchers. Dagata *et al*. were the first to report the STM-induced oxidation of an H-passivated Si (111) surface [5], [17]. Since then, several related studies have been published by a number of researchers [18]–[21]. While the ambient process is an electrochemical reaction that requires an ambient humidity, it is also possible to selectively oxidize the H-passivated Si surface by using a UHV STM. In this process, a low-energy electron from the STM tip excites an Si–H bonding electron to an antibonding orbital, thus selectively removing the H from the Si surface [22]. These depassivated regions can then be selectively oxidized by a subsequent exposure to oxygen gas [23]. The advantage of this approach is that near-atomic resolution of both the depassivation and the oxidation can be achieved. However, while this UHV process demonstrates the ultimate limit of materials modification, the ambient oxidation process is currently much more compatible with device fabrication because it is faster, and it does not require a UHV environment.

The advantage of the anodic oxidation technique is that it provides a simple, reliable process for making a highly local chemical modification to a surface. In addition, the oxidation process is fairly general and can be applied to most materials that can be anodized. The successful application of this oxidation process depends on finding uses for such thin oxides. One application is the use of these surface oxides as a mask for pattern transfer by selective etching [7].

For Si oxidation and etching, the sample preparation procedure we use is a chemical cleaning of n- or p-type (100) Si wafers followed by a 1-min dip in a 10% aqueous HF solution. The HF solution removes the native surface oxide and passivates the surface with a monolayer of H. The surface oxidation is accomplished by exposing selected regions of the surface to a negatively biased STM or AFM tip. A tip bias of -2 to -10 V is normally used for exposure with write speeds of 0.1–100 μm/s in an ambient humidity of 20–40%.

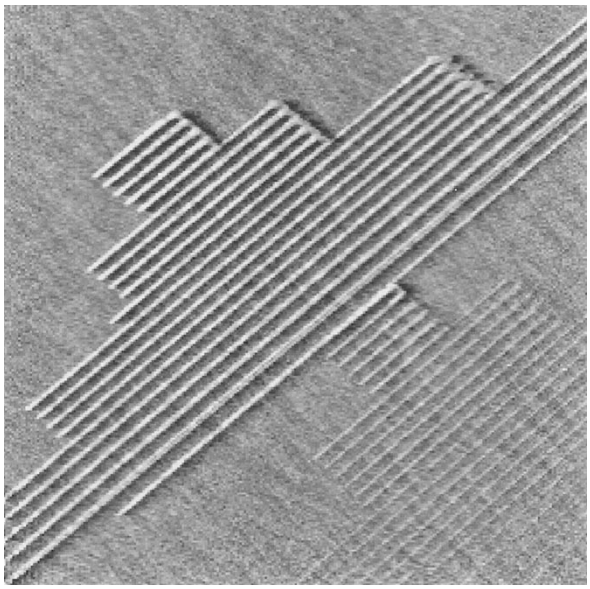
The most flexible tool for exposure is the AFM because the exposure mechanism, the tip voltage, can be applied independently of the feedback control of the tip-sample positioning. This decoupling of the feedback control allows imaging of the surface without risk of exposure and also allows the AFM to operate on insulating as well as conducting surfaces.

Fig. 1(a) shows an AFM image of an oxide pattern written by a Ti-coated AFM tip [6]. The AFM image was obtained immediately after writing by using the same tip that wrote the pattern. The act of imaging does not expose the passivated regions of the surface, nor does it damage the exposed oxide patterns. The height of the oxide is about 1.5 nm, and the period of the grating is 120 nm. The bottom section of the pattern was written at 1.5 V, while the top section was written at 2.5 V. All lines were written at the same scanning frequency so that the longer lines correspond to a higher write speed. The shortest lines were written at 1 μm/s, while the longest lines were written at 10 μm/s.

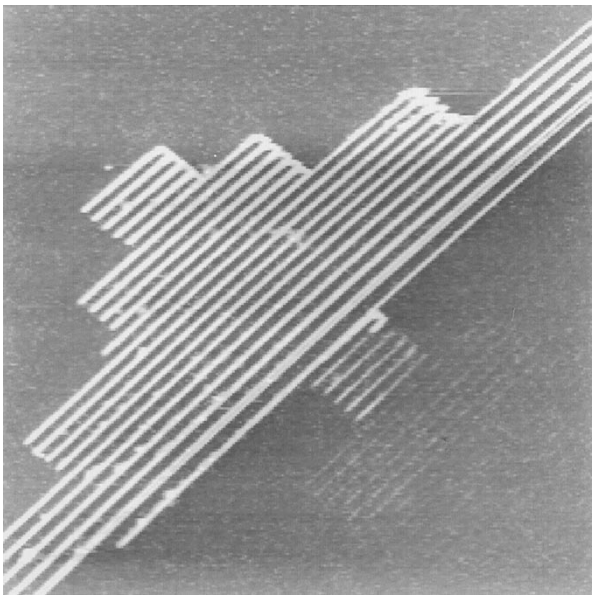
Note in Fig. 1(a) that the oxide pattern is easily observable and is much more pronounced than the background roughness of the surface. This latent image allows the success or failure of an exposure to be determined prior to etching. For example, the pattern written at 1.5 V was marginally exposed, while the pattern written at 2.5 V produced smooth continuous lines.

Fig. 1(b) shows an AFM image of the same pattern after etching 10 nm into the surrounding Si with an 11-molar aqueous KOH solution [6]. The pattern is faithfully transferred by the selective etch except in the underexposed regions that were written at 1.5 V. Thus, inspection of the oxide pattern can accurately predict those portions of the pattern that will withstand the etch. The apparent roughness observed on some of the etched lines is not due to irregular exposure or etch roughness, but due to debris left behind by the etch solution.

For deep etches, hydrazine is preferred because of its excellent selectivity against oxidized Si. Fig. 2(a) shows an AFM image of an oxide pattern written on the surface of a sample of SIMOX [24], a type of Si-on-insulator material that consists of a (100) Si wafer that has been ion implanted with oxygen and annealed to form an electronic grade SiO_2 layer buried beneath a crystalline Si surface. In this sample, the AFM-generated oxide pattern is difficult to see because it is masked by similar dimension features present on the unpatterned SIMOX surface. This oxide pattern, that is $\sim$1 nm thick, was transferred into the top Si layer of



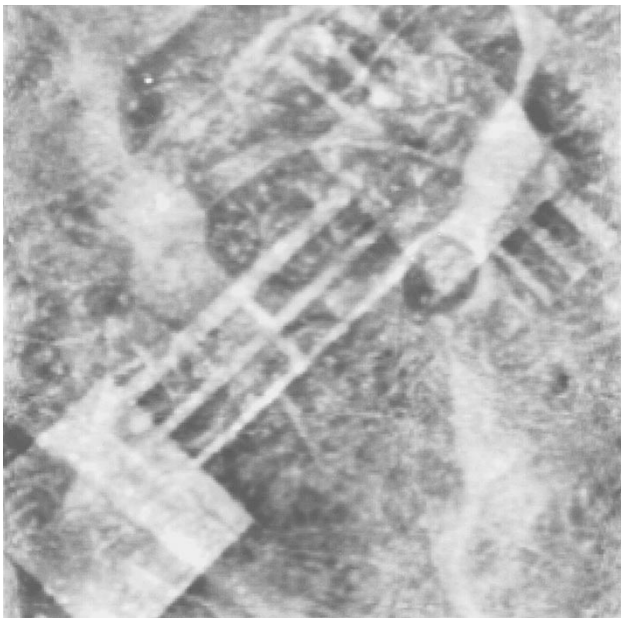
(a)



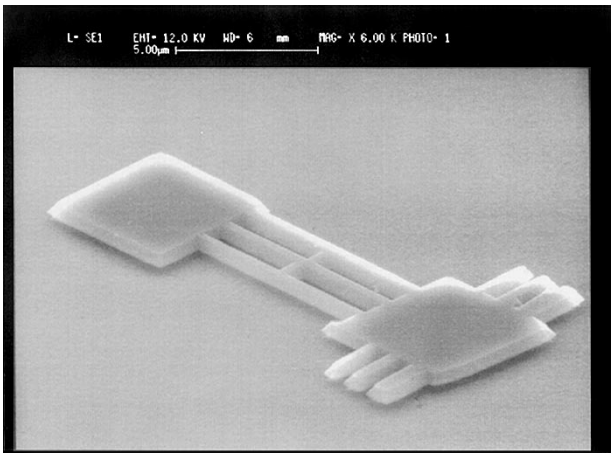
(b)

Fig. 1. (a) 5 μm $\times$ 5 μm AFM image of a 120-nm pitch oxide pattern written by the AFM and (b) the same pattern as above after etching 10 nm into the surrounding Si. The top half of the pattern was written at 2.5 V, the bottom portion at 1.5 V. The shortest lines were written at 1 mm/s, while the longest were written at 10 μm/s.

the sample by a 0.3 μm-deep etch with 70°C hydrazine. The unpatterned Si regions were etched down to the buried oxide layer which acts as an etch stop. The buried oxide layer was then etched in an HF solution for a time sufficient to completely undercut the wires and cantilevers but not enough to undercut the square support pads. This step produces the freestanding wires and cantilevers observed in the scanning electron microscope (SEM) image of Fig. 2(b) [24]. Both the uniformity of the etched features and the lack of any pinholes demonstrate the excellent properties of this thin (~1-nm thick), AFM-generated oxide as an etch mask.



(a)



(b)

Fig. 2. (a) 20 μm $\times$ 20 μm AFM image of an oxide pattern written by an AFM on the surface of a sample of SIMOX and (b) an SEM image of the same pattern after it has been etched down to the buried oxide layer with warm hydrazine and partially undercut by etching the SiO_2 layer with an HF solution.

B. Silicon as a Resist

While the passivation, oxidation, and selective etching process is well suited for patterning Si, most other material systems lack the unique surface properties of Si, and a more general lithographic process is required. A general approach to patterning materials other than Si is to cap such materials with a thin Si layer that can be patterned via the above approach and used as an etch resist to pattern the underlying material of interest. In this case, the desired surface properties are achieved by the Si capping layer which can be patterned via the passivation, oxidation, and selective etching process.

As a first test of this approach we used molecular beam epitaxy (MBE) to deposit a thin (~5-nm thick) pseudomorphic layer of Si on a wafer of GaAs [25]. We

used MBE growth in order to achieve a capping layer with surface and etch properties which closely approximate those of bulk Si. Indeed, we have found that such layers are easily patterned with the passivation, oxidation, and selective etching process and that they form an effective mask for etching GaAs. This result represents a first step toward a more general resist-based approach to proximal probe nanofabrication.

Further improvements in this process have been made by eliminating the need for MBE growth and by using hydrogenated amorphous Si (a-Si : H) as the resist layer which can be deposited on a wide range of materials. At least three groups have used a-Si : H for this purpose. Kramer *et al*. [26] used HF-passivated and STM-oxidized a-Si : H as a resist layer to etch fine metal wires. In a similar approach, Minne *et al*. [27] were successful in patterning a variety of structures (including a 0.1-μm gate MOSFET) by using reactive ion etching to selectively etch an AFM-patterned a-Si : H resist layer, and Madsen *et al*. have used both optically induced depassivation and the AFM to oxidize and pattern such layers [28]. These accomplishments are significant because they demonstrate a general application of the anodic oxidation and selective etching process to a variety of material systems by using easily deposited a-Si : H films as a resist layer.

C. Limiting Write Speed

An important issue for any lithographic technique is the ultimate write speed and spatial resolution of the technique. This is particularly the case for proximal probe-based lithography which is traditionally very slow. The typical write speeds that we use for AFM oxidation are of order 1–10 μm/s. However, it is possible to write at significantly higher speeds, although under such conditions we observe an increased rate of tip degradation. To estimate a maximum write speed for Si anodization, $v_{\max}$, we have used voltage pulsing to determine the minimum time required for oxidation, τ_{th} (i.e., the time required to produce a 0.5 nm-thick oxide feature), of a (100) Si surface as a function of the magnitude of the voltage pulse, V, applied to Ti-coated AFM tip [6]. $v_{\max}$ is then estimated to be s/τ_{th}, where s is the resulting oxide feature size. Over the range of 1–10 V we find an exponential dependence τ_{th} on the applied voltage (see Fig. 3), i.e., $\tau_{th} = \tau_0 \exp(-V/V_0)$, where τ_0 ranges from 1–10^3 s and V_0 ranges from 0.25–1 V, the exact values depending on the ambient conditions and the tip condition. Consequently, $v_{\max} = (s/\tau_0)\exp(V/V_0)$, where s is $\sim$30 nm. In principle, $v_{\max}$ can be extended to arbitrarily high values by increasing the tip voltage; however, in practice, above a limiting voltage the pulse causes damage to the Si surface. This establishes a maximum write speed of $\sim$1 mm/s for the oxidation of (100) Si. This observed exponential behavior is consistent with the model of Kramer [29] who suggests that the initial oxidation rate is determined by the desorption of OH^- from the tip and that the desorption rate depends exponentially on voltage.

Recently Teuschler *et al*. [30] have studied the kinetics of the oxide growth on (111) H-passivated Si surfaces,

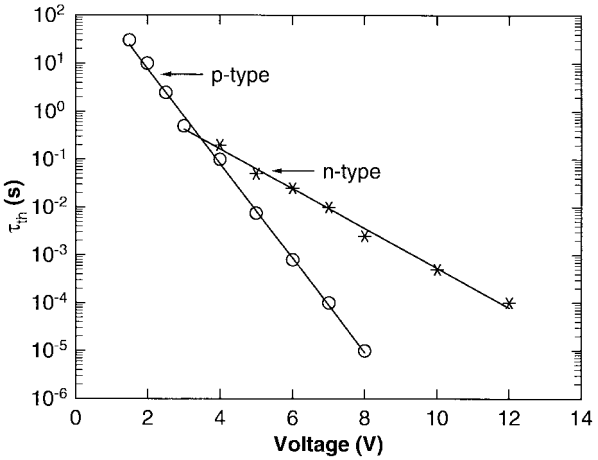


Fig. 3. Plot of the threshold exposure time τ_{th} versus voltage for an n- and p-type sample.

and they established an empirical expression relating the thickness of the resulting oxide, z, to the applied voltage, V, and the write speed, v: $z = \alpha(V - V_{th})(v_0/v)^{\gamma}$, where v_0 is an arbitrary constant chosen to be 1 μm/s and α, V_{th}, and γ are parameters that depend on the tip, sample, and ambient conditions. For p-type Si anodized with an n-type Si AFM tip in a 60% ambient humidity they found $\alpha = 0.78$ nm/V, $V_{th} = 5.4$ V, and $\gamma = 0.23$.

D. Minimum Feature Size

Due to the local nature of the tip-surface interaction and the fact that the generated oxide is only a few monolayers thick, one can expect extremely fine lateral resolution in the exposure process. Indeed, using our air-ambient exposure process we have produced oxide features with lateral dimensions as small as 10 nm. Lyding *et al*. working with a UHV STM, have achieved near-atomic-scale control of the exposure process, although pattern transfer has not yet been demonstrated with these UHV-formed oxides [22], [23]. While this UHV process demonstrates the ultimate potential of the exposure process, continued improvement in the size of etched features requires directional dry etching techniques which can improve the limited aspect ratios obtained by liquid etching.

To explore the resolution limits of etched features we have used an electron cyclotron resonance (ECR) source to etch Si nanostructures that were patterned by selective oxidation of an H-passivated Si surface with an anodically-biased AFM tip [31]. The oxide patterns were etched in a Cl_2 plasma generated by an ECR source. The etch conditions were optimized to provide high selectivity over the oxide mask, a vertical etch profile, and smooth surface morphology. Si nanostructures with $\sim$10 nm width and 30 nm depth were etched in a Cl_2/O_2 plasma (see Fig. 4). Wider structures with a thicker oxide were etched to a depth of 70 nm with no signs of mask degradation.

This result indicates that ambient AFM-oxidation and selective dry etching is suitable for fabricating structures with lateral dimensions as small as 10 nm. Combining this etching technique with the UHV-based exposure process

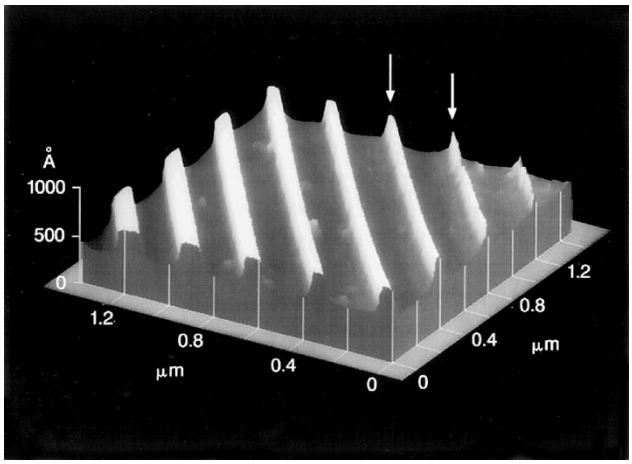


Fig. 4. AFM image of a pattern etched into an Si sample by using an Cl_2 plasma generated by an ECR source. The etch depth was 30 nm. The two lines indicated by the arrows have linewidths of 20 and 10 nm.

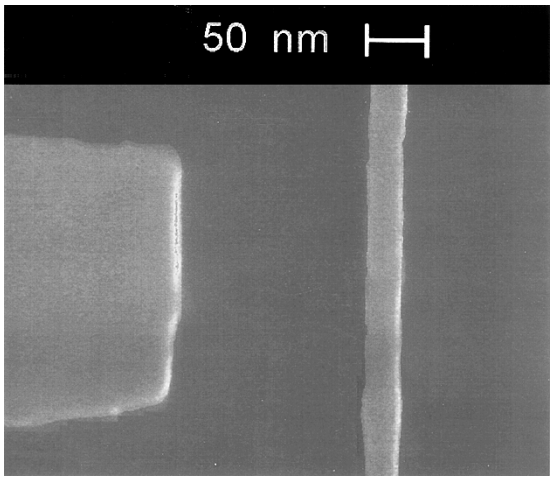


Fig. 5. SEM image of the active region of a side-gated transistor fabricated from SIMOX. The width of the source-drain channel is 30 nm.

should produce structures in the 1–10 nm range. Structures of such small dimension are not easily attainable with conventional fabrication techniques. The fact that such small structures are easily fabricated and can be adapted into device fabrication schemes illustrates an important, unique aspect of proximal probe-based nanolithography and indicates that such lithography will be an integral part of future nanostructure science and technology.

III. Device Fabrication

A. Device Fabrication by Using Selective Oxidation as an Etch Mask

A unique feature of AFM-based lithography is that the exposure and imaging mechanisms of the AFM operate independently. Thus, high-resolution images of the sample can be obtained and used for precise pattern alignment without risk of exposure. In addition, latent imaging of an exposed pattern allows the success of an exposure to be assessed and corrected before further processing. Combining these imaging capabilities with the high-resolution exposure process makes the AFM a unique lithographic tool, well suited for fabricating critical features in nanometer-scale devices. As a demonstration of this capability, we have used AFM-defined oxide patterns and selective etching to fabricate side-gated Si field-effect transistors with critical dimensions as small as 30 nm [13]. Similar structures fabricated in GaAs have been used for fast switching elements because of the intrinsically low gate-channel capacitance of such structures [32].

The devices consist of an etched Si wire between two contact pads and a lateral gate that is isolated from the wire by a small air gap. The wire and gate are isolated from the substrate by using SIMOX. The buried oxide layer of this material forms an effective barrier to isolate the device structure from the substrate [33]. Both the source-drain channels and the side gates were patterned by the AFM, while the ohmic contact pads for source, drain and gate were formed by optical lithography.

The devices were fabricated as follows. First optical lithography was used to deposit the metal ohmic contact pads. The samples were then cleaned and H-passivated. The AFM was used to image these pads and to align the tip for exposure of the source-drain channel and the side gate. After exposure, the oxide patterns were imaged to check the success of the exposure. If any defects were detected, the pattern was corrected before further processing. After the exposure was completed, a sample was then etched in 70°C hydrazine to remove all of the surface Si layer that was unprotected by the oxide pattern or the metal pads down to the buried oxide layer that acts as an etch stop. Fig. 5 is an SEM image of a completed device that is fabricated on a top Si layer that is 40-nm thick [13]. The source-drain wire shown in the figure is $\sim$30-nm wide by 40-nm high by 6-μm long. The lateral gate finger can also be seen.

While the device shown in Fig. 5 serves as a functioning field-effect transistor [13], this basic structure can also be used as a building block for fabricating quantum-effect devices. For example, the source-drain channel could be modified to contain a small island. A sufficiently small island would generate quantum effects arising from discrete quantum levels in the island. It should also manifest single electron charging effects (also known as the Coulomb blockade) that occur when the island capacitance C is small enough that a single electron transferring onto the island creates an electrostatic charging energy $E = e^2/2C$, which blocks a second electron from transferring to the island. Both of these effects depend on fabricating sufficiently small structures such that the quantum confinement energy or the charging energy is greater than kT. Several groups report the use of electron beam lithography to fabricate such structures from SIMOX [34]–[36]. In all cases thermal oxidation is used to shrink the size of the structures following etching such that quantum or charging effects are observable well above 4 K. Proximal probe lithography may provide a means to fabricate structures with dimensions

small enough to manifest these quantum and single-electron charging effects at room temperature, which would open the way for their use in practical applications.

B. Selective Oxidation for Direct Device Modification

An alternate approach to the two-step technique described above (oxide pattern definition followed by pattern transfer by etching) is to use the AFM-generated surface modifications to modify device properties directly. Such an approach has the advantage that the electrical properties of a device can be monitored in real time and tuned to specifications by the anodization. In addition, because the geometry of a device is related to its electrical properties, sub-10-nm feature sizes are easily achieved by using such real-time measurements as a guide for the fabrication.

In particular, the selective oxidation of thin metal films has been used to define narrow metal wires by oxidizing the unwanted regions of wide metal wires [10]. It has also been used to fabricate lateral metal–oxide–metal tunnel junctions by introducing thin regions of oxide in an otherwise continuous metal film [9], [10]. Such lateral metal-oxide-metal junctions can be made very small and thus have correspondingly small junction capacitance. Recent examples of structures which use AFM-generated lateral oxide junctions as the active regions of device structures include a single-electron tunneling (SET) device that was fabricated by using STM-anodic oxidation to form small-capacitance lateral tunnel junctions [14] and the use of an AFM-anodic oxidation to fabricate atomic-sized metallic point contacts that exhibit conductance quantization [15].

In the work described in [10] and [15], the point contacts and tunnel junctions were formed by using the AFM to anodize through the cross section of Al or Ti nanometer-scale wires while using *in situ* electrical measurements as feedback to guide the anodization. These metal wires were formed by first using optical lithography and metal lift-off to pattern ~ 1 μm-wide by 5–8 nm-thick metal wires, each connected to two contact pads. The nanometer-scale patterning of these structures was accomplished by selective anodization using a sharp conducting tip (an Si ultralever tip from Park Scientific Instruments).

A diagram of the fabrication circuit is shown in Fig. 6. The AFM is first used to define a small constriction (typically 40 nm-wide by 500 nm-long, but ones as narrow as 5 nm have been made) in the middle of a 1-μm-wide metal wire [10]. This is done by oxidizing the outer portions of the wire, leaving only the center metallic. In order to achieve the level of control necessary for this step, the electrical resistance of the wire is monitored during the oxidation process. When a resistance corresponding to the desired width is obtained, the tip bias is automatically set to zero, thus terminating the oxidation process. To form a lateral oxide junction, the tip is scanned repeatedly across a section of this constriction while slowly increasing the tip voltage. As the tip voltage is increased, the oxide penetrates deeper into the metal film, thus increasing its resistance. When a predetermined resistance value is achieved, corresponding to the desired junction properties, the tip voltage is automatically set to zero. Fig. 7 shows an AFM image of a completed single oxide junction device. The 1-μm-wide metal wire, the oxide that defines the 40-nm-wide constriction, and the lateral oxide barrier (highlighted by the circle) are shown.

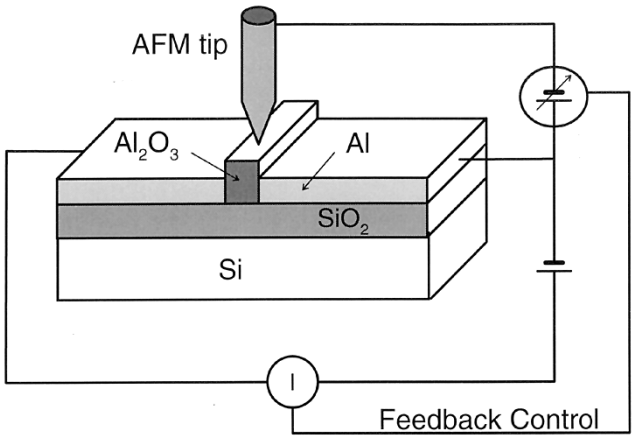


Fig. 6. Diagram of the circuit used for fabricating the metal–oxide device structures. The device current was measured in real time during the fabrication to guide the anodization.

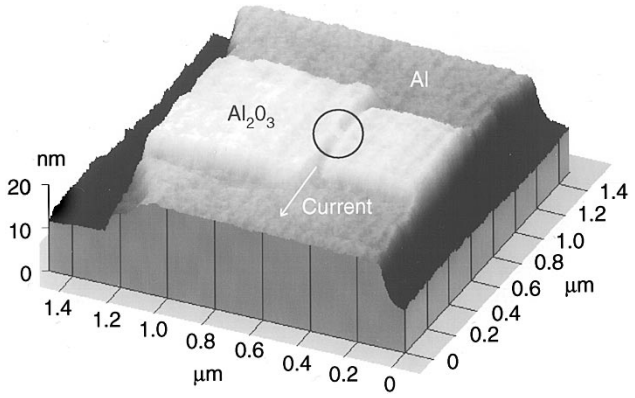


Fig. 7. AFM image of an $_{Al/Al_2O_3}$ lateral metal–oxide–metal junction. The current is first constricted down to a 40 nm-wide wire and passes through the lateral metal/oxide junction indicated by the circle.

If the oxidation procedure is continued until the oxide penetrates almost completely through the metal wire, most parallel conduction paths will be shut off. As the size of the remaining metal conduction channel decreases, it eventually approaches the limit of ballistic conduction through a one-dimensional channel, for which the conductance becomes quantized in units of $2e^2/h$. In order to achieve this regime of quantized conductance, the current flow must be constricted to a region of size $\sim\lambda_f/2$, where λ_f is the Fermi wavelength. For metals, because $\lambda_f/2$ is $\sim$0.2 nm, a quantized conductance of $2e^2/h$ indicates a conduction channel of size on the order of a single atom. These atomic-sized conduction channels form the point contacts, and they are evidenced by the discrete decreases in conductance $\sim 2e^2/h$ (shown in Fig. 8) as these last remaining paths are closed.

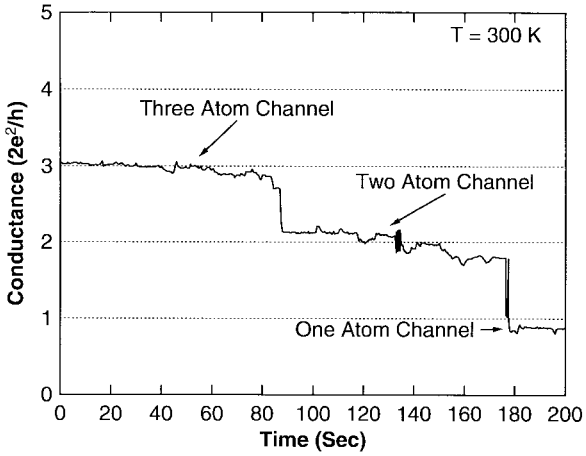


Fig. 8. Conductance of an Al/Al_2O_3 junction as the last remaining conductance channels are cut off. The conductance is quantized in approximate units of $2e^2/h$. A conductance of $2e^2/h$ corresponds to a one-atom conductance channel.

Fig. 8 plots the time dependence of the conductance of an Al point-contact device after the tip voltage was set to zero and indicates that additional oxidation events occurred during this time. These oxidation events correspond to the large discrete steps to lower conductance which close the remaining conduction paths. These steps occurred in approximate, but not exact, units of $2e^2/h$. This behavior is consistent with other metallic point-contact experiments [37]–[41] and can arise from a number of sources such as electron scattering, the detailed electronic wavefunctions of the Al atoms, and from series resistance of the thinned Al layer leading to the actual atomic-sized point contact. The device eventually stabilized at a conductance value $\cong 2e^2/h$ that corresponds to a single, atomic-sized conductance path [41]. In such stabilized devices, it is possible to maintain a stable one-atom point contact over a period of a day or more. Such atomic-sized wires demonstrate the level of control that is achievable by using real-time electrical measurements as feedback to guide the AFM anodization.

As the last remaining conduction path is closed, the conduction through such devices changes from metallic to tunneling. In Al structures it is difficult to achieve a reproducible tunneling resistance because the large Al/Al_2O_3 barrier height ($\sim$2 eV) results in large discrete resistance changes for each subsequent oxidation event. In contrast, by using Ti/TiO_x, which has an approximate order of magnitude smaller barrier height, tunnel junctions with predetermined resistances can be made.

Such control of the tunneling resistance, combined with the intrinsically small capacitance of the lateral geometry, makes the Ti/TiO_x system attractive for lateral tunnel-junction devices. Matsumoto *et al.* recently reported the fabrication of a room-temperature operational SET device by using STM-anodization of a thin Ti film [14]. In addition, a novel nanometer-scale transistor can be constructed by using a gate to modulate the transmission through such a lateral tunnel barrier [42]. AFM anodization provides a powerful tool for exploring such novel metal/oxide-based devices.

IV. High-Throughput Nanolithography

A. SAM's

An aspect of proximal probe lithography (PPL) that is often overlooked is the utility of imaging layers. Imaging layers are used in other lithographic technologies as a means of recording a pattern, either by masking, as with photon-based processes, or by direct writing, as with e-beam writers. While several schemes have been demonstrated that record information as written by proximal probes (in addition to the previous section, see the reviews by Marrian [43] and Shedd and Russell [44]), these schemes are limited in terms of writing speed, range of substrate applicability, or ability of masking various etch processes, to name a few. For this reason, in our laboratory we have devoted considerable effort to finding imaging layers suitable for high-speed, high-resolution lithography based on pattern transfer of STM and AFM generated patterns.

Polymeric films, such as commercial e-beam resists poly(methylmethacrylate) and SAL-601-ER7$^{\mathrm{TM}}$ [45], have demonstrated high-resolution capabilities in STM lithography [46], [47], and investigations are currently underway to investigate their suitability for AFM-based lithography [48]. Unfortunately, films sufficiently thin to be compatible with the current feedback mechanism of an STM are generally too thin to make useful etch masks or defect-free lift-off layers. SAM's have not only demonstrated high resolution [49], but also compatibility with PPL [50] and functionality as a hard etch mask [8]. Because the mechanism that drives self-assembly is a highly energetic chemisorption reaction [51], films based on these materials have an extremely low defect density, are quite environmentally stable, and are mechanically robust.

Insofar as it affects PPL, the precursors from which SAM's are grown may be thought of as consisting of three parts, as shown in Fig. 9: a substrate binding part, a spacer part, and a surface functionality part. While these parts are not quite fully interchangeable from one molecule to the next, different considerations are appropriate for the selection of each. For the surface binding part, a silane (RSX_3) is used to bind to hydroxol (OH) groups (typical on Si and Pt). Hydrogen substituents on the silane (the "X" part) are most commonly methoxy groups (CH_2O), Cl, or a mixture of the two. The composition of the surface binding part strongly affects film ordering [52], the tendency of the film to grow multilayers [53], and, to a lesser extent, the packing density [54]. A thiol (RSH) forms highly ordered layers on surfaces of GaAs [55] or Au [56]. The spacer part has an effect on the interaction of the film with the tool. By moving the functional part away from the surface and closer to the high field of the tip, long spacer groups (multiple CH_2 groups, for example) can lower the dose or voltage threshold for exposure [50]. The conjugated bonds found in phenyl groups are also somewhat conductive, and hence more amenable to STM operation [57]. The surface functional group actually defines the "new" surface. For example, amine (NH_2) groups can be used as ligation sites for certain molecules [58]. While

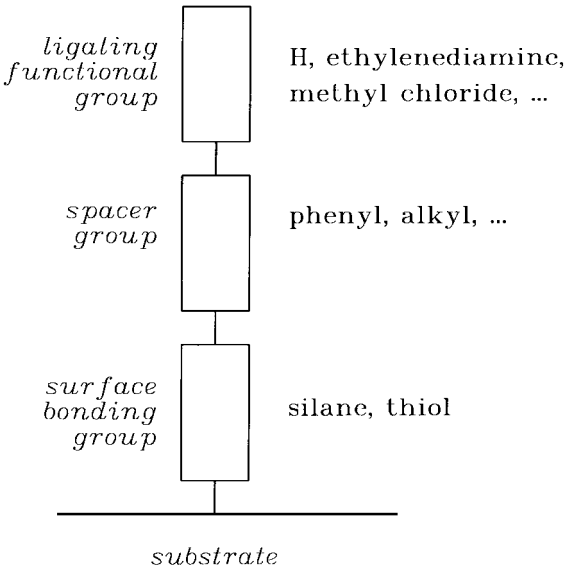


Fig. 9. Component representation of precursor molecules used for SAM growth.

not particularly active themselves, halides (Cl, I, etc.) have an extremely high cross section for electron capture and subsequent desorption of the halide fragment [59]. Subsequent processing can be based on either replacing the halide atom with a more reactive functional group [60] or acting upon the fragment remaining after halide desorption [61]. Alkyl terminated surfaces are extremely inert and hydrophobic, being chemically identical to paraffin. As such, they have been used for pattern transfer as masks against wet etching [62]–[64] and, to a limited extent, dry etching [65]. They have also been used to *enhance* STM-induced etching of gold [66], [67].

So far, the only investigations of functionalized monolayers as imaging layers for PPL have used organosilanes to grow films on Si. We have used a Pd-containing oligimeric colloid [58], [68] as an intermediate step in the eventual generation of a high-resolution patterned Ni layer, useful as a hard etch mask [64]. This process is illustrated in Fig. 10. After cleaning and hydrogen passivation in dilute HF, the wafer sample is immersed briefly in a solution of the monomer, removed, and dried on a hot plate. The resulting film thickness is on the order of 1–1.3 nm [52]. After STM patterning (and ligand grafting, in the case of certain films [60]) the sample is immersed in the colloidal Pd, which selectively ligates onto the unexposed film forming a layer another 2.6 nm thick [68]. The sample is subsequently rinsed and again immersed into a nickel borate electroless plating bath [69], where nucleation of the Ni is catalyzed by the Pd. In this way, we have been able to write gaps between Ni pads as small as 15 nm and have transferred them through reactive ion etching into Si (Fig. 11). Under optimal conditions, the distribution of Pd particle diameters peaks at about 25 nm. However, there is a substantial number of particle diameters below 10 nm. Furthermore, the Ni growth is somewhat anisotropic and tends to smooth rough edges. Edge roughness of fine patterns is generally

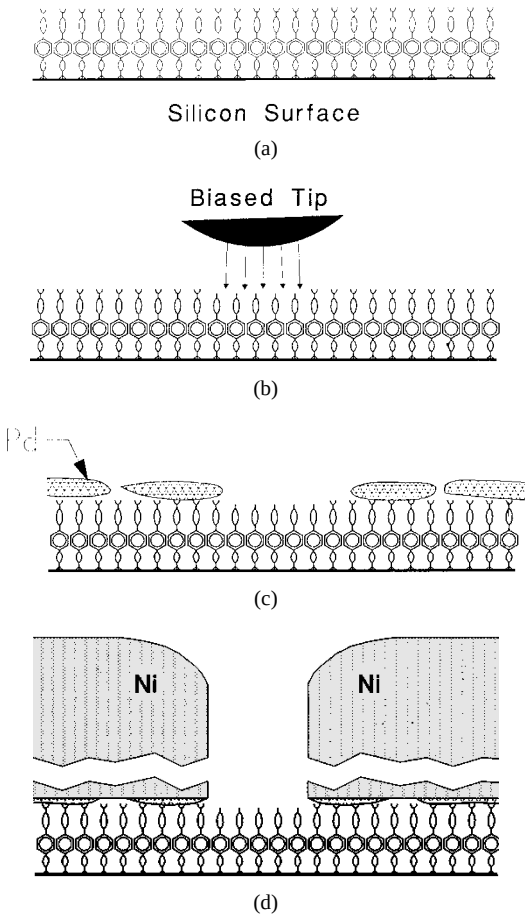


Fig. 10. Schematic illustrating replication of a high-resolution pattern in an STM exposed SAM film. (a) Starting SAM film, (b) pattern generation by using an STM as a source of low-energy electrons to interact with and expose the film, (c) ligation of Pd catalyst, and (d) electroless growth of Ni from solution.

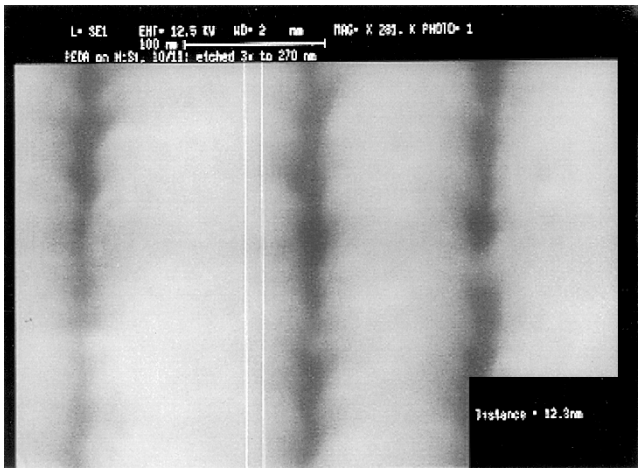


Fig. 11. SEM image of narrow trenches etched into Si created by the process illustrated in Fig. 10. The parallel white lines are spaced by 12.3 nm.

below 3 nm (rms). The Ni may be easily removed after patterning by immersion in the catalyst solution.

We have investigated exposure characteristics of several organosilane films using a vacuum STM: octadecyltrichlorosilane [OTS], (aminoethylaminomethyl)

phenethyltrimethoxysilane [PEDA], chloromethylphenyltrimethoxysilane [CMPTS], chlormethylphenethyltrimethoxsilane [CMPETS], and -monochlorodimethoxysilane versions of PEDA and CMPTS. Exposure threshold voltage is primarily determined by the end group and is generally reduced about 2 V for films grown on passivated Si rather than the terminal native oxide (NO): ~10 V for OTS on NO, 8 V for PEDA on NO, 5 V for PEDA on Si, 4 V for CMPTS on NO, and under 2 V for CMPTS and CMPETS on Si. We have not observed a minimum dose threshold for exposure to the limits of our equipment, 30 nC/cm linear dose. We have also investigated the use of a conducting tip air ambient AFM to modify a deposited PEDA film on NO, observing an exposure threshold at 5 V [71].

SAM's have an advantage over other investigated imaging layers in that the "granularity" of the film is relatively large. Analogously to photographic film, speed is inversely proportional to grain size. In other words, a smaller dose is needed to expose a given area. For example, the molecular density of a PEDA film is 5 nm^{-2} [52]. In comparison, the density of hydrogen atoms on a passivated Si(100) surface is about 6.8 nm^{-2}. Conversion of 1-nm^3 bulk Si into SiO_2 requires ionization of 100 O atoms. Although the resolution possible with electroless metallization of SAM's is not going to be as good as achievable with hydrogen desorption, if resolution is determined by device architectures it does not need to be.

This speed advantage is strengthened when dissociation cross sections are considered. The cross section for hydrogen desorption from passivated silicon reaches an efficiency maximum of 4×10^{-7} nm^2 at about 6.5 eV [72]. Although the corresponding cross section for a Cl functional group on a SAM has not been measured, it may be possible to estimate it from the electron dissociative attachment (i.e., low-energy electron induced fragmentation) cross section of gaseous monochloroethane, $1–3 \times 10^{-5}$ nm^2, at about 1.6 eV [73]. The cross section for production of Cl^- from chlorobenzene is even higher, 2×10^{-3} nm^2 at 0.8 eV [74]. This dramatic increase is largely related to a favorable interaction between the terminal halide and unsaturated bonds nearby in the spacer part of the molecule [74]. The ambient high-electric field under an STM tip will likely have a strong enhancement effect on dissociation rates.

As stated above, the terminal group largely determines exposure threshold voltage. The low voltage threshold for fragmentation of monochloroethane corresponds with our experience of a threshold below 2 V tip bias for Cl-terminated SAM's [60]. We have observed that a film with an $NH(CH_2)_2NH_2$ termination (PEDA) exhibits a voltage threshold of approximately 5 V. This is in agreement with a higher dissociative attachment threshold for production of NH_{2-} from NH_3 at 5.5 eV [77]. The cross section for this reaction is 1.5×10^{-4} nm^2, suggesting that this material may exhibit a dose threshold under STM exposure even lower than Cl-terminated SAM's. Despite the loss of resolution due to operation at a higher bias [77], a voltage threshold greater than two may be a useful thing as it allows imaging on semiconductors without exposing the resist. Hydrogen-terminated SAM's generally require a 10 V threshold [62]–[65], which again corresponds rather well to production of H^- from CH_4, which begins at about 9-eV incident electron energy [78].

B. Massively Parallel Proximal Probe Systems

Lithography is the enabling technology for the continuing trend toward smaller and higher density electronic components. Up to this time and for the next few years, tools based on high energy e-beams are used to pattern the mask which is reproduced through one of various optical technologies onto many target wafers. The pattern so defined is further processed through etching, implantation, deposition, etc. However, it is not expected that this practice will be feasible for very much longer as dimensions shrink beyond the imaging capabilities of realizable light sources and optical components. Of course, e-beams and focused ion beams are more than capable of sub-100-nm performance, and so a continued role in research and development is assured. Nevertheless these are serial writers, and they generally do not have the throughput needed for cost-effective industrial "direct write" production; even mask-making is becoming difficult [79]. Parallel writing implementations are under development [80], [81], but it is not clear that they will solve various technical problems with the optical system and the mask. The small and compact nature of proximal probes has led to the speculation that a large number of them may be integrated into a single tool, achieving a dramatic increase in throughput [82]–[85]. Considerable progress has, in fact, already been made in this area in terms of developing miniaturizable probes [86], high-speed probes [87], [88], and parallel probes [27].

Pease has discussed some of the performance requirements of a PPL system [82]. He has pointed out that if one considers such a system to have a 10-nm pixel size (comparable to the best results so far of viable high-speed patterning technologies) and 10^4 parallel tips, all writing together, a pixel *rate* of 500 MHz is needed to expose 5 cm^2 s^{-1}. However, this requires a scanning speed of 5 m s^{-1}, which is an extreme challenge for proximal probe systems due to resonance frequency limitations and finite surface roughness and ambient vibrations from a high-speed stage [85]. Consequently, while massively parallel probe arrays remain an attractive candidate for high-throughput nanolithography, many technological barriers must be overcome before this technology can be successfully implemented.

V. SUMMARY

Over the past few years much progress has been made in the development of proximal probes for use as a nanolithography tool. AFM/STM anodic oxidation combined with selective etching provides a simple, reliable process for fabricating nanostructures and nanometer-scale devices. In addition, this oxidation process combined with *in situ* electrical measurements can be used to directly pattern

metal/oxide devices with feature sizes well below 10 nm and in some cases down to atomic dimensions. Such control is allowing the exploration of new classes of devices which are based on lateral metal/oxide tunnel junctions. Another promising approach to PPL is the use of SAM's. Such films offer the potential for high-speed exposure as well as practical functionality, such as serving as templates for metal growth. Such high-speed processes combined with parallel arrays of microfabricated proximal probes offer the potential for a unique, high-throughput nanolithography tool.

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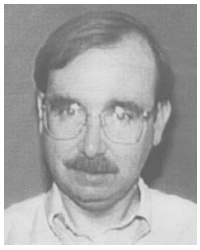
Eric S. Snow received the Ph.D. degree in solid-state physics at the University of North Carolina at Chapel Hill in 1986.

From 1986 to 1987, he was a National Research Council-Naval Research Laboratory Post-Doctoral Associate. He became a permanent member of the research staff at the Naval Research Laboratory in 1987. He is a research physicist in the Electronics Science and Technology Division of the Naval Research Laboratory in Washington, DC. His research specialty is nanostructure science and technology and includes such areas as proximal probe-based nanofabrication, nanoelectronic devices, and near-field optical studies of quantum dots.



Paul M. Campbell received the Ph.D. degree in physics from the Pennsylvania State University, University Park, in 1980.

In 1979, he joined the General Electric Corporate Research and Development Center in Schenectady NY, where he performed research on III–V materials, processes, and devices. In 1985, he became a Research Physicist in the Electronics Science and Technology Division of the Naval Research Laboratory, where he has performed research on the electronic and optical properties of semiconductor heterostructures and nanostructures. Most recently he has pursued the use of proximal probes such as the STM and AFM for the fabrication of nanostructures. He has published more than 50 journal articles and presented numerous invited and contributed talks at international conferences in these fields as well as contributing frequently to the scientific literature and occasionally to its proliferation.

F. Keith Perkins received the B.S. degree in physics from the Massachusetts Institute of Technology, Cambridge, in 1982. He received the M.S. and Ph.D. degrees from the University of Wisconsin-Madison in 1988 and 1992, respectively.

He came to the Naval Research Laboratory, Washington, DC, on a National Research Council Fellowship, where for three years he investigated applications of the scanning tunneling microscope in nanolithography. He has published several papers based on this and other novel nanolithographic technologies. He is presently employed at the NRL, where in addition to his earlier work, he is now developing tools for use in high performance e-beam lithography.