# Silicon Carbide FETs for High Temperature Nuclear Environments

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### *Abstract*

SiC transistors can operate at very high temperatures and survive very high radiation doses. These characteristics make SiC potentially the ideal technology for nuclear power applications. In this paper we report, for the first time, on the active in-core irradiation of 6H-SiC depletion-mode junction field-effect transistors (JFETs) at 25° and 300°C in a nuclear reactor operated at 200 kW. No significant degradation in the device characteristics was observed until the total neutron fluence exceeded $10^{15}$ n/cm$^2$ for irradiation at 25°C, and no significant changes were observed even at $5 \times 10^{15}$ n/cm$^2$ at 300°C. The results of this experiment may also indicate exciting evidence for the anneal of neutron displacement damage for devices irradiated at 300°C.

## I. Introduction

Silicon carbide (SiC) is a very promising semiconductor material for the development of electronics that will operate at high temperature [1,2]; it has the additional advantage that for some applications it should be less sensitive to radiation than Si or GaAs. There will be advantages to eventually using SiC to build very radiation-resistant, high-temperature circuits, which could be located near or within severe radiation environments. System benefits would come from development of amplifier and multiplexer circuits for sensor and control functions which operate at 500° to 600°C. The goal of our research is to demonstrate that high-temperature radiation-hardened devices can be developed and ultimately to deomonstrate circuit operation in these severe environments.

In this paper we report, for the first time, on the in-situ operation of state-of-the-art SiC junction field-effect transistors (JFETs) at high temperature within the core of an operating nuclear reactor. These devices represent the current state-of-the-art but do *not* represent the limits of operation of SiC semiconductor devices. This work was in fact carried out to increase our understanding of the device characteristics so as to allow the design of new SiC devices and circuits that could meet the extremely stressful requirements of nuclear power systems.

## II. SiC Device Description

The design of the JFET devices, fabricated by Cree Research, Inc. (see cross-section in fig.1), used Al-doped *p*-type substrates ($2 \times 10^{16}$ cm$^{-3}$) as the gate. A *p*+ epitaxial layer was grown on the substrate with a thickness of 3 µm and a doping level of $2.2 \times 10^{18}$ cm$^{-3}$. The nitrogen-doped *n*-type conducting channel layers were grown 0.45 µm thick and doped to $1.2 \times 10^{17}$ cm$^{-3}$. A thin (0.2 µm) *n*+ epi-layer was then grown on top with a doping density of $2 \times 10^{19}$ cm $^{-3}$. Through reactive ion etching in $NF_3$, a mesa was etched down on the buried p-type layer to confine the current. Then a fine line trench (1 mm × 5 µm) was etched across the mesa that cut through the top *n*+ layer and down to the desired depth in the *n*-type conducting channel, thus defining the actual channel length of 5 µm and a channel depth of 0.32 µ m. The wafer was thermally oxidized to a thickness of ~200 Å to passivate the surface. The Ni source and drain contacts were deposited and patterned on either side of the trench, and the gate contact metal, an Al alloy, was deposited on the back side of the wafers to form the gate contact. Finally, the ohmic contacts were annealed at high temperature.

Each device was mounted on a TO-46 header. The devices were "scrubbed" to the heated header with a AuGe preform. Scrubbing ensured a good mechanical contact for the gate connection. Device contacts were then connected to their pins using a eutectic wire bonder and a 1-mil Au wire. The devices were hermetically sealed in a dry nitrogen atmosphere so as to help prevent oxidation of the source/drain electrodes during high-temperature operation. The present packaging and metallization limit long term testing to 300°C.

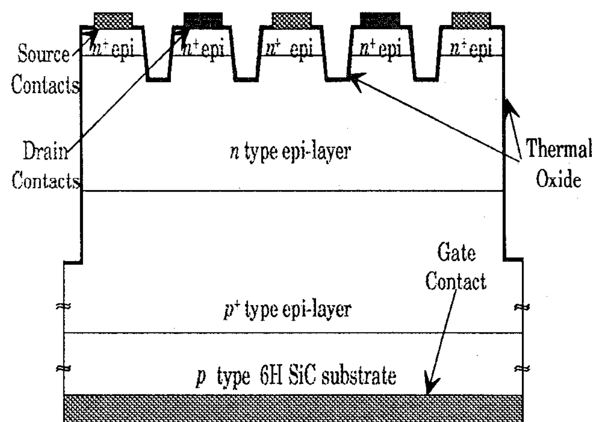


Figure 1. Cross-sectional design of 6H-SiC FET.

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## III. DEVICE ELECTRICAL CHARACTERIZATION

The drain current ($I_{ds}$) versus drain-to-source ($V_{ds}$) and gate ($V_{gs}$) voltages were measured before, during, and after the active reactor irradiation for a series of temperatures between room temperature (RT) and 300°C. From these measurements, values for the threshold voltage ($V_t$), transconductance ($G_m$), and drain saturation current ($I_{dss}$) were obtained. $V_t$ was extracted from the data using the $I_{ds}$ vs $V_{gs}$ curve, in which the slope of the square root of the curve was extrapolated to the $x$-axis, and the threshold voltage $V_t$ defined as the $x$ intercept. $V_t$ is the externally applied gate voltage required to achieve pinch-off. The pinch-off voltage ($V_{po}$) is related to $V_t$ via $V_{po} = |V_t| + V_{bi}$, where $V_{bi}$ is the built-in potential at the $p^+n$ gate junction in the channel region. The $V_{bi}$ for these devices changes 1.8 mV per degree Celsius above room temperature. $G_m$ is defined as the maximum transconductance evaluated at $V_{gs} = 0$ V. $I_{dss}$ is defined as the average value of the drain current in the saturation region for $V_{gs} = 0$ V.

The typical RT current voltage characteristics for the depletion-mode JFETs used in this study are shown in Fig. 2 for several values of gate voltage. The saturated drain current shown in Fig. 2 for $V_{gs} = 0$ V is approximately 40 mA, but some small number of the FETs had $I_{dss}$ values greater than 100 mA. The SiC JFETs for this experiment were selected from a lot of 200 packaged parts. The average RT device characteristics for this lot of JFETs are $G_m = 8.01 \pm 1.91$ mS, $I_{dss} = 37.5 \pm 13.8$ mA, and $V_t = -8.23 \pm 2.26$ V. The variation in device characteristics is attributed to the variations in epi growth thickness, epi-layer doping, and etching of the fine-line trench that defined the channel region in the JFETs. Such process variations are not atypical, as these samples are early development hardware.

Figure 3 illustrates the results of our temperature characterization. This figure shows $I_{ds}$ versus $V_{ds}$ curves at $V_{gs} = 0$ V for a series of temperatures between 23° (RT) and 400°C. The RT threshold voltage for this device was -8.8 V, with a corresponding pinch-off voltage of 11.5 V, transconductance of 8.0 mS/mm, and saturated drain current of 39 mA. We note that $I_{dss}$ (as measured well above threshold, e.g., at $V_{ds} = 20$ V) decreases monotonically from 39 mA at 23°C to 17 mA at 400°C, a drop by a factor of a little over two. However, it is clear that good, clean transistor action is obtained throughout the temperature range of RT to 400°C for these SiC JFETs; these devices have been shown to demonstrate near-ideal behavior throughout this temperature range [3,4].

Elsewhere [5], we reported on a study in which 15 JFETs (of the same lot as those reported on here) were subjected to 1000-hour electrical stress tests at 300°C. Each of three test groups of five JFETs were subjected to a different bias condition: (a) unbiased (control group), (b) dc-biased at $I_{dss}$= 2 mA, and (c) dynamically biased with devices modulated from full-on ($I_{ds\,s}$= 30 mA) to full off at a 1-kHz rate and 50-percent duty cycle. Figure 4 gives the group average change in extracted device parameters ($V_t$, $G_m$, and $I_{dss}$ as defined previously) as a function of time at 300°C for the most stressing condition: dynamic bias. Values in this figure are normalized to the 0 hour 300°C measurements. Surprisingly, these devices show only about a 4-percent decrease in $V_t$ and $G_m$ and a 10-percent decrease in $I_{dss}$. Note that these effects approach saturation at 200 hours with little change during the rest of the 1000-hour life test.

During these temperature studies, the zero temperature coefficient (ZTC), a temperature-independent bias point, was identified for these devices for operation in the saturation region. We have demonstrated that, for properly pretreated devices, this ZTC can be exploited in the circuit design to provide stable operation of a JFET amplifier from 25° to 300° C [6].

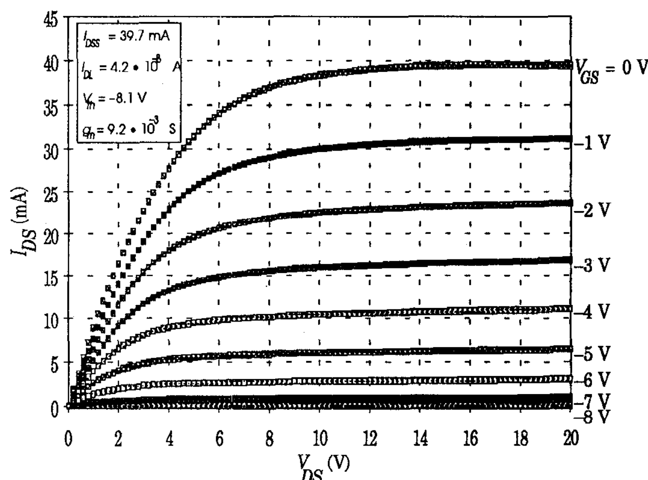


Figure 2. *I-V* characteristics of the JFET described in figure 1.

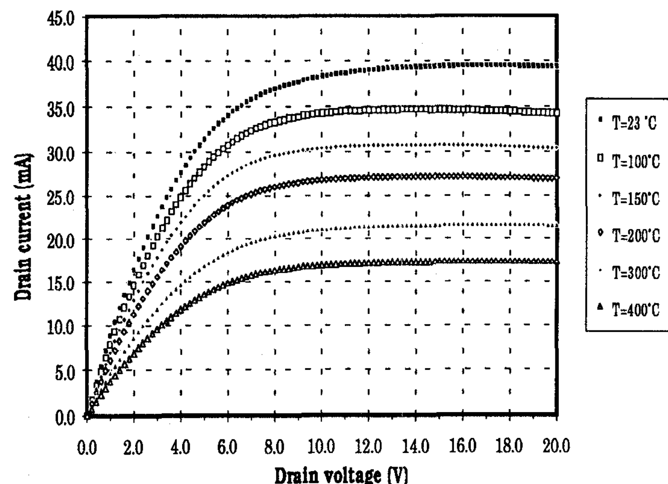


Figure 3. Id-Vd as a function of temperature for Vg = 0 V for SiC JFET described in figure 1.

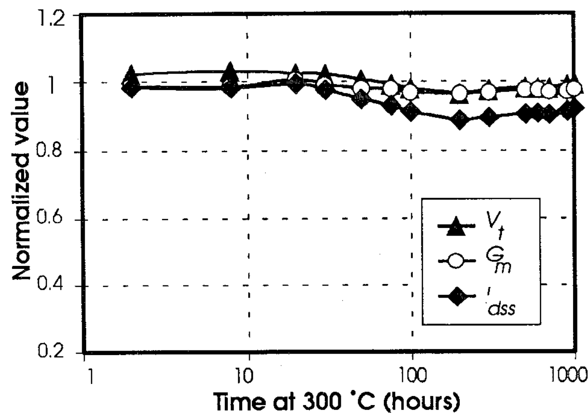


Figure 4. Average change in device characteristics vs. time at 300° C for dynamically biased JFETs.

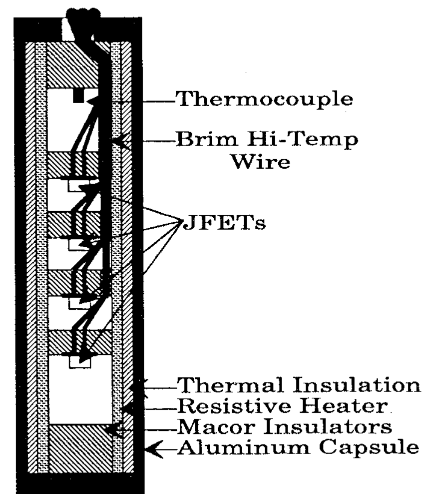


Figure 5. Schematic of irradiation test fixture.

## IV. DESCRIPTION OF NUCLEAR REACTOR EXPERIMENT

A series of active SiC JFET radiation experiments was performed at the Maryland University Training Reactor (MUTR), where measurements of in-situ device radiation response were made during continuous reactor operation. The MUTR is a 250-kW open-pool TRIGA reactor that has five test facilities which includes a 1-in. ID delivery tube, which is part of a pneumatic sample transfer system that allows in-core sample irradiation. This tube was used to gain access to the reactor core for this set of active experiments. The typical fast (>10 keV) neutron flux and gamma dose rate at the in-core rabbit test location are $8.0 \times 10^9$ n/cm$^2$-kW-s and 19 rad (Si)/kW-s, respectively, which at full power (250 kW) provides an environment of $2.0 \times 10^{12}$ n/cm$^2$-s and 4.7 krad (Si)/s gamma.

To achieve our key objective of making in-situ measurements at high temperature, we developed a test fixture that could maintain the devices at temperatures of greater than 300°C while providing electrical insulation currents of at most a few nanoamps. This fixture also had to slip easily within the 1-in. ID delivery tube for insertion into the reactor core. Figure 5 is a schematic of the 0.98-in. OD by 6.25-in. long test fixture. A cylindrical high-temperature ceramic Globar® power resistor was used as the heater. This resistor is encased in an aluminum silicate insulation and pressed into a thin-walled aluminum tube. Although thin, the insulation is effective; about 40 W of power maintains an internal temperature of 300°C with the outer tube at RT. The transistor sockets/insulators are made from Macor®, a glass-ceramic, which is machineable with ordinary metal working tools, into which are inserted plug-in receptacle pins. Electrical connections to the sockets are made via a high-temperature wire obtained from BRIM Electronics (Fair Lawn NJ); the wire is spot welded to the pins. Although the electrical insulating materials were carefully selected on the basis of tests, they provided only a small margin in regard to leakage currents at 300°C; we monitored leakage during the tests by measuring the current to a transistor header pin that was not connected within the transistor package but was otherwise connected to and instrumented the same as the "active" pins. This pin suffered the same header leakage, socket leakage, and connecting wire leakage as the transistor pins. Note that signal wires could not be allowed to electrically contact the interior of the heating resistor because the ceramic from which it is made has considerable electrical conduction at high temperature. The thermocouple was connected to a typical commercially available temperature indicator/controller, which switched the dc power applied to the 18-ohm resistor to maintain a temperature of 300° ± 3° C during the high-temperature irradiation.

Eight devices were used in these active experiments; four devices were irradiated at the same time at each of two temperatures, ambient and 300°C. The test-fixture geometry for both the ambient and 300°C irradiations was identical and contained a device package with the spare pin instrumented, as discussed above, which also provided a measure of the radiation induced-current along the instrument cable and within the device package during the exposure.

The devices in both the ambient and 300°C test groups were biased at $V_{ds}$ = 5 V and a $V_{gs}$ value that would provide an $I_{dss}$ of about 300 μA. This is a typical bias that would be applied to devices during use as logic gates in a high-temperature multiplexer circuit. Before the test, all devices were subjected to a 200-hour unbiased prestabilization bake at 300°C followed by a 160-hour burn-in (at 300°C) under the same bias condition as was applied to the devices during the active irradiations.

Device measurements were made at logarithmic intervals of accumulated fluence between $1 \times 10^{13}$ and $5 \times 10^{15}$ n/cm$^2$ with the reactor under continuous operation see fig.

6). So that the exposure times would be long enough for accurate measurements to be made at each neutron fluence, the nuclear reactor power level was changed several times during the experiment. The final maximum power level at which most of the neutron fluence was accumulated was 200 kW. The devices in the ambient temperature test group experienced irradiation temperatures ranging from 22° to 40° C depending on the reactor power level.

Device characteristics were measured by PC-controlled HP 4145A semiconductor analyzers, one for each of the four devices being simultaneously tested. The control program kept the devices under a dc bias most of the time, periodically "sweeping" the bias conditions (gate-to-source voltage, drain-to-source voltage) and measuring gate and drain currents. The sweeps covered a limited number of data points in the operating regions of interest, both to limit electrical stress on the test devices and to avoid substantial differences in time (and accumulated dose) between first and last points of a set. $I_{ds}$ vs $V_{ds}$ sweeps with $V_g$ = 0 V, including higher source currents, were made for parameter extraction. Frequently, we manually inspected the accumulated data to identify trends in device characteristics (as a result of accumulated dose and temperature); and we made adjustments, when necessary, to keep the devices in the desired region of operation.

## V. Results

Typical in-situ $I_{ds}$-$V_{ds}$ characteristics as a function of neutron fluence for two devices irradiated under bias (one at ambient temperature and the other at 300°C) are presented in

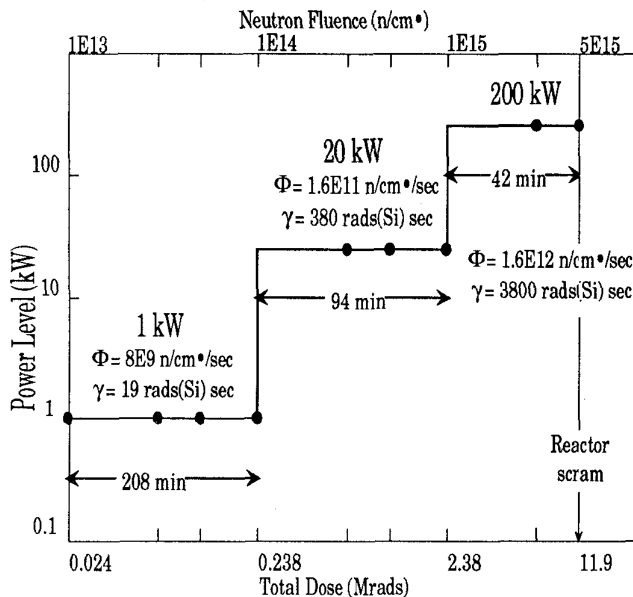


Figure 6. MUTR Experimental Sequence. Solid circles on chart denote device measurement periods and are plotted against irradiation time at each power level with the associated accumulated neutron fluence and total dose.

figures 7a and 7b. In this figure, the $I_{ds}$-$V_{ds}$ characteristics are given for $V_{gs}$ = 0 V. For the device irradiated at ambient temperature (Fig. 7a), there is a slight initial increase in $I_{dss}$ of several percent above the pre-test $I_{dss}$ at low accumulated fluence (<1 × $10^{15}$ n/cm$^2$), followed by a significant reduction in current to about only 36 percent of the pre-test value at the maximum fluence of 5 × $10^{15}$ n/cm$^2$. The small initial increase in $I_{dss}$ was noted earlier for devices tested passively at RT and was ascribed to the influence on the conducting channel of positive trapped charge in the 200-Å thermal oxide passivation layer covering the trench that defines the channel for the device (Fig. 1) [7]. The dramatic 60-percent decrease in saturation drain current is a direct result of the effects of the neutron induced displacement damage on channel carrier mobility and concentration.

The typical in-situ response for devices irradiated at 300°C is given in fig. 7b; the pretest RT curve is included for reference. This figure shows the pre-irradiation characteristic 50-percent decrease in $I_{dss}$ between RT and 300°C for these SiC JFETs at the 1 × $10^{12}$ n/cm$^2$ fluence. Under irradiation there is an initial slight enhancement of $I_{dss}$ at 1 × $10^{14}$ n/cm$^2$ followed by less than a 6-percent decrease in $I_{dss}$ overall at the maximum fluence of 5 × $10^{15}$ n/cm$^2$. These drastically different responses in irradiated samples at different temperatures have been noted following passive exposures of SiC JFETs at ambient temperature and have been shown to result from the difference in the impact of the neutron-induced defects on the carrier removal and mobility at the two temperatures [7,8].

Figure 8a and 8b gives analyses of the in-situ measurements for the device test groups irradiated at ambient and 300°C. This figure presents the relative group average change in extracted device parameters as a function of fluence and normalized to the pretest RT values, for the four devices tested at each temperature. Also included in this figure are the extracted parameters from posttest measurements made the day after the reactor exposure with the devices at their respective test temperatures. The devices were stored at RT in the reactor pool away from any significant radiation field after termination of the active irradiation, until the posttest measurements were made.

For the active irradiation at RT, figure 8a shows very little change in device characteristics out to 1 × $10^{15}$ n/cm$^2$ accumulated fluence, at which point the $I_{dss}$ and $G_m$ have degraded about 10 percent; these values are in reasonable agreement with previous passive irradiations. But the end-point measurements made at 5 × $10^{15}$ n/cm$^2$ with the reactor still under power show significantly less degradation in the device characteristics than expected based on previous passive irradiations at RT [7]. However, the posttest measurements made 24 hours later after the irradiation was terminated show a significant decrease (25 percent) in $V_t$ with the corresponding decreases in the $I_{dss}$ and $G_m$ to values that are in very good agreement with our previous passive radiation experiments. To explain the result that there is less degradation in device parameters with the reactor

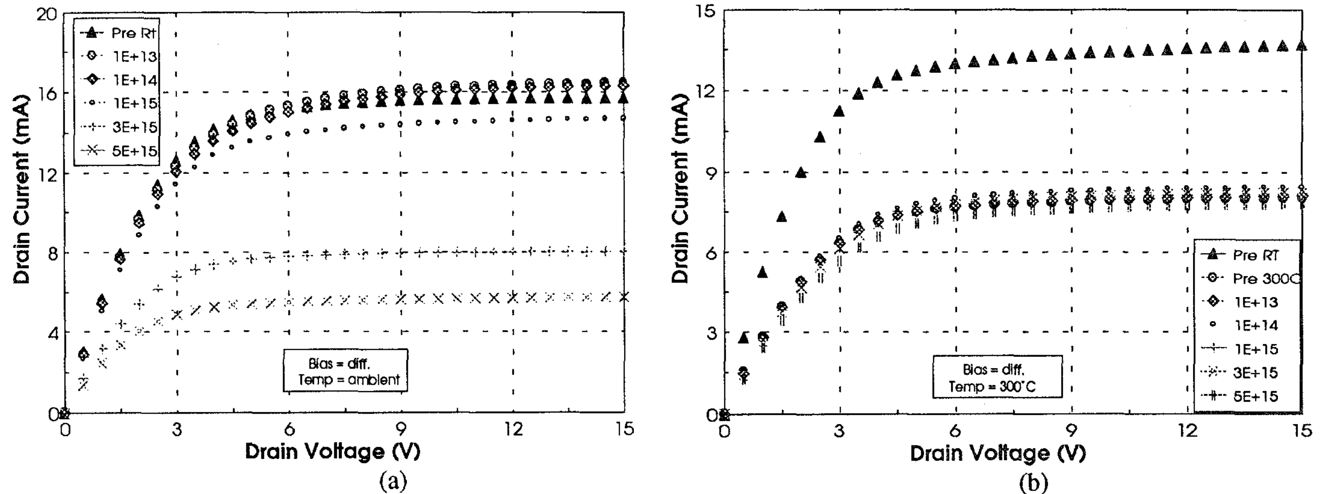


Figure 7. Typical in-situ measured $I_{ds}$-$V_{ds}$ characteristics ($V_g$ = 0 V) for 6H-SiC JFETs as a function of neutron fluence for devices irradiated under bias (Vds = 5 V, Idss = 350 μA) at RT (a) and at 300°C (b).

operating, we suggest that there is a positive charging of the passivation oxide, which is in contact with the back of the conducting channel, arising from ionizing radiation effects; but this a much larger effect than noted in earlier passive irradiations because of the applied fields in the active devices. The final values after 24 hours we believe agree because these ionizing effects anneal out over time.

The characteristic initial increase in $V_t$ and decrease in $I_{dss}$ and $G_m$ resulting from raising the device temperature from RT to 300°C is shown in Figure 8b at the $1 \times 10^{12}$ n/cm$^2$ fluence. This figure shows degradations in $I_{dss}$ and $G_m$ of less than 20 percent as opposed to the greater than 60-percent degradation shown in figure 8a for the devices irradiated and measured at RT. From our previous analysis for device operation at 300°C you would expect to see considerably less degradation in $I_{dss}$ and $G_m$ characteristics as a result of neutron irradiation than you would for device operation at RT. We conclude that since the carrier mobility is already so severely degraded due to the thermal phonon scattering at 300°C, the additional scattering due to the neutron-induced charged trap states has very little impact on mobility. (Therefore, carrier removal should be the primary effect from the neutron irradiation observed for device operation at this temperature; the effect of carrier removal is also less severe at 300°C due to the additional ionization of carriers at this temperature.)

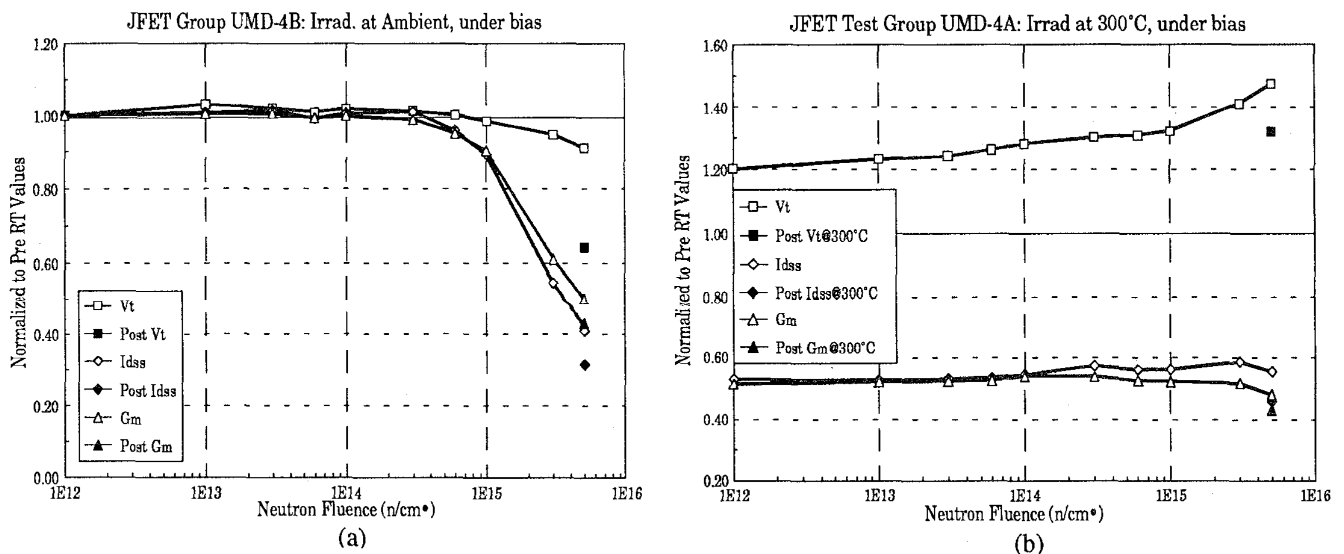


Figure 8. Relative group average change in extracted device parameters as a function of fluence and normalized to the pretest RT values for the four devices irradiated under bias at RT (a) and at 300°C (b). In-situ and post test measurements are presented.

Figure 8b also shows a continuing slow increase in $V_t$ with the neutron fluence, resulting in a maximum end-point value at $5 \times 10^{15}$ n/cm$^2$ that is about 25 percent larger than the pretest value. As suggested previously [7], the pinch-off voltage ($V_p$) should be constant with neutron fluence at 300°C, since we concluded that at that temperature, thermal detrapping of electrons trapped in the neutron-induced deep-level traps in the depletion region completely empties these traps. There should be no effect on $V_p$ which depends on the channel doping density ($N_D$) and the physical characteristics of the device and we recall that $V_p$ is related to $V_t$ by the relation $V_p = |V_t| + V_{bi}$ where $V_{bi}$ is the built-in potential at the $p^+n$ junction. During the exposure we believe that with the applied bias between the source and drain and a competition between charge generation in the 200Å oxide and annealing of charge at 300°C, the balance between the two competing processes increases the net positive charge until the reactor is turned off. This could explain the continued increase in $V_t$ with gamma dose and neutron fluence shown in Fig. 8b while under reactor power and the decrease in $V_t$ (and the associated decreases in $I_{dss}$ and $G_m$) in the posttest with the reactor power off.

It is important to note here that the posttest parameter values shown in Fig. 8b, for the devices irradiated at 300°C, indicate less degradation from the reactor exposure than noted in our previous experiments, where devices were passively irradiated at RT and measured at 300°C. Further, when the temperature on these devices was decreased to room temperature (where we would have expected the results to agree with the posttest measurements in figure 8a for the devices irradiated at ambient temperature), we found that the devices irradiated at 300°C show significantly less degradation. These results, given in table 1, would imply that the damage was less severe for devices irradiated at 300°C than at ambient temperature. We also note that the posttest $V_t$ measurement in figure 8b may indicate the presence of some permanent trapped charge within the passivation oxide, which would tend to increase the device parameters, as discussed previously. But at most this effect would account for less than half the difference between the parameter degradations that are shown in table 1 for the two JFET test groups.

Table 1

Group average change in parameters measured at RT for 6H-SiC JFETs after accumulated fluence of $5 \times 10^{15}$ n/cm$^2$ and gamma dose of 12 Mrad. Values are normalized to the pretest RT measurements.

| Device Parameters | Posttest /Pretest ratio after Irradiation, measured at RT | | | |
|---|---|---|---|---|
| | Irradiated at Ambient | | Irradiated at 300C | |
| | Avg | Stdev | Avg | Stdev |
| $V_t$ | 0.64 | 0.03 | 0.88 | 0.03 |
| $G_m$ | 0.43 | 0.09 | 0.66 | 0.05 |
| $I_{dss}$ | 0.31 | 0.05 | 0.57 | 0.01 |

## VI. Summary

This preliminary study has clearly shown that SiC FETs offer advantages over Si or GaAs FETs for nuclear applications at high temperature. The transistors used in this study were limited in application to 300°C because of the particular metallizations used for source and drain contacts. In the nuclear reactor environment, the devices (and circuits, we expect) are less sensitive to radiation when operated at high temperature.

Recent work has yielded a refined physics model for the JFET that takes into account both the temperature and radiation response of SiC [7]. Based on this model and the radiation response discussed above, it could be concluded that redesigned devices with increased channel doping density ($10^{18}$ cm$^{-3}$ ) would be capable of operating after exposures of $10^{16}$ n/cm$^2$ at room temperature and $10^{17}$n/cm$^2$ at 300°C.

Additional radiation experiments are required to confirm and quantify the extent of the annealing of neutron displacement damage that may occur at temperatures as low as 300°C, as indicated by the results of this experiment. Such behavior would significantly extend the neutron tolerances of SiC devices beyond the $10^{17}$n/cm$^2$ fluence mentioned above, especially for device operation at 400° to 500°C.

Further improvements could also be made by investigation of alternative passivation for the SiC surface to replace the thermally grown $SiO_2$. Of course, long-term operation at 400° to 500°C is a very significant challenge for the semiconductor technology and the packaging.

## VII. Acknowledgment

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