

A Methodology for the Identification of Worst-Case Test Vectors for Logical Faults Induced in CMOS Circuits by Total Dose

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Abstract

A new methodology was developed for the identification of the worst-case combination of irradiation and postirradiation test vectors. The methodology significantly simplifies total-dose testing of CMOS VLSI devices. It also provides more accurate assessment of failure levels for such devices.

I. INTRODUCTION

A test vector is a combination of inputs to the circuit under test that meets two requirements: first, the test vector must excite a fault, and second, it must be able to propagate the fault so that it can be observed at the primary outputs of the circuit under test [1].

According to the above definition, both the irradiation bias and the postirradiation test vectors used in total-dose testing of digital very-large-scale-integration (VLSI) circuits can be considered test vectors if they contribute to the excitation and the observability of faults induced by total dose. However, there has been no effort to relate the selection of irradiation test vectors (ITV's) and the postirradiation test vectors (PTV's) to the excitation and observability conditions of logical faults induced in complementary metal-oxide-semiconductor (CMOS) circuits by total dose. Input vectors (irradiation and/or postirradiation) that do not fulfill those conditions do not detect faults induced by total dose, and may result in a misleading assessment of failure levels.

Although the total-dose testing standard, MIL-STD-883, method 1019, emphasizes the use of worst-case test vectors, they are typically not used in total-dose testing of VLSI devices. That is because there is no practical methodology to identify worst-case test vectors, especially for complex VLSI circuits [2].

In this paper, we analytically investigate the problem of identifying ITV's and PTV's for CMOS circuits that satisfy the excitation and observability conditions as well as the worst-case conditions. Results are supported by simulations of CMOS circuit behavior under irradiation. The simulation is based on experimental data on the total-dose response of MOS transistors from two technologies, one radiation-hard (P1) and the other radiation-tolerant (P2). Total dose causes inversion of the n-channel under the gate oxide in P1 transistors, and inversion of n-type material under both the gate oxide and the field oxide in P2 transistors.

Our approach is inspired by the approach used for the generation of test vectors to detect faults produced by process defects. We start by performing a comprehensive analysis of

the logic failure induced by total dose in CMOS circuits. Next, we identify all factors contributing to this kind of failure. Then we describe a fault model that we used to simplify the generation of test vectors. Finally, we present a heuristic methodology for the identification of worst-case test vectors.

II. GATE-LEVEL FAILURE ANALYSIS

It is important to understand the gate-level failure mechanism of logic faults induced in CMOS combinatorial circuits containing gates only (no pass transistors). Although total dose degrades MOS transistor parameters, we deliberately choose to perform the failure analysis on the gate level. This will simplify the generation of test vectors, since we increase the level of abstraction of the circuit under test from the transistor level to the gate level.

Previous efforts have addressed the problem of logical faults induced by total dose in CMOS circuits [3,4,5]. However, none of these efforts led to the development of a method which could identify the excitation and observability conditions for the detection of those faults by test vectors.

We start the analysis for the simple case of the CMOS inverter (INV) and then move on to multi-input gates (NOR and NAND gates).

A. Inverter Failure Mechanism

A CMOS inverter consists of a pair of n-device (NMOS) and p-device (PMOS) transistors with their gate electrodes connected together. Typically, input logic 1 is the worst-case irradiation bias condition for the INV. Figures 1 and 2 show the effect of total dose on the voltage transfer characteristic (VTC) of an inverter with different irradiation biases for P1 and P2, respectively. These figures show significant degradation of the VTC of the inverter with irradiation bias at logic 1, $I = 1$, because of total dose, whereas total dose has a relatively insignificant effect on the VTC of an inverter irradiated at bias $I = 0$. A node is defined as the point of connection between a driving gate and a driven gate. The logic value for a node n in Figure 3 is then defined in terms of the output voltage of the driving gate, V_{oh}^a or V_{ol}^a , and the switching voltage of the driven gate, V_s^b , as follows [6]:

$$\begin{aligned} &\text{logic 1 if } V_{oh}^a > V_s^b, \text{ and} \\ &\text{logic 0 if } V_{ol}^a < V_s^b. \end{aligned} \quad (1)$$

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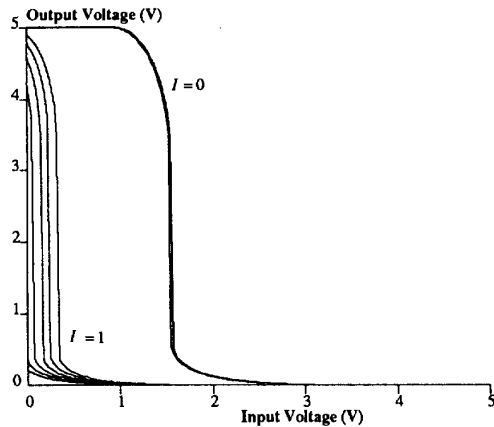


Fig. 1. Total-dose degradation of the VTC's of two inverters: one with $I = 1$ and the other with $I = 0$. Total dose varies from 1.5 to 2.0 Mrads* in steps of 100 krad for P1.

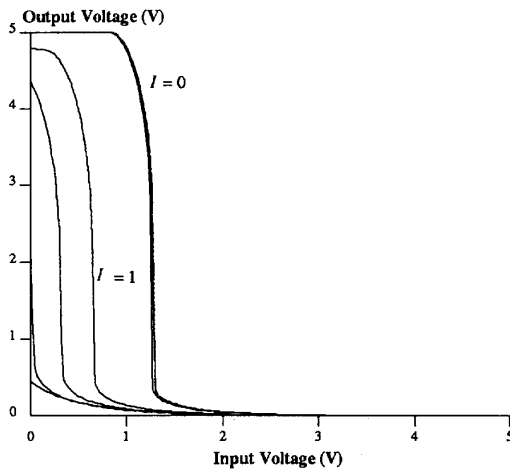


Fig. 2. Total-dose degradation of the VTC's of two inverters: one with $I = 1$ and the other with $I = 0$. Total dose varies from 100 to 250 krad in steps of 50 krad for P2.

From Figures 1 and 2 and Equation (1), a logic failure will be induced at node n if V_{oh}^a of the driving gate is reduced by total dose to a value smaller than V_s^b of the driven gate. This can only happen if the irradiation input of the driving gate is set to logic 1 and the postirradiation input, P , of the driving gate is set to logic 0, as shown in Figure 4. D represents logic 1 before failure and logic 0 after failure. Typically, this notation is used to describe the faulty and the fault-free circuit on the same circuit representation, which simplifies the automatic generation of test vectors [7].

*All total-dose levels are in reference to SiO_2 .

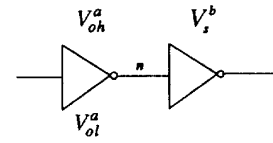


Fig. 3. Two cascaded inverters with node n .

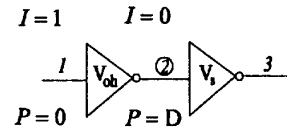


Fig. 4. Two cascaded INV's with total-dose logical failure induced at node 2.

Figures 5 and 6 demonstrate the mechanism of a logic failure induced by total dose at node 2 in the simple circuit of Figure 4 for P1 and P2, respectively. A logical fault will occur in a digital circuit when a node experiences a logic level that is complementary to that which exists at the same node of the fault-free circuit.

The values of V_{oh} and V_s depend on the gain ratio factor of the NMOS and PMOS transistors, $k_r = k_N / k_P$, where k_N and k_P are the gain of the NMOS and PMOS transistors, respectively. The bigger the value of k_r , the smaller the values of V_{oh} and V_s [8].

Therefore, the value of k_r of the driving and the driven inverters will affect the failure level of a node. The bigger the value of k_r of the driving gate, the more sensitive the node will be to failure. Also, the smaller the value of k_r of the driven gate, the more sensitive the node will be to failure. Figure 7 illustrates the effect of k_r on the failure level for P2 as an example.

B. Failure Mechanism of Multi-Input Gates

Multi-input CMOS gates (e.g., NOR, NAND, etc.) are constructed from pairs of NMOS-PMOS transistors whose number is equal to the number of inputs of the CMOS gate. Moreover, a CMOS gate has a unique structure: if the NMOS transistors are connected in series, the corresponding PMOS transistors are connected in parallel, and vice versa, as shown in Figure 8. Because of this structure, the switching operation of the output of a CMOS gate from one logic state to another is carried out by the NMOS-PMOS pairs in a way similar to that of the INV.

However, the excitation conditions of multi-input CMOS gates are more sophisticated than those of the INV. There is more than one input controlling the reduction of V_{oh} of the driving gate and more than one input affecting the stability of V_s of the driven gate. Consider the case where a 3-input NAND gate (NAND3) drives a 3-input NOR gate (NOR3), as shown in Figure 9. We want to analyze the excitation conditions of a target logic fault at node n . Assume that the

irradiation input vector is given by $\mathbf{I} = [101]$ (i.e., $X_1 = 1$, $X_2 = 0$, $X_3 = 1$ during irradiation); then only the first and the third NMOS-PMOS pairs (heavy lines) will cause the failure of the NAND gate, because they were driven by a logic 1 during irradiation. In order to produce a reduced V_{oh} (weak 1) at the output of the driving gate, three conditions must be satisfied. First, at least one of the heavy-line pairs should be excited (EX) as in the case of the inverter, which means that at least one of the pairs should have a 1/0 irradiation/postirradiation input combination. Second, unexcited pairs (fine-line) should ensure a path between V_{DD} and the ground, which means that the series transistors should be ON and the parallel ones should be OFF. Therefore, the second postirradiation input of NAND3 should be 1 for the series NMOS transistor to be ON and the parallel PMOS transistor to be OFF. Third, the postirradiation input vector, \mathbf{P} , must ensure a logic 1 at the output of the driving gate. This means that at least one of the postirradiation inputs must be at logic 0, which is automatically satisfied by the first condition for the NAND gate. Therefore, for $\mathbf{I} = [101]$, \mathbf{P} can take one of three values: $\mathbf{P} = [010]$, $[011]$ or $[110]$.

On the other hand, there are two conditions for the driven gate. First, the $\mathbf{I/P}$ input combination should be selected such that it does not excite another weak 1 (the above three excitation conditions) at the output of the driven gate to avoid the masking of double faults (one at the output of the driving gate and one at the output of the driven gate). Second, \mathbf{P} should be selected to pass the fault to the output of the driven gate as shown in Figure 9.

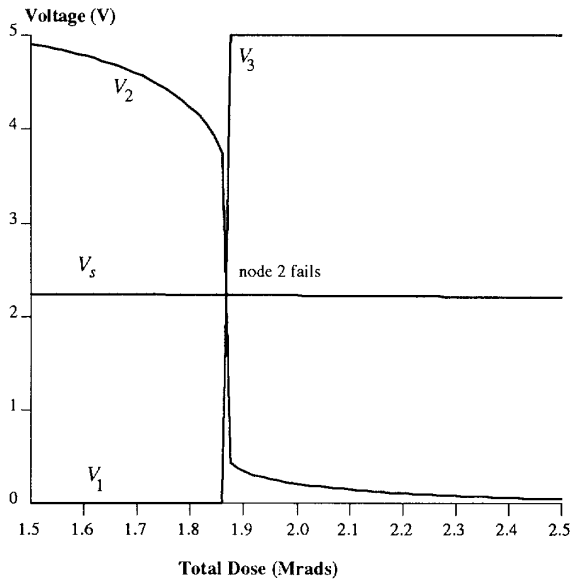


Fig. 5. Logic failure induced at node 2 (Fig. 4) for P1.

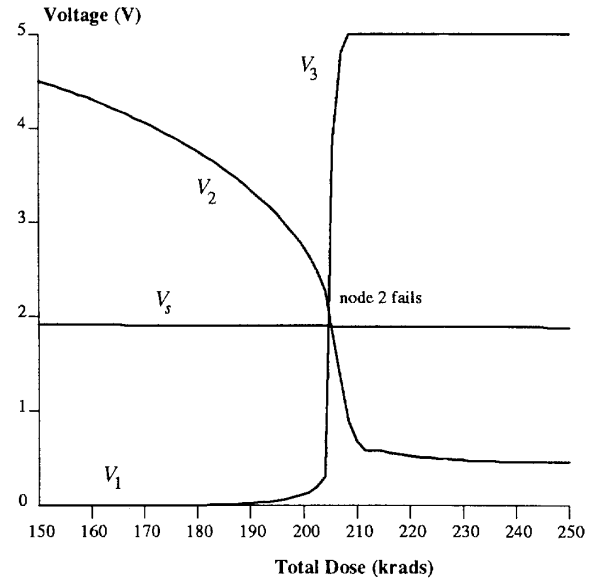


Fig. 6. Logic failure induced at node 2 (Fig. 4) for P2.

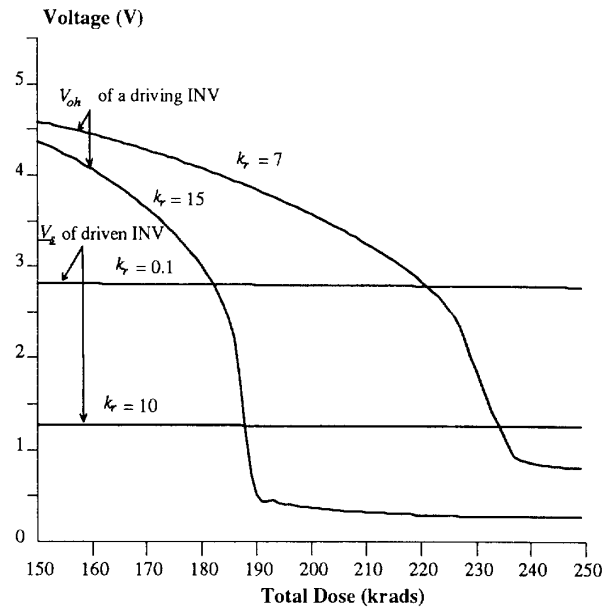


Fig. 7. Sensitivity to total-dose induced failure for INV's with different gain ratios for P2.

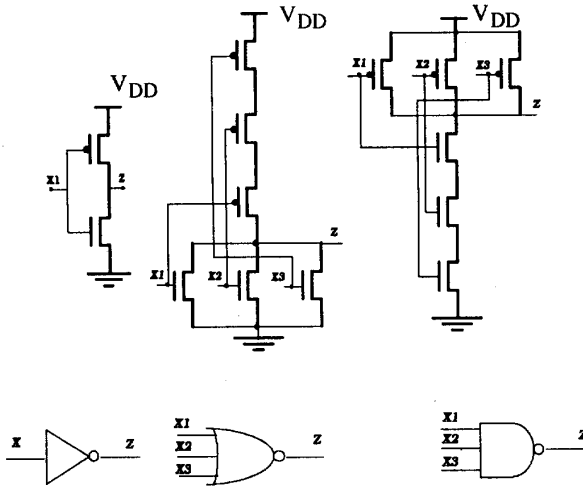


Fig. 8. Transistor-level and gate-level representation.

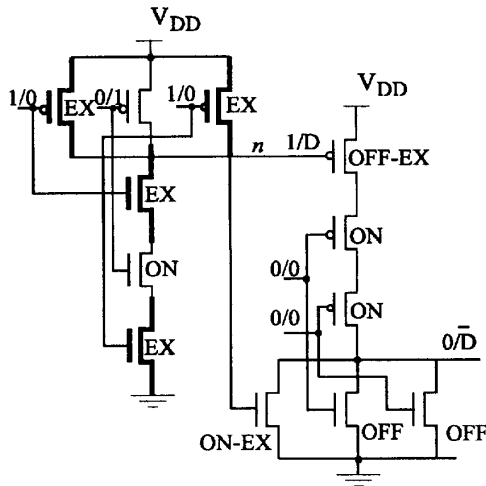


Fig. 9. Example of a NAND3 driving a NOR3 with I and P input vectors for both gates satisfying the excitation conditions for both gates.

Three very important results can be concluded from the above analysis. First, the selection of a postirradiation input vector P that manifests a fault depends on the irradiation input vector I . Therefore, it is more appropriate to refer to these input vectors as combination of input vectors, I/P . Second, the simple stuck-at-0 fault model previously suggested [5] will not be a sufficient representation of logic failure induced by total dose, because this fault model does not require any kind of correlation between I and P . In fact, all that it needs for excitation is at least one of the inputs of P to be at logic 0. Also, according to the stuck-at-0 fault model, there are no conditions required of the driven gate in order for the fault to be manifested. For example, according to the stuck-at-0 fault model, an input vector combination

$[110]/[100]$ applied to NAND3, Figure 9, can excite a fault at node n . In fact, it could not, as we showed earlier. Finally, we showed in the NAND example that we have three possible P 's capable of exciting a fault at the output of the gate given that $I = [110]$. However, the sensitivity of node n to failure for the three input combinations may not be the same. That is because each combination may result in different V_{oh} 's and consequently a different failure level. Thus, one node may have more than one failure level, depending on the combination of the irradiation and postirradiation test vectors exciting a fault at a particular node.

From the above analysis, it is clear that the sensitivity of a node to a failure depends on a number of factors:

I , the irradiation input vector;

P , the postirradiation input vector;

$[W_N/W_P]$, the widths of the NMOS-PMOS pairs assuming equal channel lengths for all NMOS's and PMOS's;

g , the type of CMOS gate; and

m , the number of inputs of the CMOS gate.

Therefore, for a node n , a fault will be excited if and only if

$$V_{oh}^n(d, I_a^n, P_a^n, [W_N/W_P]_a^n, g_a^n, m_a^n) < V_s^n(d, I_b^n, P_b^n, [W_N/W_P]_b^n, g_b^n, m_b^n), \text{ and } (2)$$

$$d \geq FL^n(t_i, t_p),$$

where a and b are subscripts indicating whether the CMOS gate is driving or driven with reference to node n , d is the total-dose level, and $FL^n(t_i, t_p)$ is the failure level of node n when the irradiation and postirradiation test vectors t_i and t_p are applied to the primary inputs of the circuit under test.

An adequate model for the generation of test vectors in CMOS circuits subjected to total dose is shown in Figure 10. Obviously, the model is more than just a gate-level representation of CMOS circuits. It contains all the necessary information required for the calculation of the failure condition as shown in Equation (2). Note that the model simultaneously describes the circuit before and after failure given the irradiation and postirradiation inputs.

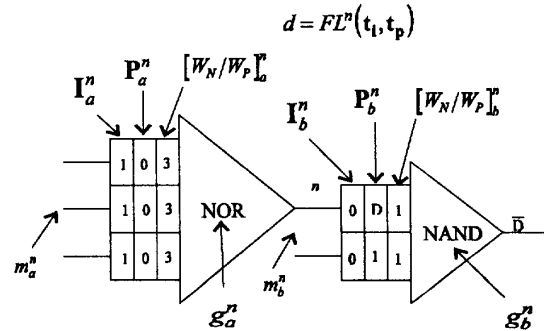


Fig. 10. Circuit model representation for generation of total-dose test vectors.

III. FAULT MODELING

Fault modeling is an abstraction of a failure mechanism at a certain level of circuit representation that is performed to simplify the process of generating test vectors [1]. Bhuva *et al.* modeled the reduction of V_{oh} as an ordinary stuck-at-0 fault at the output of the gate [5]. Apparently, this model is inadequate in representing logic faults induced by total dose as shown in the previous section.

Logic faults induced by total dose can be modeled as a combination of (1) a transistor-level stuck-on fault that occurs to those NMOS transistors that are biased high during irradiation, and (2) a gate-level weak-1 fault model at the output of the gate. This weak 1 becomes a logical fault depending on the switching threshold of the driven gate. We refer to this fault model as rad-weak-1 (RW-1).

A. Excitation Condition Modeling

We focus on CMOS combinational circuits that contain only INV, NOR, and NAND gates. We can restate the three conditions for excitation in terms of the stuck-on and weak-1 fault model as follows:

1. At least one of the stuck-on faults is excited; i.e., at least one 1/0 combination is applied.
2. Those NMOS-PMOS pairs that have no stuck-on NMOS transistors are set so that a connection path between V_{DD} and ground is established. This means that series transistors should be ON, and parallel transistors should be OFF.
3. The weak-1 fault must be excited at the output of the gate; i.e., the postirradiation input of the gate should be set in an attempt to bring the output to logic 1.

The excitation conditions for the different driving gates can be modeled as Boolean functions of the irradiation and postirradiation input combination. E equals 1 only for those input combinations that satisfy the above three conditions, and 0 otherwise. Assuming that $\mathbf{I} = [I_1 I_2 \dots I_m]$ and $\mathbf{P} = [P_1 P_2 \dots P_m]$ are generic irradiation and postirradiation input vectors, then E can be expressed as follows:

$$E_{INV} = (I_1 \bar{P}_1). \quad (3)$$

$$E_{NOR2} = (I_1 + I_2) \bar{P}_1 \bar{P}_2. \quad (4)$$

$$E_{NOR3} = (I_1 + I_2 + I_3) \bar{P}_1 \bar{P}_2 \bar{P}_3. \quad (5)$$

$$E_{NAND2} = (I_1 \bar{P}_1 P_2 + I_2 P_1 \bar{P}_2 + I_1 I_2 \bar{P}_1 \bar{P}_2). \quad (6)$$

$$E_{NAND3} = (I_1 \bar{P}_1 P_2 P_3 + I_2 P_1 \bar{P}_2 P_3 + I_3 P_1 P_2 \bar{P}_3 + I_1 I_2 \bar{P}_1 \bar{P}_2 P_3 + I_2 I_3 P_1 \bar{P}_2 \bar{P}_3 + I_1 I_3 \bar{P}_1 P_2 \bar{P}_3 + I_1 I_2 I_3 \bar{P}_1 \bar{P}_2 \bar{P}_3). \quad (7)$$

Similar functions can model the conditions for the driven gate.

B. Node Sensitivity

Typically, the driven gate has a negligible effect in terms of the failure level of the node, as shown in Figure 7. Thus, the sensitivity of a node to failure can be determined by the driving gate. As shown in Figure 7, the bigger the gain ratio of an INV, the more sensitive the INV will be to a logic fault. Similarly, for multi-input gates with an input combination satisfying the excitation conditions, the sensitivity will be proportional to the equivalent gain ratio. This means that, for a particular input combination satisfying the excitation conditions, a multi-input gate can be replaced with an equivalent inverter having equivalent channel widths (assuming equal channel lengths for all transistors). The equivalent gain ratio can be evaluated (to first-order) by the series and parallel laws for combining conductances [4,9]. Thus, the sensitivity of a node to failure can be expressed as follows:

$$\begin{aligned} S(\mathbf{I}, \mathbf{P})^n &= E_{INV} \times \frac{W_N}{W_P} \\ &= E_{NORM} \times \frac{\sum_{i=1}^m W_N^i}{1 / \sum_{i=1}^m 1/W_P^i} \\ &= E_{NANDm} \times \frac{1 / \sum_{i=1}^m 1/W_N^i}{\sum_{i=1}^m W_P^i} \end{aligned} \quad (8)$$

$i=1 \text{ and } i \text{ is such that } I_i \bar{P}_i = 1$

Consider for example the NAND3 gate shown in Fig. 11. The input combination satisfies the excitation condition of the gate, and the NMOS 1 and 3 transistors are excited, since $I_1 \bar{P}_1 = I_3 \bar{P}_3 = 1$. Thus, the sensitivity is

$$S([101], [010])^n = \frac{W_N^1 W_N^2 W_N^3}{W_N^1 W_N^2 + W_N^2 W_N^3 + W_N^1 W_N^3} \cdot \frac{W_P^1 + W_P^3}{W_P^1 + W_P^2 + W_P^3}.$$

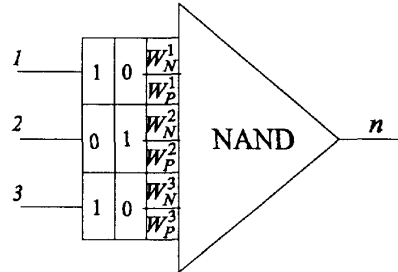


Fig. 11. NAND3 driving gate where RW-1 fault is excited at node n .

C. Observability Condition

In general, a test vector is selected so that it excites a fault and at the same time maintains a clear path for the fault to be propagated to the primary outputs.

For logic faults induced by total dose, two kinds of fault masking might obscure the fault at the primary outputs of the circuit under test. The first, driven gate masking, might occur if the test-vector combination is set so that, at the time of failure, the driven gate has a sensitivity equal to that of the driving gate; in this case, both gates fail at the same time, producing two faults that mask each other, and the failure is not observable at the primary outputs. Circuit CKT1 in Figure 12 shows an example of a test-vector combination that is set to detect an RW-1 fault at node 2; in this circuit, the possibility of driven gate masking was not considered. Circuit simulation of CKT1 is shown in Figure 13. This figure shows that the primary output (node 4), when it is about to change logic (fail), satisfies the excitation condition; however, since nodes 2 and 4 fail at the same level, node 4 remains at logic 0 (no failure).

The second kind of fault masking is multiple-fault masking. Figure 14 shows a test-vector combination for the detection of a target RW-1 fault at node 2. In this circuit, the possibility of multiple fault masking has not been considered. This combination of test vectors also excites another fault at node 3. Since both faults have equal sensitivity, they occur at the same dose level and mask each other. No failure would be observed at the primary output, node 5.

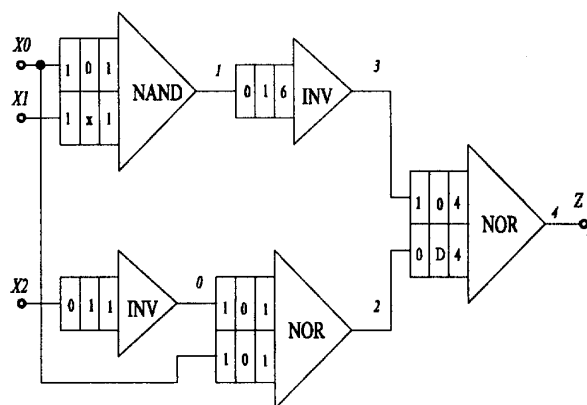


Fig. 12. Masking RW-1 fault at node 2 in CKT1.

Therefore, in the selection of a worst-case test vector combination, we excite a target RW-1 fault of the most sensitive node and propagate the fault to the primary outputs by deactivating nontarget RW-1 faults that might obscure the observability of the target fault at the primary output of the circuit under test. Note that the deactivation of nontarget faults requires violating the excitation conditions. This shows that the irradiation bias is a test vector, since it contributes to the observability as well as the excitation of faults.

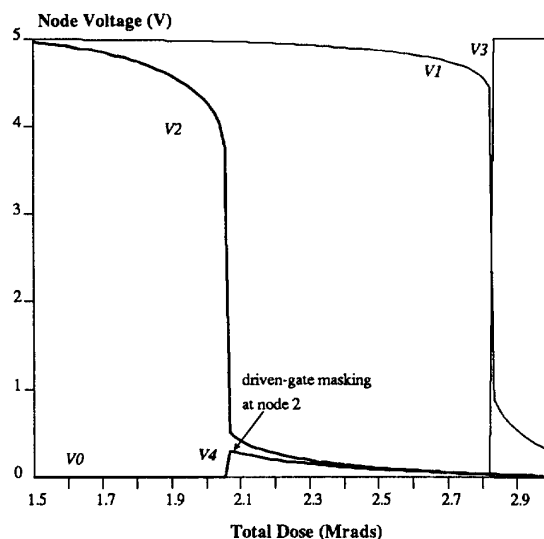


Fig. 13. Simulation of CKT1 with total dose for P1 with driven-gate masking for CKT1 shown in Fig. 12.

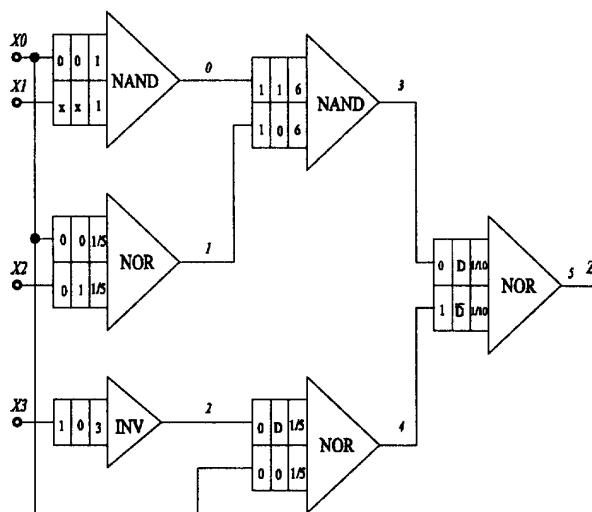


Fig. 14. Circuit CKT2 under conditions that lead to masking of multiple faults for nodes 2 and 3.

IV. WORST-CASE TEST VECTORS

We propose a heuristic search methodology for the identification of worst-case test-vector combination. The objective is to find the most sensitive node and then search for the test-vector combinations that satisfy the excitation and observability conditions of an RW-1 fault at the this node.

However, node sensitivity to failure depends on the applied test-vector combination. To overcome this problem, we use an iterative search methodology. First, we assume the availability of the absolute maximum sensitivity, S_{\max} , at every node. Assuming equal W_N 's and W_P 's within each gate, Equation (8) can be reduced to allow the calculation of S_{\max} as follows:

$$\begin{aligned} S_{\max} &= \frac{W_N}{W_P} \quad \text{for INV} \\ &= m^2 \times \frac{W_N}{W_P} \quad \text{for NOR} \\ &= \frac{1}{m} \times \frac{W_N}{W_P} \quad \text{for NAND} \end{aligned} \quad (9)$$

Nodes are then classified according to their S_{\max} 's. Nodes in the class of the largest S_{\max} 's are considered candidate nodes. We check the availability of test-vector combinations that can result in S_{\max} for the candidate nodes. If there exists only a test vector combination that results in the maximum available sensitivity less than S_{\max} , then we have to check whether the node still belongs to the class of candidate nodes. We repeat the above process until we find a node with maximum sensitivity excited by available combinations of test vectors. This is the worst-case combination of worst-case test vectors, (\hat{t}_i, \hat{t}_p) .

Consider, for example, the CKT3 shown in Figure 15. Node 5 is the candidate node, with $S_{\max} = 20$, because it has the largest S_{\max} in the circuit. To set node 5 to maximum excitation, we must set the input vectors of the driving gate to $I_5^a = [11]$ and $P_5^a = [00]$, and, to avoid the possibility of driven gate masking, we set the input vector of the driven gate to $I_5^b = [00]$. Finally, in order for the RW-1 fault to be observable at the primary output Z2, $P_5^b = [D1]$. There exist test vector combinations that satisfy the above conditions simultaneously. Consequently, $\hat{t}_i \in \{[0100], [0101], [1100], [1101]\}$, and $\hat{t}_p \in \{[0011], [1011]\}$. Simulating CKT3 for all possible inputs (irradiation and postirradiation) assures that the worst-case test vectors are the same as those identified by the above methodology. Another example is CKT4 in Figure 16. Node 4 is the candidate node, with $S_{\max} = 12$. However, there is no primary input combination that excites the node at its absolute maximum sensitivity. The available maximum sensitivity of node 4 equals 6. Therefore, the most sensitive node is node 3, with maximum sensitivity equal to 8. Figure 16 shows the worst-case test-vector combinations that satisfy the excitation and observability conditions for an RW-1 fault at node 3 and at the same time maintain maximum sensitivity at the node.

All test vectors are generated manually in the above examples because of the simplicity of the circuits in the examples. However, the methodology can easily be automated so that test vectors can easily be identified for more complex circuits.

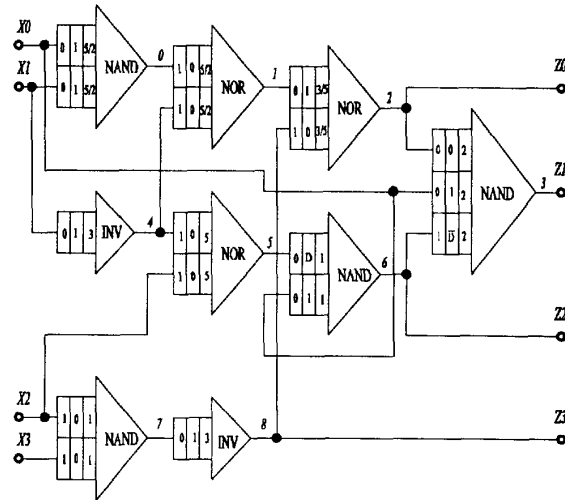


Fig. 15. Circuit CKT3 showing worst-case conditions for excitation and observability of RW-1 fault at node 5.

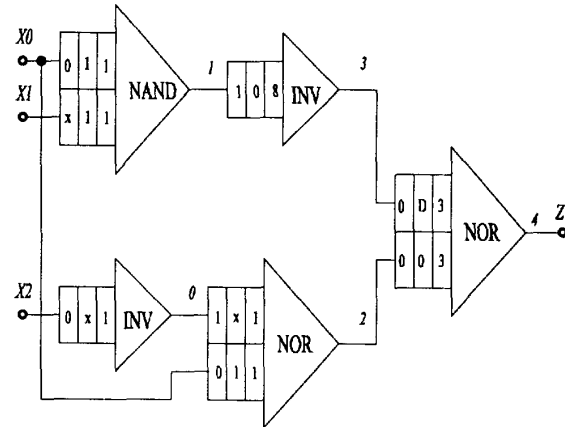


Fig. 16. Worst-case conditions for excitation and observability of RW-1 fault at node 3 in CKT4.

The above methodology can be extended for application to sequential circuits as well. That is because storage elements are typically composed of CMOS gates, in which inputs and outputs are cross-coupled. Therefore, Equation (8) can be used to determine the sensitivity of nodes in sequential circuits. However, we will have to find the worst-case combination of the *sequence* of irradiation and postirradiation test vectors that can maintain the excitation and observability conditions of the RW-1 fault at the most sensitive node.

The difference between the worst-case and best-case test-vector combination in terms of failure level depends on the technology and circuit design. We found that, for P1 (rad-hard technology), this difference is about a factor of 2, and, for P2 (rad-tolerant technology), it is about a factor of 5 for node sensitivities between 0.01 and 20. Therefore, the importance of utilizing worst-case test vectors during total-dose testing depends on the application and the environment where the device under test will be used. It appears, though, that worst-case test vectors become more significant for softer technologies, especially commercial devices, where circuit designers do not follow circuit design guidelines for radiation hardening.

V. CONCLUSION

We focused in this work on developing a methodology for the identification of worst-case test vectors for total-dose testing of CMOS circuits. In general, test vectors are input vectors that satisfy the fault excitation and observability conditions. Our approach was inspired by the approach used in the generation of test vectors that detect process defects in the manufacturing of VLSI devices. We started by performing a gate-level failure analysis of the logic faults induced by total dose in CMOS circuits. We correlated the induced logic failure and the irradiation/postirradiation input-vector combination. Then we developed a new fault model, RW-1, that simplifies the identification of the excitation conditions. We also developed a model for node sensitivity to logic failure. We found that node sensitivity depends on both irradiation and postirradiation input vectors. We also found that both the irradiation and postirradiation input vectors contribute to the excitation and observability conditions, proving that both input vectors have to be treated in *combination*. We developed a heuristic methodology to simplify the search for the worst-case combination of test vectors. We implemented the methodology in simple CMOS circuits and verified the results using circuit simulations derived from experimental data of two different technologies, P1 (rad-hard) and P2 (rad-tolerant). We found that the significance of using worst-case test vectors in total-dose testing depends on the circuit design and the technology used; worst-case test vectors are more significant for softer technologies and design practices.

In the future, we want to develop methodologies for the identification of worst-case test vectors for other kinds of failure modes, e.g., leakage current failure and delay failure. We also want to work on developing a computer-aided tool for the automatic identification of worst-case test vectors for all failure modes so that vendors can find it easy to supply total-dose test engineers with the appropriate set of test vectors.

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