A 10-V Josephson Voltage Standard

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Abstract—**This paper describes the design and operation of an 18 992 Josephson-junction array which can generate reference voltages up to 12 V. This device has applications for the direct calibration of Zener reference standards, calibrators, and digital voltmeters at the 10-V level, and for very accurate linearity and ratio measurements.**

I. Introduction

In THE last several years large arrays of 2000 or more Josephson junctions have been used in many laboratories to generate reference voltages on the order of 1 V [1]–[4]. These devices can be used to calibrate standard cells and other reference devices at the 1-V level without the use of a voltage divider. This has resulted in substantial improvements in accuracy and has greatly simplified the operation of Josephson voltage standards. A series array of 15 000–20 000 junctions would extend the inherent simplicity and accuracy of a direct calibration to the 10-V level commonly used in precision Zener-diode reference standards. The first observation of Josephson steps at the 10-V level used an array of 14 184 junctions [5]. The poor stability and large microwave power requirement of this array made its use as a practical standard marginal. This paper describes an array with a modified design which resolves the problems of stability and power requirement. The new arrays can perform direct calibrations at levels up to 12 V and have also found application for ratio and linearity measurements.

II. Array Design

Fig. 1 is a drawing of the 10-V array. It is a straightforward extension of a previous 2076-junction array design [4]. A finline at one end of the chip collects 70–100 GHz radiation from a waveguide and directs it into a microstripline. The microstripline splits into 16 parallel paths, each of which passes through 1187 junctions. The 16 microstriplines are terminated in matched loads. High impedance connections between sections allow the dc voltage across all 18 992 junctions to add in series. Blocking capacitors in the microstriplines prevent the dc voltage from being short circuited through the microwave network. "Curly" bends are used in the microstriplines to minimize the chip area without compromising the bend radius-to-width ratio of 3.2. Significantly smaller ratios lead to unacceptable reflections at the bends.

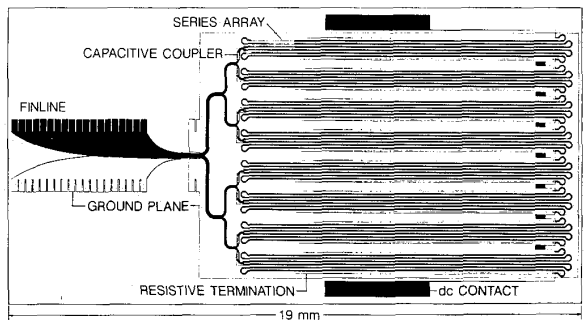

Fig. 1. The layout for an 18 992 junction voltage-standard array.

The length of each microstripline section is limited to about 1200 junctions by the attenuation in the microstripline, which is estimated to be 0.004 dB/junction. After passing through about 1200 junctions the microwave power is significantly below the optimum value for step generation. Since each junction generates from 0.5 to 1 mV, the total number of junctions required for 10-V operation is about 20 000. Thus the microwave power must be split into 16 sections. The power required for each section is proportional to the square of the junction capacitance. Thus in order to minimize the total microwave power required, smaller (lower capacitance), higher-current density junctions were used. This reduces the margin of acceptable critical current density from the 30-90 A/cm^2 of the 1-V design to about 50–90 A/cm^2 for the 10-V design. Table I lists the primary design parameters of the 10-V array.

III. Fabrication

The primary technical challenge in realizing the 10-V Josephson standard is the fabrication of nearly 19 000 flawless junctions with critical currents which all fall in the acceptable range of 150–250 μA. Junctions with low critical currents will be overdriven by the microwave input while those with high critical currents will exhibit chaotic behavior [6], [7]. In either case the array will not generate stable quantized levels. Two process modifications were critical in achieving a successful result. First, the lithographic process was improved by converting from a contact printer to a noncontact wafer stepper which projects and reduces the image. This decreased the defect density by about two orders of magnitude. Second, just

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TABLE I
10-V ARRAY DESIGN PARAMETERS

Junction materials	$Nb/Nb_2O_5/PbInAu$
Critical current density	70 A/cm^2
Junction length	12 μm
Junction width	24 μm
Critical current	200 μA
Plasma frequency	22 GHz
Lowest resonant mode	175 GHz
rf drive frequency	87 GHz
rf drive power	5 mW at finline input

before the barrier oxidation, the cathode around the wafer was coated with lead to give a more reproducible environment, and the wafer and cathode were vigorously sputter cleaned.

IV. 10-V ARRAY PERFORMANCE

It is not advisable to display the full I–V curve of these 10-V arrays because the combined energy gap voltage of 51 V may breakdown the 1-μm thick microstripline dielectric. The partial I–V curve of Fig. 2 maps out the critical currents of the first 13 500 junctions of a typical array. The range of critical currents is 190–245 μA. A constant voltage step with an amplitude of 90 μA at 11 V is shown superimposed on the I–V curve. The frequency response of this array was measured by applying a fixed power level (4 or 20 mW) at the finline input and measuring the highest voltage step which crossed the zero current axis as a function of frequency. The result, using three different microwave sources, is shown in Fig. 3. Voltages well above 10 V can be reached over a fairly broad frequency range. The structure in the frequency response is not well understood but is typical of all array chips measured.

The design of the cryoprobe used to insert the chip into a liquid He Dewar is critical to the operation of these arrays. The chip must be magnetically shielded and all electrical leads attached to it must be filtered to remove RF interference. The waveguide is a 90-cm length of 90–10 bronze WR-12 guide and has a loss of 5.5 dB. The bronze guide is a compromise between microwave loss and thermal loss. A better but more expensive solution is a composite guide consisting of 30 cm of solid silver guide, 15 cm of internally gold plated stainless steel guide, and 30 cm of solid silver guide. This guide has about the same thermal loss but a microwave loss of only 2.8 dB. Commercially available Gunn diode sources with output powers of 40 mW are quite sufficient to supply the 4 mW required at the finline input of a 10-V array.

We have used 10-V arrays in the same system used to perform calibrations at the 1-V level [4]. Calibration of a reference standard is performed by selecting the step number, n, and the frequency, f, such that the array voltage $nhf/2e$ is within a few microvolts of the reference value. Since n can take on any value in the range

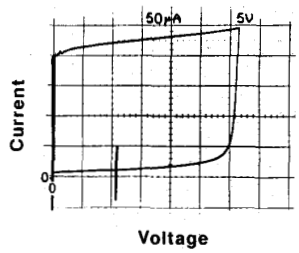

Fig. 2. A double exposure showing a 10-V array I–V curve without microwave power and a single constant voltage step at 11 V with 4 mW at 87 GHz applied at the finline input.

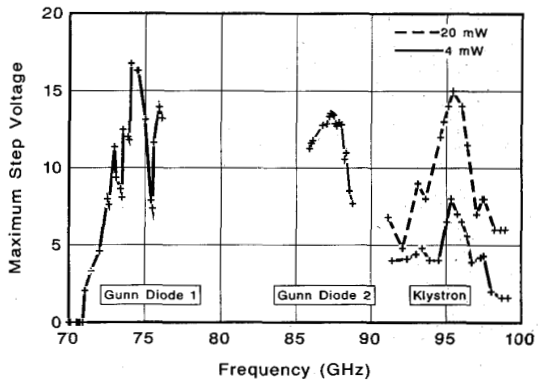

Fig. 3. A plot of the maximum step voltage as a function of frequency for power inputs of 4 and 20 mW at the finline input.

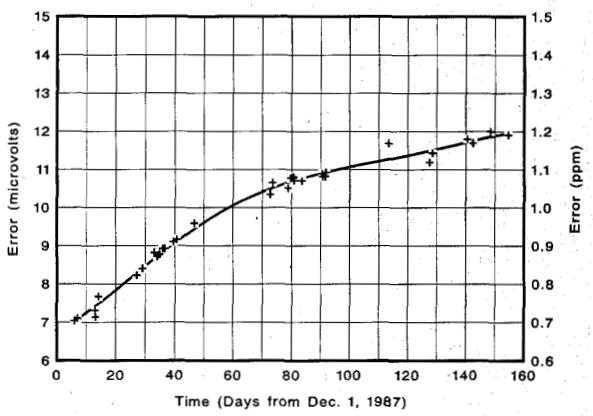

Fig. 4. A 5 month record of calibrations of a Zener reference standard versus the 10-V Josephson array standard.

$-75\,000$ to $+75\,000$ and f can be tuned over a few gigahertz, any voltage between a few millivolts and 12 V can be achieved. Selecting a particular value of n requires a very stable bias source with an adjustable output impedance and very fine control over the level. Calibrations of a Zener reference standard using 900 null readings and two reversals can be completed in about 15 min. The uncertainty is dominated by the noise of the Zener reference and is typically 0.004 ppm. Fig. 4 shows 70 calibration points for a Zener reference standard taken over a period of 5 months. Different chips, probes, and frequencies were used with no statistically significant effect.

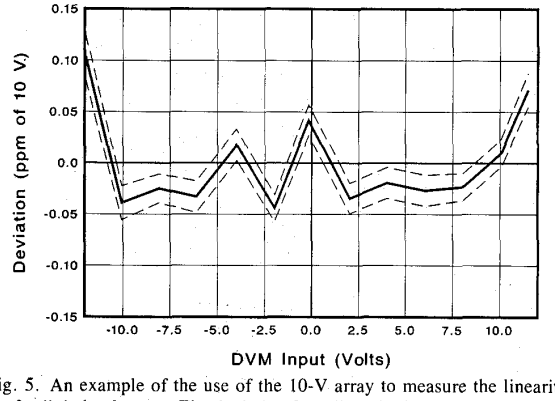

Fig. 5. An example of the use of the 10-V array to measure the linearity of a digital voltmeter. The deviation from linearity is plotted in parts per million of the 10-V full scale value.

The flexibility of the array in generating a wide range of accurate voltages has also found application in making very accurate ratio and linearity measurements. At least one recently introduced digital voltmeter has a linearity specification of 0.1 ppm, a level which is difficult to verify with conventional voltage divider techniques. This instrument was tested by comparing its reading with the array voltage at a set of arbitrarily chosen points. This data were then fitted to a straight line and the deviation from linearity plotted as a function of voltage. A typical result, shown in Fig. 5, verifies that the maximum linearity deviation for the DVM is ± 0.05 ppm of full scale over a range of ± 10 V. The dashed curves indicate the 3-σ uncertainty due to noise in the measurement. This result illustrates two important points. First, the 10-V Josephson array is a very accurate and flexible instrument for making linearity/ratio measurements and second, state-of-the-art digital voltmeters are now capable of ratio measurements with an accuracy comparable to that achieved with conventional voltage dividers.

Much work remains to be done to make the 10-V Josephson voltage standard into a practical and widely used instrument. The fabrication yield of 10-V chips must attain a level where chips are readily available at reasonable cost. Our experience to date indicates that with proper handling, our array chips last more than a year. A significant improvement is expected when 10-V array chips are fabricated with the Niobium–Aluminum Oxide–Niobium process. Both ETL and NBS have already made 1-V arrays with this process. These arrays use significantly lower microwave power and are expected to be much more durable than the Niobium-Lead devices.

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