SIMULATION OF CASCADED H- BRIDGE MULTILEVEL INVERTER USING PD, POD, APOD TECHNIQUES

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ABSTRACT

Multilevel inverter (MLI) can achieve medium voltage high power efficiency inverters in industrial application. It can generate stepped waveform by reducing harmonic distortion with increase in the number of voltage level; a full bridge is known as H-bridge inverter because it shows alphabet 'H'. In this paper, Multicarrier PWM topologies and there Modulation schemes are discussed. Level Shifted [LS] Scheme is applied to the Cascade H-bridge multilevel inverter and the complete analysis of THD to 9 levels is done.

KEYWORDS

Multilevel Inverter, Cascaded H-Bridge, Multicarrier (PWM) topologies.

1. MULTILEVEL INVERTER

The inverter is a power electronic circuit which converts the DC to AC power, used in power backup at home [1]. Like motor, radio etc. Now days Multilevel Inverters are used in high power switching application [2-3].Multilevel Inverter consists of several switches, used in industrial applications, Railway Traction Drives and Electrical Vehicle etc. [4].

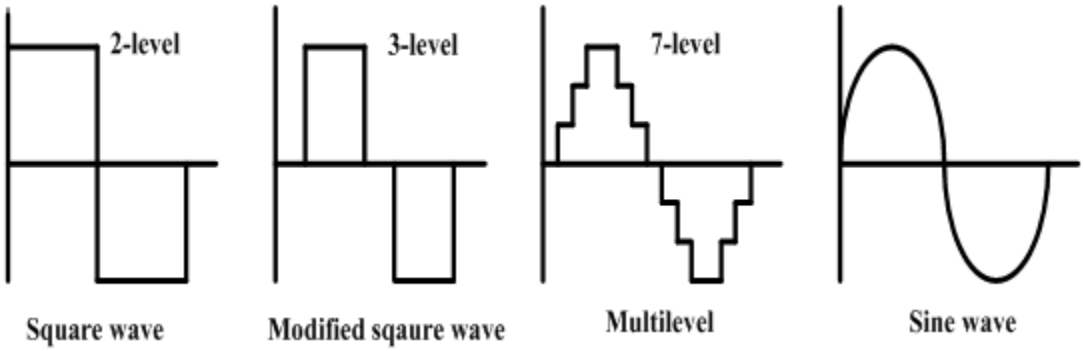

Figure 1. Inverter Output Waveform [5]

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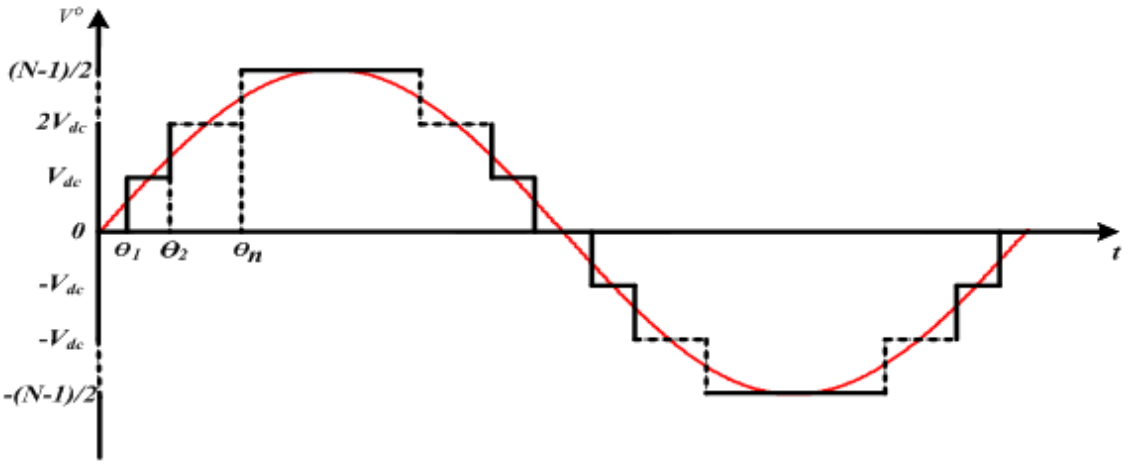


Figure 2. Generalized stepped waveform of multilevel inverters [1]

1.1 Classification of Multilevel Inverter

Figure 3 Shows Inverter is classified into Cascade H-Bridge Multilevel inverter (CHB-MLI), Flying Capacitor Multilevel inverter (FC-MLI), Diode Clamped inverter (NPC-MLI) [2-3].

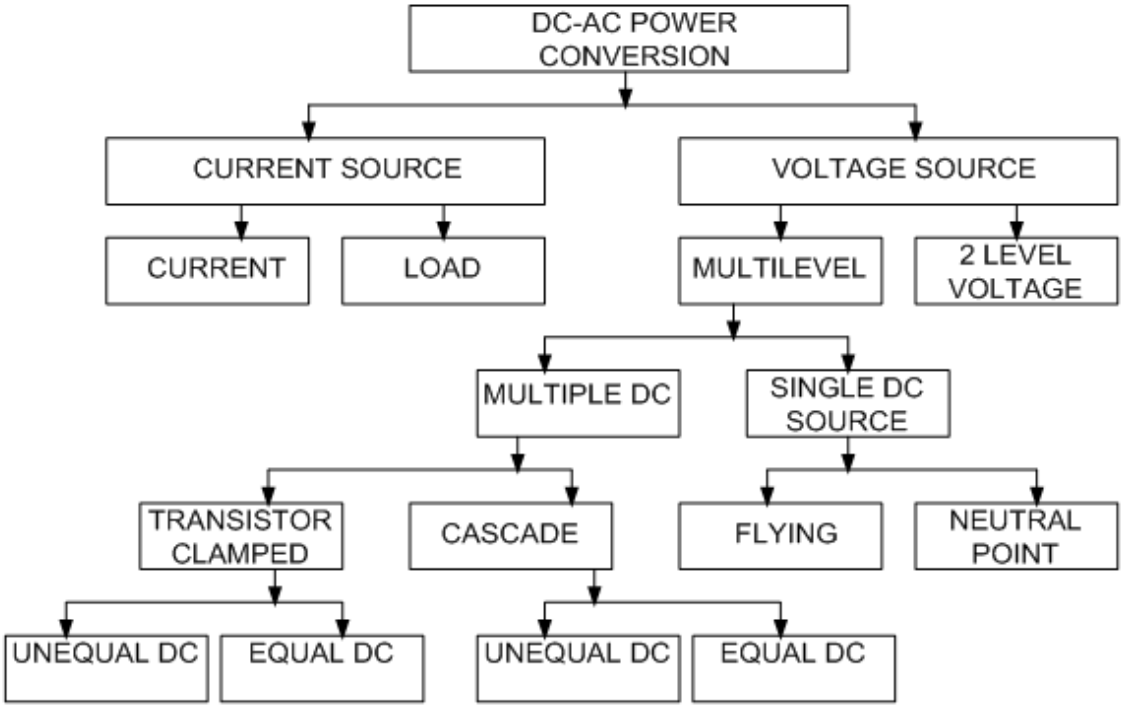


Figure 3. Classification of Multilevel Inverter [1-3]

1.2 Main Topologies of MLI

- Diode Clamped Inverter
- Flying Capacitor
- Cascaded H-Bridge Inverter

1.2.1 Diode Clamped Multilevel Inverter (DC-MLI)

Figure 4 shows 3 level Diode clamped inverter also known as Neutral Point Clamped Inverter (NPC).The maximum output voltage is half of the input DC voltage. To remove this problem, simple control technique is applied i.e. increasing the component like switches and diodes [1-5].

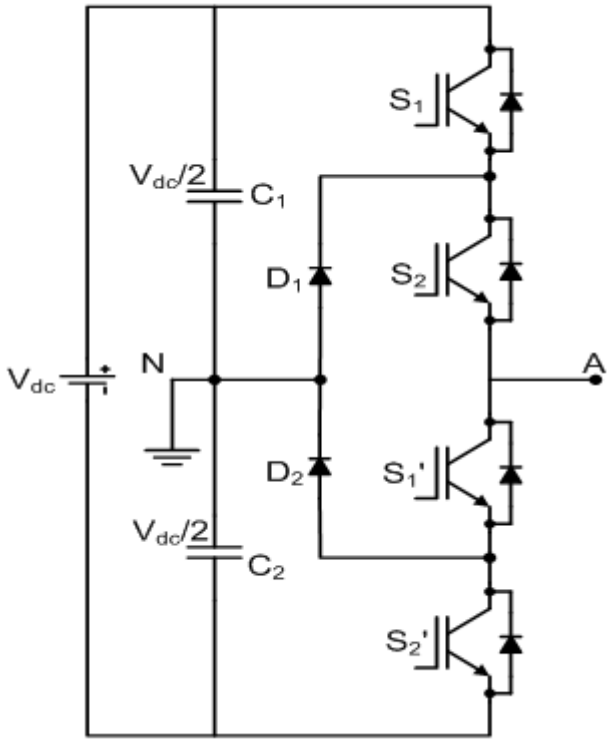


Figure 4 3-level Diode-clamped inverter

Table 1. Switching Pattern of diode-Clamped Multilevel Inverter

Output Voltage $V_o = V_{an}$	**Switch states**			
	S_1	S_2	S_1'	S_2'
$V_{dc}/2$	*1*	*1*	*0*	*0*
0	*0*	*1*	*1*	*0*
$-V_{dc}/2$	*0*	*0*	*1*	*1*

Advantages:

- The Control technique is simple.
- When the number of levels increases the distortion content is reduced.

Disadvantages:

- When the number of level is high more clamping diodes are used.

1.2.2 Flying Capacitor Multilevel Inverter (FC-MLI)

Figure 5 shows the 3 level Flying Capacitor Multilevel, also known as Capacitor Clamped Inverter. Clamping diodes are replaced by flying capacitors. It can control both active and reactive power flow [5-12].

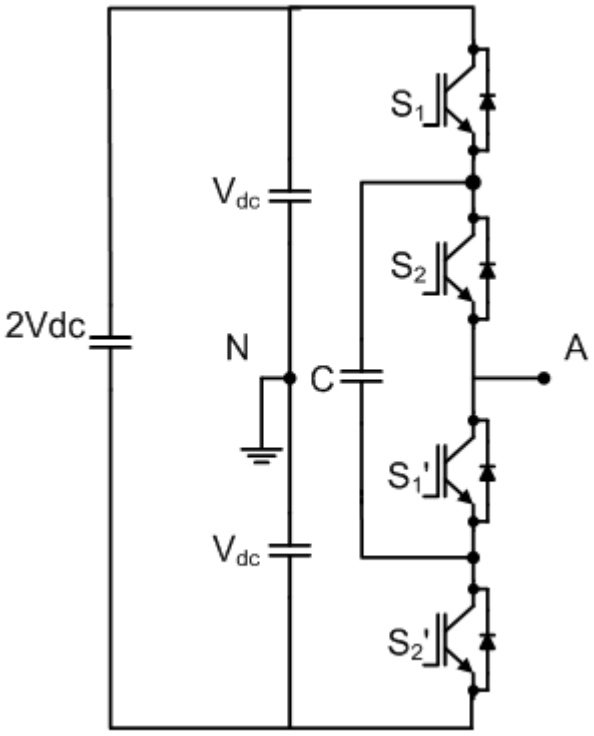


Figure 5 3-level flying capacitor inverter

Table 2. Switching Pattern of Flying Capacitor Multilevel Inverter

Output Voltage $V_o = V_{AN}$	Switch states			
	S_1	S_2	S_1'	S_2'
V_{dc}	1	1	0	0
0	1	0	1	0
	0	1	0	1
$-V_{dc}$	0	0	1	1

Advantages:

- Similar to NPC inverter to avoid the needs for filters.
- A Large amount of packing capacity.

Disadvantages:

- Inverter control can be complicated.
- Switching losses are high.

1.2.3 Cascaded H-Bridge Multilevel Inverter (CHB-MLI)

Figure 6 shows the 3 level CHB MLI consist of single H-bridge combine with a series of the power conversion cell. Cascaded H-Bridge Multilevel Inverter is better than the diode clamped inverter and flying capacitors inverter, it requires less number of the component in each switching levels. In Cascade H-Bridge Multilevel Inverter, the grouping of switches and capacitors is called H-bridge consisting of isolated DC Voltage source [10].

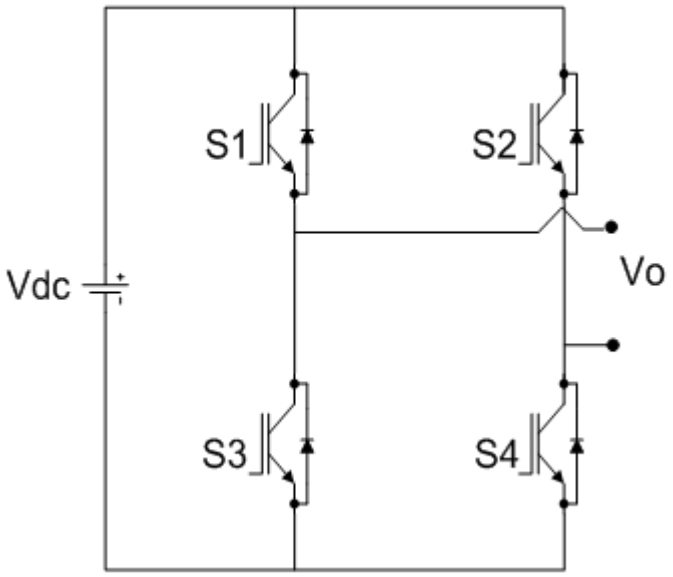


Figure 6 3-level cascaded H-bridge inverter

Table 3. Switching Pattern of Cascade H-Bridge Multilevel Inverter

Output Voltage $V_o = V_{AN}$	**Switch states**			
	S_1	S_2	S_3	S_4
V_{dc}	*1*	*0*	*0*	*1*
0	*1*	*1*	*0*	*0*
	0	*0*	*1*	*1*
$-V_{dc}$	*0*	*1*	*1*	*0*

Advantages:

- Reduced THD.
- As Compare to Diode clamped and Flying capacitor inverter it can required less number of components in each level.

Disadvantages:

- It needs isolated DC voltage sources.

2. MODULATION TECHNIQUES

Modulation Technique is Low and High switching Frequency fort high switching frequency is considered above 1 KHz [13].

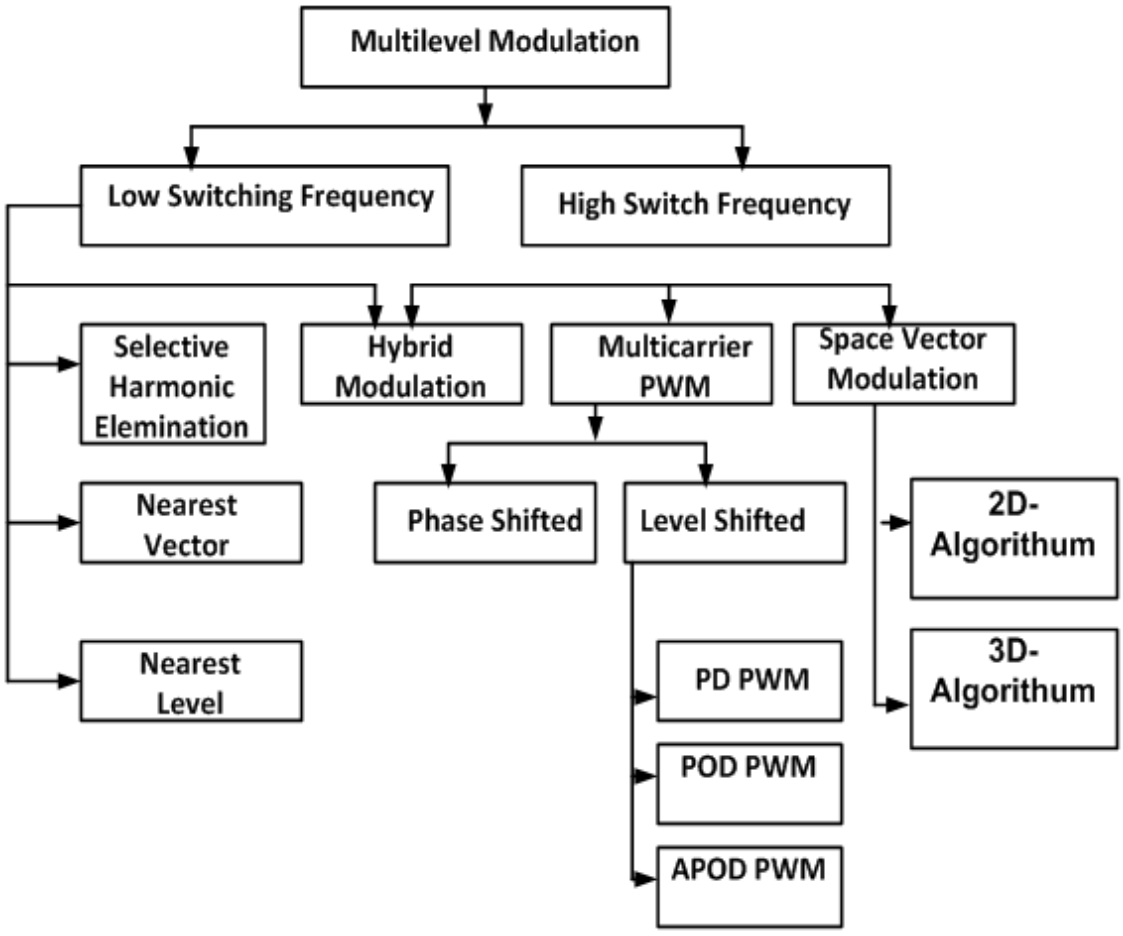


Figure 7. Classification of Modulation Technique

2.1 Multicarrier PWM

Multiple Pulse Width Modulation Technique is used in three level or more than three levels. These are classified into two types: - Level Shift, Phase Shift.

2.1.1 Level Shifted PWM (LS-PWM)

N-1 carrier signals are used which are vertically shifted to each other. A level-shifted PWM can be classified in three types [14-16-17-18].

- **Phase Disposition (PD-PWM):** In Phase Disposition all the carrier signals are in same phase.

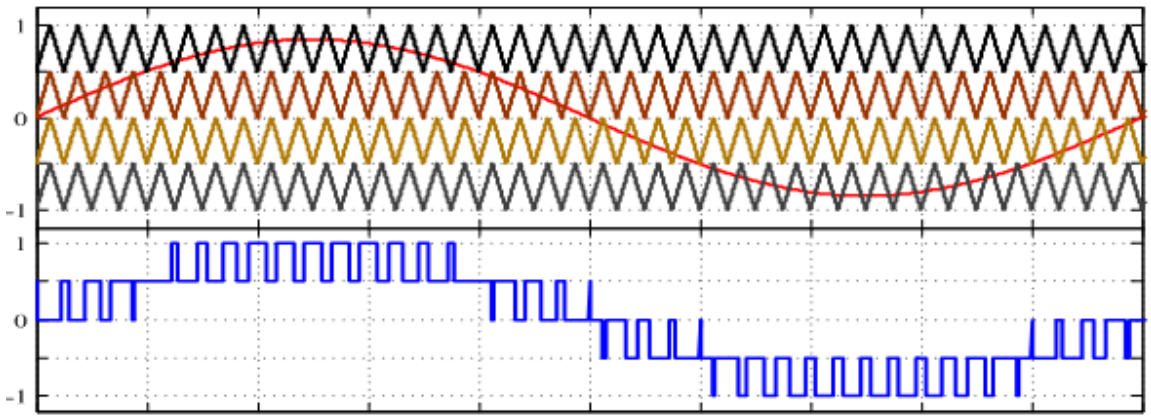


Figure 8 PD-PWM

- **Phase Opposition Disposition (POD-PWM):** In Phase Opposition Disposition all the carrier signals above the zero are out of phase with those below the zero by 180º.

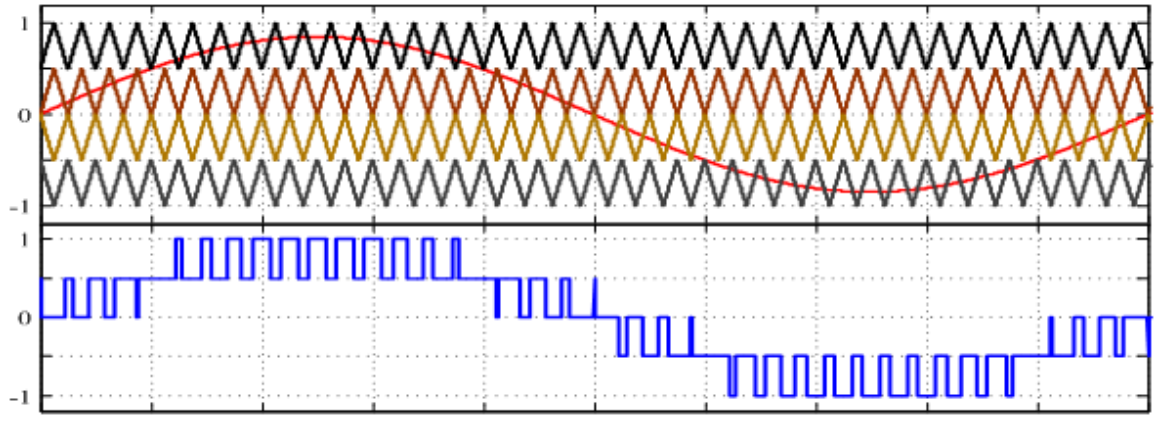


Figure 9 POD-PWM

- **Alternative Phase opposition Disposition (APOD-PWM):** In Alternate Phase Opposition Disposition all the adjacent carrier signals are out of phase by 180º.

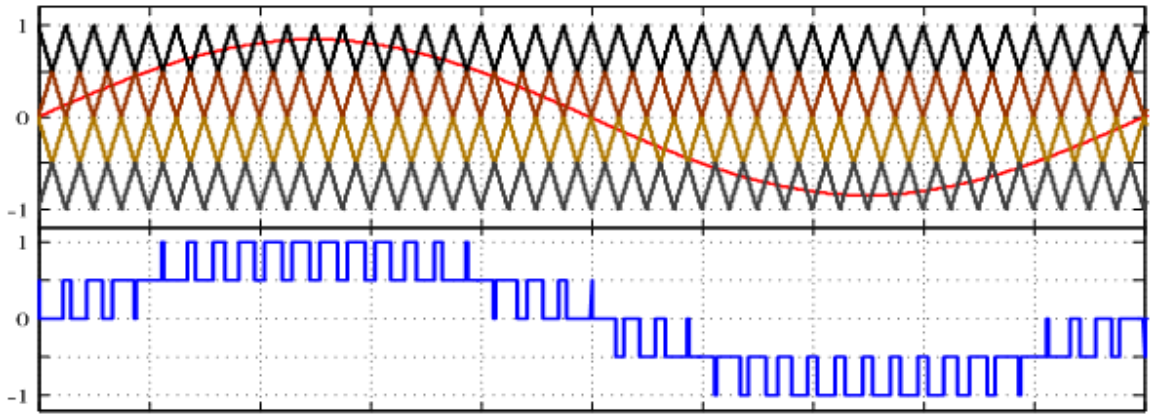
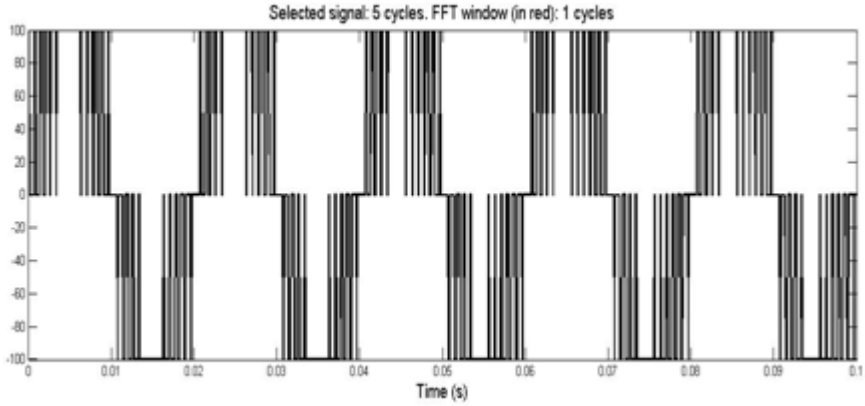


Figure 10 APOD-PWM

3. SIMULATION AND RESULTS

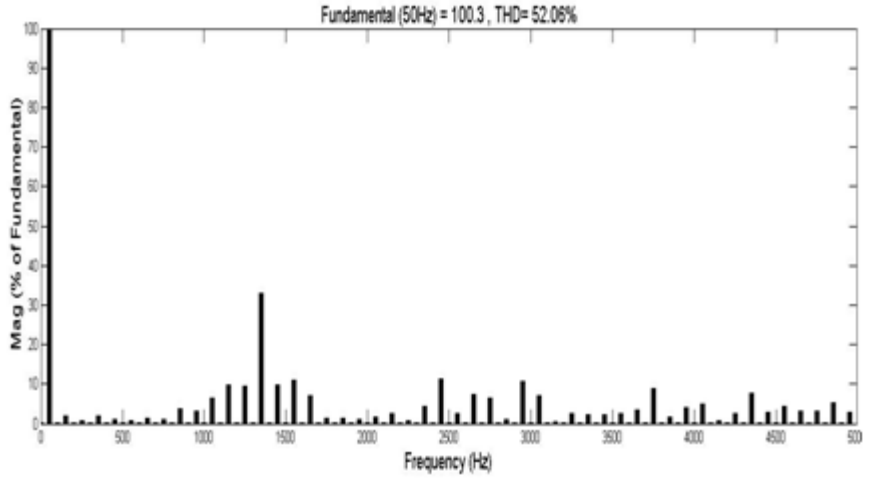
Table 4. THD Comparisons of PWM Technique

S.No	PWM Technique	No of Level	THD %
1.	Phase Disposition	3 Level	52.06%
2.	Phase Opposition Disposition	3 Level	54.17%
3.	Alternate Phase opposition Disposition	3 Level	54.17%
4.	Phase Disposition	5 Level	26.69%
5.	Phase Opposition Disposition	5 Level	26.96%
6.	Alternate Phase opposition Disposition	5 Level	37.13%
7.	Phase Disposition	7 Level	18.05%
8	Phase Opposition Disposition	7 Level	22.48%
9.	Alternate Phase opposition Disposition	7 Level	25.20%
10.	Phase Disposition	9 Level	16.77%
11.	Phase Opposition Disposition	9 Level	17.08%
12.	Alternate Phase opposition Disposition	9 Level	17.10%

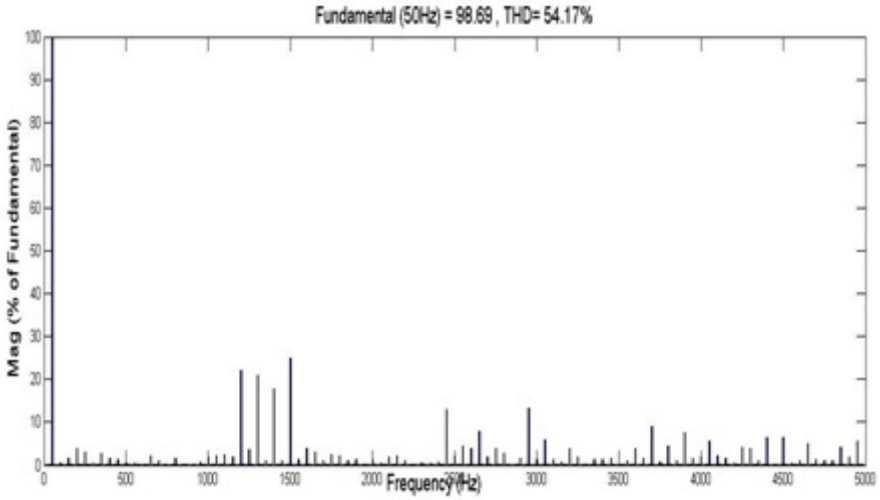


Showing the Phase Voltage 3 Level CHB MLI

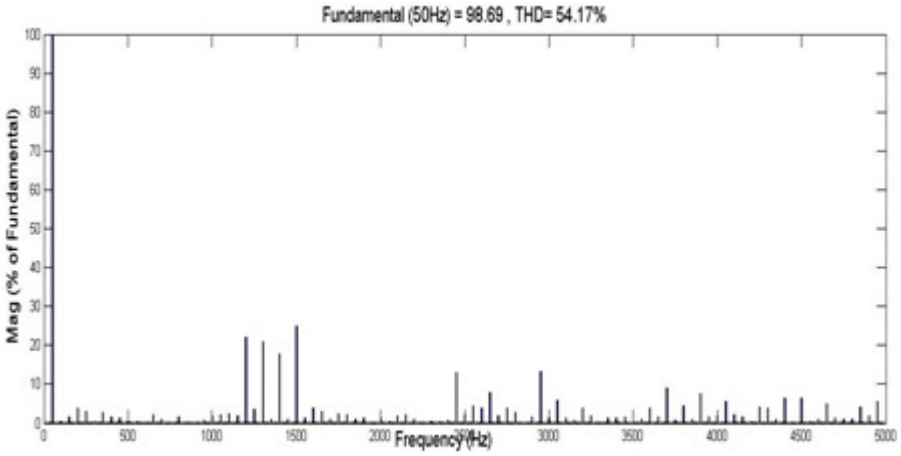
THD Analysis of 3 Levels CHB MLI (a) PD (b) POD (c) APOD



(a)



(b)



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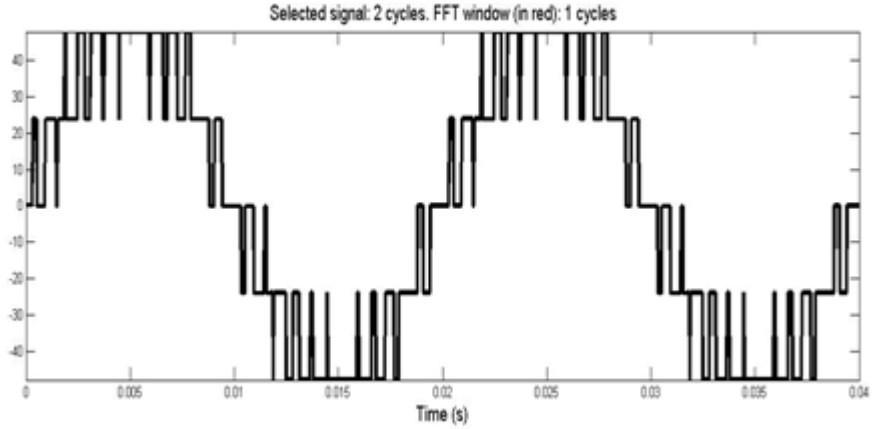
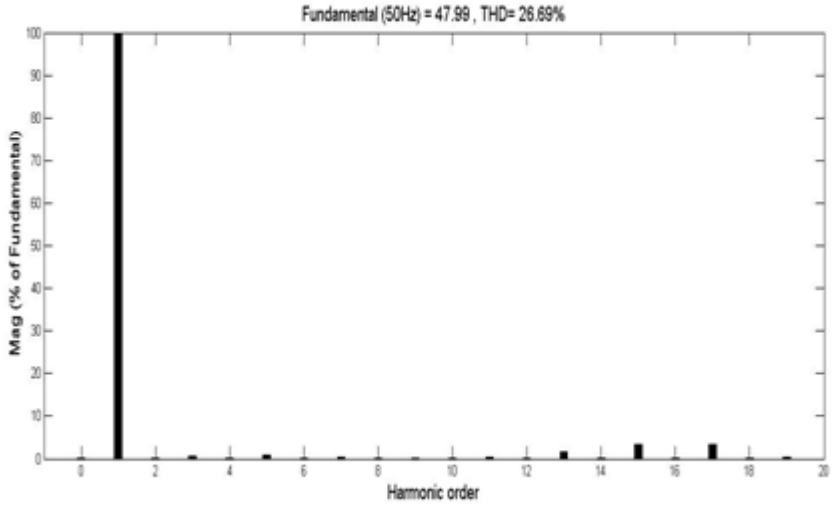
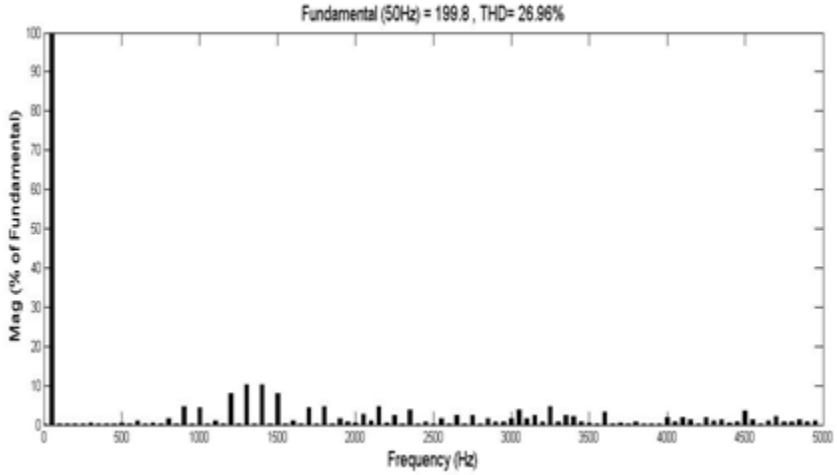


Showing the Phase Voltage 5 Level CHB MLI
THD Analysis of 5 Levels CHB MLI (a) PD (b) POD (c) APOD



(a)



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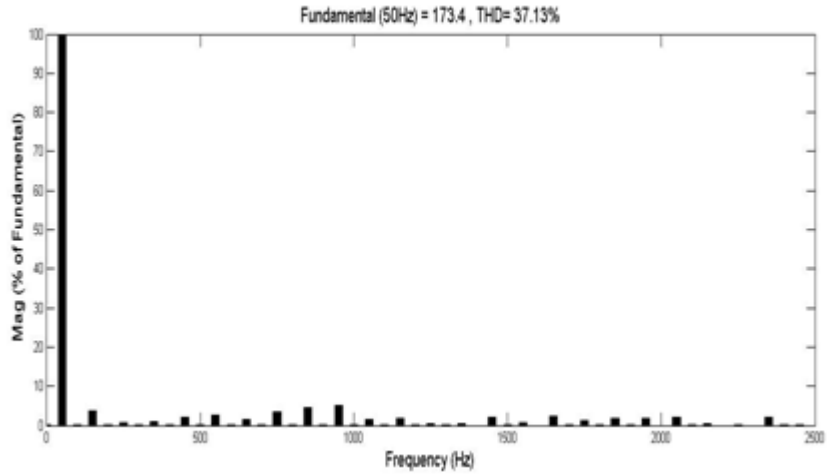

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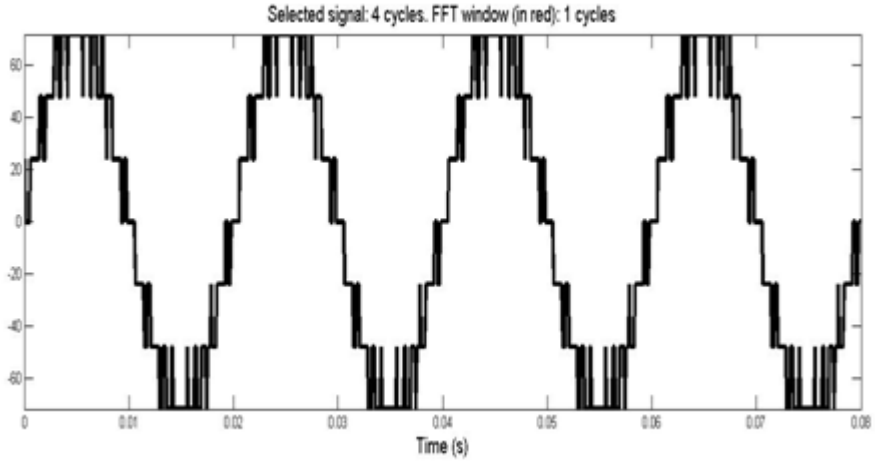
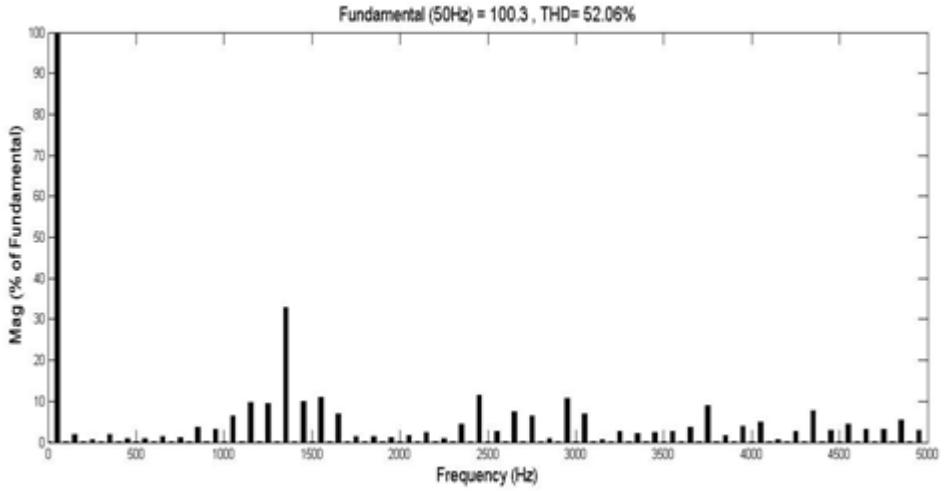
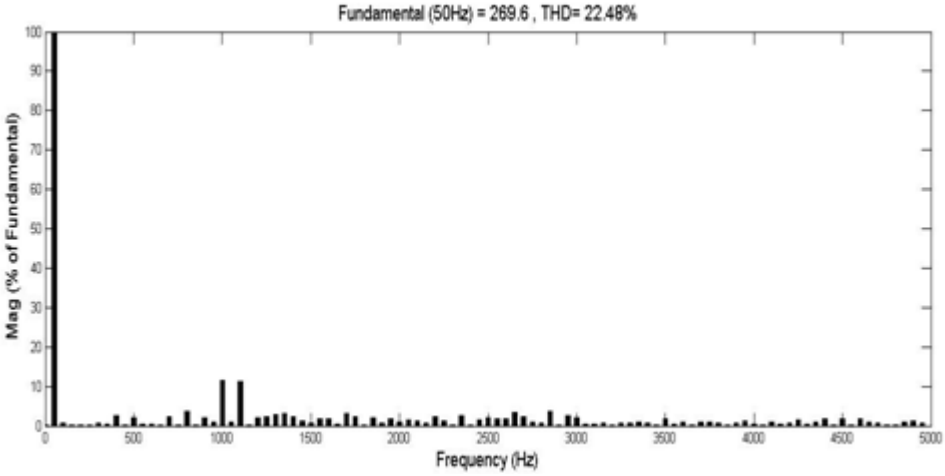


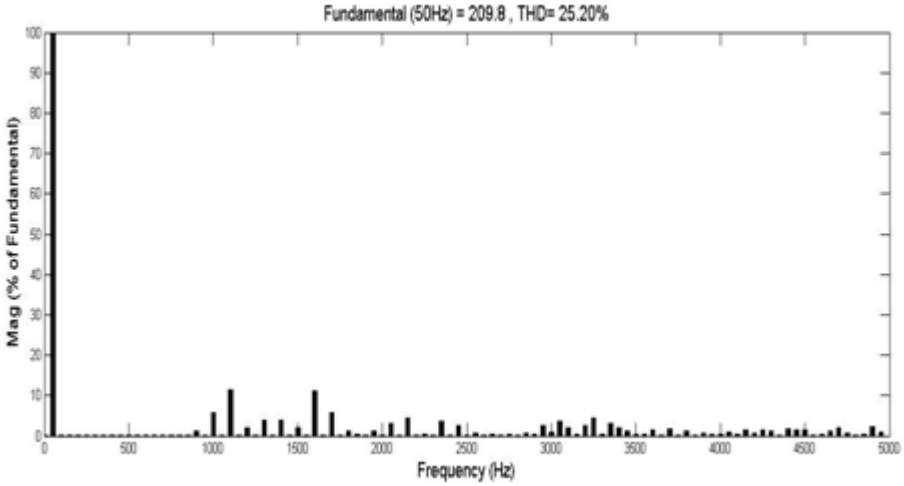
Showing the Phase Voltage 7 Level CHB MLI
THD Analysis of 7 Levels CHB MLI (a) PD (b) POD (c) APOD


Fundamental (50Hz) = 100.3 , THD= 52.06%
Mag (% of Fundamental)
Frequency (Hz)

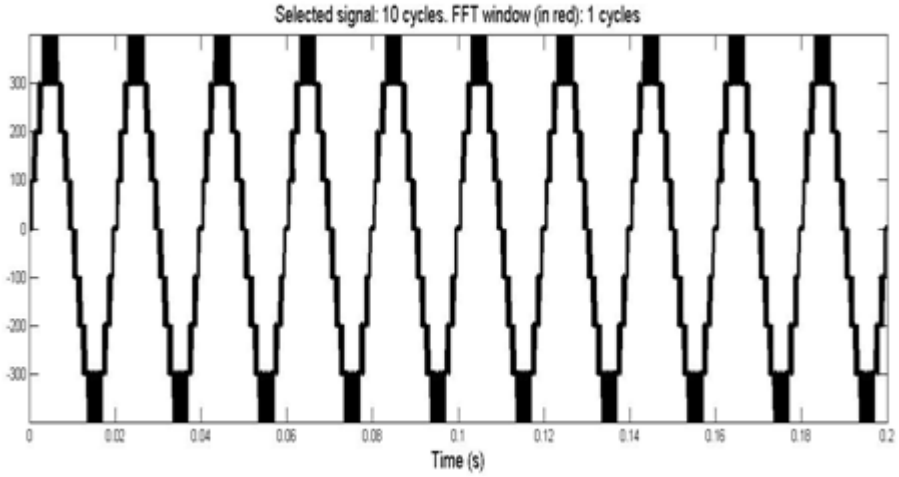
(a)


Fundamental (50Hz) = 269.6 , THD= 22.48%
Mag (% of Fundamental)
Frequency (Hz)

(b)

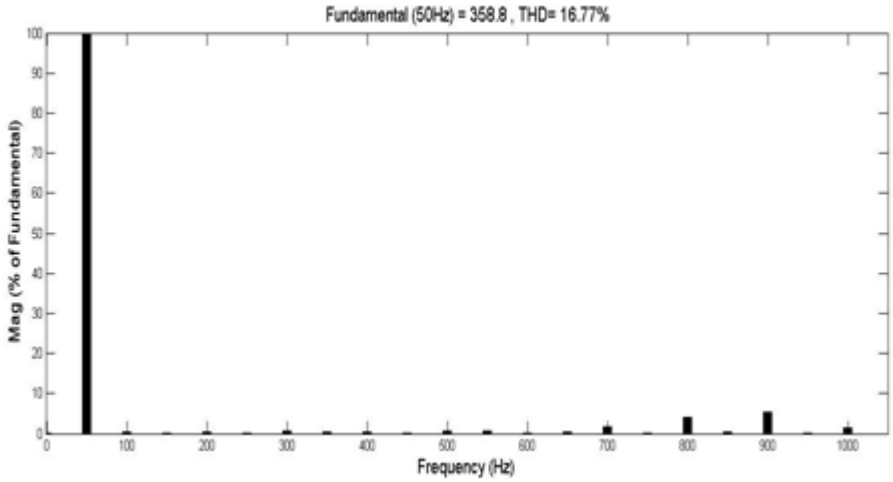

Fundamental (50Hz) = 209.8 , THD= 25.20%
Mag (% of Fundamental)
Frequency (Hz)

(c)

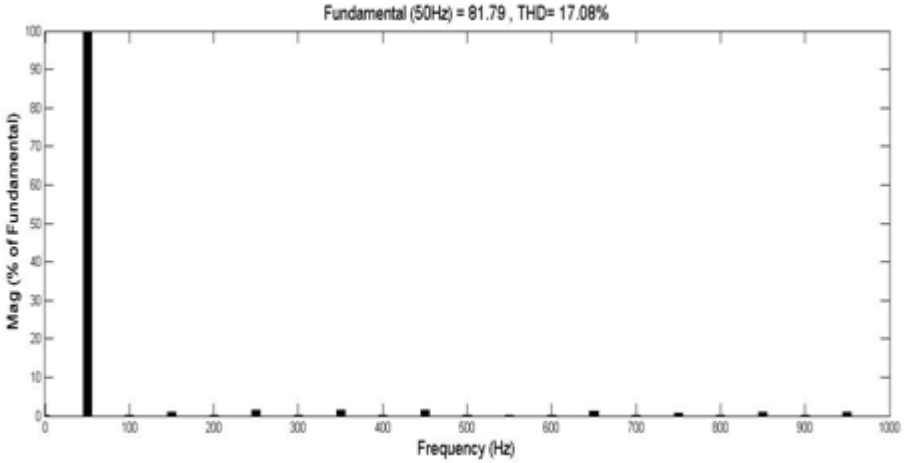


Showing the Phase Voltage 9 Level CHB MLI

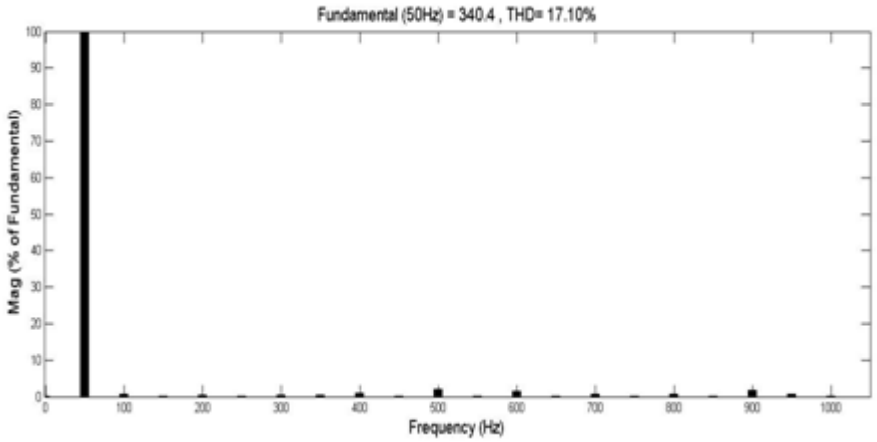
THD Analysis of 9 Levels CHB MLI (a) PD (b) POD (c) APOD



(a)



(b)



(c)

4. CONCLUSION

In this paper has been Discuss the Cascade H-Bridge Topology using Phase Disposition, Phase opposition Disposition, and Alternate Phase opposition Disposition are compared. The three techniques it can conclude that the Phase Disposition Topology is better among the three topologies. Simulation results show that it can see that when we increase the number harmonics content will be reduced.

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