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Electron-beam lithography with the scanning tunneling microscope

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The scanning tunneling microscope (STM), operated in vacuum in the field emission mode, has been used in lithographic studies of the resist SAL-601 from Shipley. Patterns have been written by raising the tip–sample voltage above −12 V while operating the STM in the constant current mode. Resist films, 50 nm thick, have been patterned and the pattern transferred into the GaAs substrate by reactive ion etching. The variation of feature size with applied dose and tip–sample bias voltage has been studied. Comparisons have been made to lithography with a 10 nm, 50 kV electron e-beam in a JEOL JBX-5DII in the same resist thickness films. In all cases the resist films were processed in the standard fashion before and after exposure. The STM can write smaller minimum features sizes and has a greater process latitude. Proximity effects are absent due to the reduced scattering range of the low energy primary electrons. However, the writing speed is slower, being limited by the response of the piezoelectric scanner. Advances have been made recently in the construction of fast STMs which scan at video rates making the STM comparable in speed to the JEOL for nanolithography. The development of ultralow voltage e-beam lithography based on STM technology is discussed.

I. INTRODUCTION

A steered beam lithography tool represents an essential part of the technology to meet the current and future need for ultrahigh resolution mask making and direct write. The need for sub-100 nm lithography (nanolithography) is evident for the next century. In the case of e-beam lithography, the major obstacles to increased resolution are the understanding of proximity effects and their correction. Even in present day e-beam lithography systems, resolution is limited by proximity effects as opposed to the size of the focused beam. The conventional approach to overcome proximity effects is to increase the primary beam energy as this creates a more diffuse "fog" of backscattered electrons for which correction can be made. This technique has been shown to work with some resists and substrates but it is not clear that correction can be made for a broad range of resists and substrates at a resolution below 100 nm. An alternative strategy is to decrease the primary beam energy so the scattered electrons responsible for proximity effects are spatially localized. The logical extension of this approach is to lower the energy close to the threshold energy required for the material change (i.e., resist chemistry). However, the creation of such a focused low energy electron beam is difficult. The advent of the scanning tunneling microscope (STM) provides a technique for providing a spatially confined (but not focused) electron beam.

In the STM a sharp tip is maintained very close to a surface by controlling the tip–sample separation with a simple servo loop. The servo controls the position of the tip to maintain a constant tip–sample current. In most applications the STM is operated with a small voltage bias (<4 V) between the tip and the sample, so the tip–sample current is that which tunnels through the electronic barrier between the tip and the sample. The tunnel current is an exponential function of tip–sample separation allowing the servo loop to precisely track a sample surface. At higher tip–sample biases, the tip–sample current is determined by field emission from the tip (or sample). For the same current, the tip–sample separation is greater in the field emission mode than that in the tunneling mode. The field emission current is also an exponential function of the separation. As a result, surface topographic imaging and lithography can be readily performed.

In recently published papers,[1,2] we have shown that lithography in resist materials is possible with the STM. Here we demonstrate that the lithography is technologically useful by demonstrating that a pattern defined with the STM can be replicated into a semiconductor substrate with a reactive ion etch. We also discuss issues relevant to the development of a lithographic tool based on STM technology.

II. STM LITHOGRAPHY

Two essential components of a lithographic technology are the abilities to both image the surface topography and modify a surface or surface film for patterning. Results are presented in this section describing the results of lithography with the STM and STM imaging of the lithographic process.

A. STM operation

The STM head was obtained commercially from W. A. Technology and is mounted in a stainless steel chamber with ion and turbo pumps. The STM is driven by custom built electronics and in-house developed software. Vacuum operation is required to avoid electrical breakdown between tip and sample. Lithography is performed at pres-

sures of about 10^{-7} Torr. Samples are introduced under dry N_2 and the chamber can be evacuated in about 15 min with the turbo pump which is then valved off and turned off for the lithographic patterning.

Lithography is performed by raising the voltage between tip and sample and moving the tip laterally (at a constant speed) with a constant tip–sample current to define a pattern. The STM tip is biased negatively with respect to the sample at voltages up to −35 V. Thus the STM is more properly described as operating in the field emission mode.

B. Sample preparation and processing

Operation of the STM requires a conductive substrate. Care must be taken to remove nonconductive oxides from the semiconductor surface. Si was etched in dilute HF to remove the native oxide and passivate the surface with hydrogen. GaAs was etched in 7:1:1 sulfuric acid: hydrogen peroxide: water, followed by rinsing in water and then coated with 10 nm of silicon which stabilizes the surface and improves resist adhesion. Films of the e-beam resist SAL-601 from Shipley were then spin coated onto the samples. Resist thickness was nominally 50 nm as measured with a surface profilometer. Following exposure, the resist was baked (107 °C for 7 min) and developed (17 min in MF-322) as recommended by the manufacturers.[3] The GaAs samples were etched in a small custom built reactive ion etch (RIE) system with boron trichloride. Etching was performed at an radio frequency (rf) power of 80 W, a pressure of ~1 mTorr and a flow rate of 6 sccm. Samples were coated with 10 nm of gold or gold-palladium for inspection in a scanning electron microscope (SEM).

C. Lithography results

Successful patterning on GaAs has been achieved at tip–sample voltages between −12 and −35 V. The smallest voltage at which resist exposure has been observed is −12 V. With our present experimental setup, 3 pA is the minimum tip–sample current possible and 1 μm/s is the maximum lateral tip velocity. Even this minimum line dose (30 nC/cm) is sufficient to expose the resist. An example of STM lithography of SAL-601 is shown in Fig. 1, which is an SEM micrograph of an etched GaAs sample at an tilt of 45°. The micrograph has not been expanded vertically to correct for the tilt. The developed resist was used as a mask for an approximate 100 nm RIE of the substrate. The pattern was written at −25 V with a line dose of 200 nC/cm. The beam was "blanked" between the noncontiguous parts of the pattern by retracting the tip before moving it laterally to the start of the next element of the pattern (i.e., letter). We have achieved similar results by reducing the tip–sample current and/or voltage between features.[4] This has not proved as reliable due to limitations in the speed of our STM and the high exposure sensitivity of SAL-601.

SEM micrographs of a similarly patterned and etched GaAs sample are shown in Fig. 2. The micrographs give a clearer view of the depth of the etch and illustrate the absence of proximity effects. Both micrographs were taken

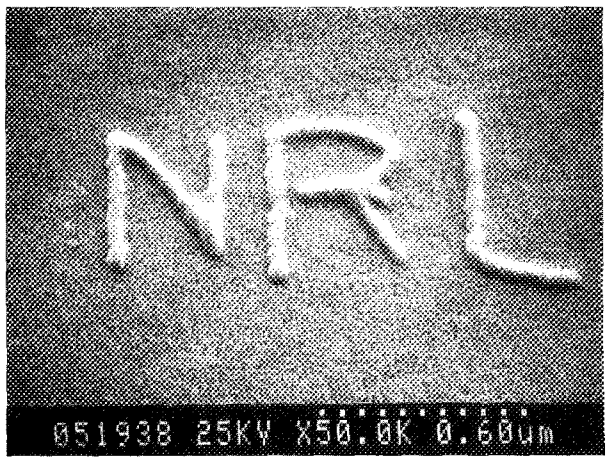

FIG. 1. Noncontiguous pattern written with the STM at a tip–sample voltage of −25 V in SAL-601 and etched 100 nm into GaAs.

with an (uncorrected) sample tilt of 45°. The pattern on the left was written at −35 V. The intersection between the lines show no signs of the interproximity effects found with such patterns written with a high voltage e-beam. The right half of Fig. 2 shows a different part of the same sample showing part of a pattern written at −15 V. The smaller linewidth is a result of the lower writing voltage. Note particularly the two lines separated by less than 10 nm to the left of the micrograph. Again no indication of any proximity effect is visible.

A further attractive feature of low voltage e-beam lithography is the wide process latitude. The variation of feature size with dose as shown in Fig. 3 is significantly less than that observed in lithography with a tightly focused 50 kV e-beam on identically prepared samples of SAL-601 on GaAs or Si.[5] A thirty times increase in line dose results in only a 40% increase in feature size. The lowest dose points shown in Fig. 3 correspond to the lowest tip–sample current (3 pA) possible with our setup. Even at this dose, no evidence of underexposure was observed. Also shown in the figure is the control of the feature size by the tip–sample bias. As the tip–sample bias is increased in magni-

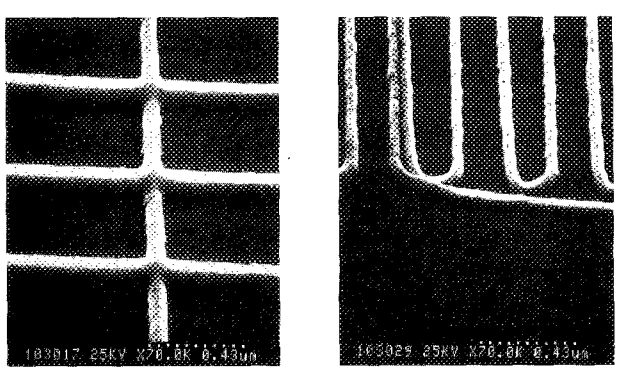

FIG. 2. STM written patterns in SAL-601 which have been transferred into the GaAs substrate by RIE. The left pattern was written at −35 V and 60 nC/cm. The right pattern was written with the same dose at −15 V, also at 60 nC/cm.

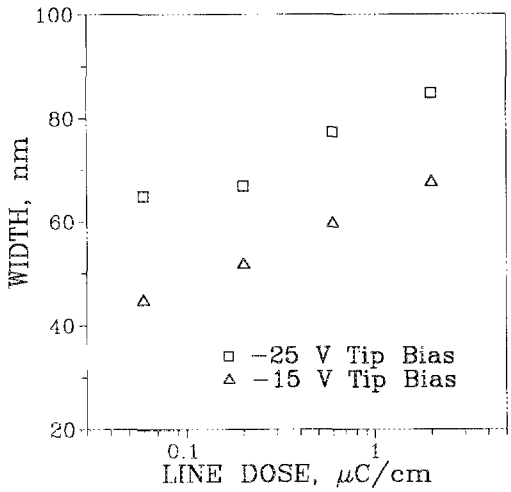

FIG. 3. Developed linewidth vs line dose for STM lithography in SAL-601

tude, the tip is retracted from the surface to maintain a constant tip–sample current. As a result, the effective spot size at the sample surface increases with tip bias. The data for Fig. 3 was recorded from SEM micrographs similar to Figs. 1 and 2. Some variation from sample to sample ($\pm \sim 15\%$) was observed which we attribute to variation in the sensitivity of SAL-601 and possibly effects of surface morphology. We are continuing to examine this issue.

D. Comparison to high voltage lithography

We have consistently observed smaller minimum feature sizes in the STM defined patterns than patterns written at 50 kV. On silicon, for example, 23 nm features have been written.[2] This is factor three smaller than has been defined with a 17 nm ($1/e$ diameter), 50 kV e-beam.[5] Most importantly, proximity effects are essentially eliminated.

The STM lithography demonstrates that the resist SAL-601 is inherently capable of sub-25 nm resolution. An upper limit can be put on the effect on feature size of the resist processing (e.g., diffusion of the acid catalyst) of 23 nm, the minimum feature size we have obtained in SAL-601. The question then remains as to why the resolution observed at 50 kV is much worse. The results described here suggest that it is the exposure process at 50 kV which is responsible for the resolution degradation. Indeed other studies of SAL-601 at the Naval Research Laboratory indicate that the resolution can be improved and proximity effects reduced by a thin dielectric layer between substrate and resist.[6,7] The indications are that the resist is more sensitive to the effects of secondary electrons than resists such as polymethyl methacrylate (PMMA) for which the exposure can be modeled more successfully.

These results indicate that it is not necessarily resist technology which is the limiting factor in determining the resolution of an e-beam lithography technique. Furthermore, there are significant advantages in using extremely low voltages for lithography in terms of the elimination of proximity effects and the achievement of smaller feature sizes.

E. Imaging

The ability of the STM to image with atomic resolution is well known. However, the surfaces associated with microfabrication are rarely sufficiently clean and ordered to exhibit atomic scale features. The main requirement for lithography is the ability to recognize alignment and registration marks with nanometer scale precision. Surface topographs are readily obtained from the STM operating in the field emission mode. A comparison of the imaging in the tunneling mode (-0.6 V tip bias, left image) and the field emission mode (-35 V bias, right image) is shown in Fig. 4. The line displacement plots are of the same 500 nm by 500 nm area of a tungsten film and have the same X, Y, and Z scales. Although more detail is apparent in the tunneling image, the corresponding features (particularly the depressions at front and back of the images) are readily

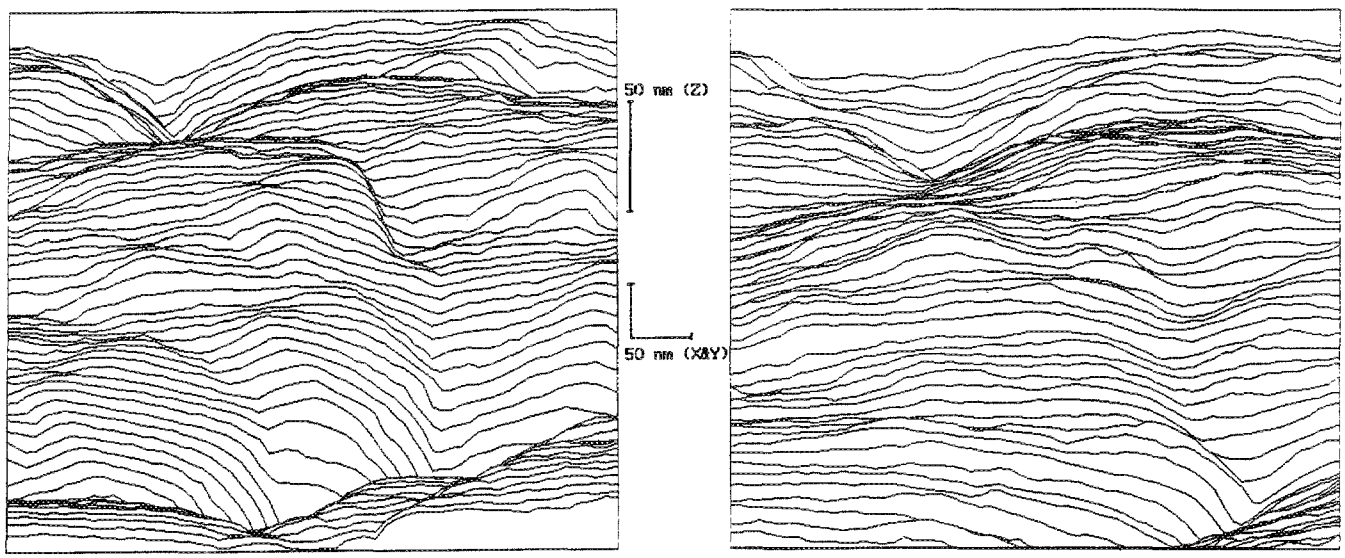

FIG. 4. The same surface imaged with the STM under tunneling, -0.6 V tip bias (left) and field emission, -35 V tip bias (right).

apparent in the field emission image. Further, in some cases, the lithographic exposure can be imaged *in situ* with the STM. The latent exposure image written at 50 kV has been imaged with the STM in an undeveloped polydiacetylene resist.[8] The exposed pattern appeared as depressions in the STM image, the apparent depth increasing with the 50 kV exposure dose. The ability to locate a pattern in an undeveloped resist film is a significant advantage for a mix and match lithographic scheme where an STM-based system is used to add very fine features to patterns defined with a lower resolution lithography.

III. A VIABLE LITHOGRAPHY

Our results have demonstrated that the STM can be used for lithography with an e-beam resist. Further, the resulting patterns are sufficiently robust to act as a mask for a reactive ion etch with boron trichloride. The results with the resist SAL-601 further demonstrate that there are specific advantages in using an STM (i.e., low energy) approach to e-beam lithography in that the resist resolution is enhanced and proximity effects are absent. In terms of registration, the imaging capabilities of the STM indicate that it is possible to align STM written patterns on a sample. However, significant challenges must be overcome before the technique can be considered viable outside the research laboratory. Here we concentrate on two specific issues, namely, positioning precision and speed, and discuss other advantages of very low voltage e-beam lithography.

A. Positioning accuracy

Although the linewidths of the features (letters) in Fig. 1 are uniform, the pattern is distorted because of the nonlinear response of the piezoelectric scanner in the STM. Although the configurations differ, all STM's use piezoelectric elements (usually tubes or slabs) to move the tip perpendicular to and in the plane of the sample surface. However, the voltage applied to the piezoelectric elements does not give a sufficiently accurate measure of the position of the STM tip. An independent measure of the tip position is necessary. For an STM instrument being developed for metrology,[9] a capacitance monitor has been used to reduce the positioning errors to better than 10 nm root mean square (rms) over a 7 μm scan. As the authors point out significantly better results should be possible from improvements in design and fabrication of the sensors. An optical technique for tip position measurement has also been described.[10] Thus there is a reasonable expectation that the problems associated with the nonlinear response of the scanners can be overcome.

B. Lithographic speed

The lithographic speed of the STM is determined by the maximum lateral velocity of the tip which is limited by the transient response of the STM servo loop.[11] Ideally the response is inversely proportional to the open loop gain of the servo loop. In practice the transient response is limited by the resonant frequency and/or the resonance damping of the scanner used to move the STM tip. To obtain the fastest transient response the resonance should be as high a frequency as possible and be critically damped. For example, by improving the damping of an underdamped tube scanner, its transient response was decreased from 2 to $\sim$0.2 ms because the servo loop could be operated at a higher gain.[11] More recently, with piezoelectric slabs with resonant frequencies in the MHz range, STMs have been built which can scan at video rates.[12] The pattern in Fig. 1 was written at a speed close to 0.5 μm/s in an instrument with a transient response of $\sim$4 ms. The instrument is only three years old, but an improvement of close to three orders of magnitude in speed has been demonstrated in instruments designed today.

TABLE I. "Mask" writing times for different numbers of tips.

No. tips	1	10	1000
Time, h	5×10^3	5×10^2	5

The STM probe can provide such a high current density that resist sensitivity is not a factor. In contrast, the resist exposure time is the speed limiting factor for nanolithography with our JEOL JBX-5DII operating with its smallest probe sizes. To make the point that an STM based nanolithography system would be comparable in terms of speed to the JEOL, the times required to expose a 100 μm line of 30 nm width have been estimated. For the STM, a lateral tip velocity of 1 mm/s is assumed. To write the line, a single pass at a tip-sample voltage chosen to give a 30 nm feature size would take approximately 0.1 s. For the JEOL a 30 nm linewidth requires a high resolution resist such as PMMA which has a low sensitivity of 2 nC/cm. A single pass line with a beam current of 100 pA would take $\sim$0.2 s. Thus at these dimensions, an STM based lithographic tool would give a comparable writing speed. For larger feature sizes, the advantage of the conventional lithography tool becomes marked. Significant increases in speed can be obtained through the use of more sensitive resists and higher beam currents.

Further increases in speed could be realized by the parallel operation of multiple STM tips, with each tip having its own piezoelectric scanner and servo loop. For example, an array of about 10 tips operating in parallel is feasible with conventional STM technology. Greater numbers of parallel STMs would require microfabrication techniques similar to that demonstrated in Japan and at Stanford University.[13] Incorporation of the control circuitry would also be feasible. Table I is an estimate of the time required to write a "mask" requiring 30 nm minimum feature sizes over a 4 cm^2 area with a 50% fill factor. It has been assumed that 50% of the writing would be performed at -15 V (30 nm effective spot size) and 50% at -50 V (100 nm spot). Thus 1000 is the order of magnitude of the number of tips required for this approach to full scale nanolithography. Such a number is well within the capabilities of present microfabrication technology.

C. Advantages of the low voltage approach

In ultrahigh resolution e-beam lithography, shot noise in the beam current causes an unacceptable variation in exposure, when the smallest resolved pattern element requires less than ~ 100 electrons for exposure. (For a resist sensitivity of 2 $\mu C/cm^2$, this corresponds to about 30 nm.) Our measurements suggest that SAL-601 requires about 100 times greater dose at 15 V than 50 kV. Therefore the problem of shot noise will become apparent at far smaller feature sizes with low voltage e-beam lithography.

As mentioned above vacuum operation is required because of the tip–sample voltages needed for lithography. If exposure could be performed at voltages close to 5 V, the STM could be operated at ambient pressure. An example of such lithography is the direct surface modification of Si (Ref. 14) and arsenic capped molecular beam epitaxy (MBE) grown III–V surfaces.[15] In both cases a thin surface oxide is formed when the tip–sample voltage is raised to around 5 V. Linewidths below 50 nm have been written. The oxide patterns have been transferred into InGaAs with a boron trichloride RIE. The surface modification can be imaged with the STM prior to any pattern replication allowing the latent exposure image to be inspected and corrected if necessary. Direct surface modification is clearly attractive as it is a "resistless" nanolithography. However, each different material requires a specific process to be developed for surface preparation, passivation, and lithography. Thus a resist based scheme has the advantage that it can be used with a wide range of substrate materials. As resist materials exist that can be exposed with photons of less than 5 eV in energy, it seems reasonable to expect a resist to be exposed with 5 eV electrons. The use of conductive resists and monolayer films is being explored to achieve this goal.

STM technology provides a very compact low voltage electron source. As a result, a low voltage system can be made far more compact than a conventional e-beam writer. This simplifies system design and engineering, especially in terms of sensitivity to mechanical vibration and stray magnetic fields. This suggests that the STM approach would be attractive for the development of a low voltage e-beam tool for nanometer scale lithography. One could envision such a tool being used in much the same way that converted SEMs are currently used for lithography at many institutions pursuing research and development.

IV. SUMMARY

Technologically useful low voltage e-beam lithography can be performed with the STM. The lithographic exposure of a commercially available e-beam resist and the transfer of the pattern into GaAs with a reactive ion etch has been demonstrated. Various advantages of low voltage e-beam lithography with the STM have been described. In particular, the absence of proximity effects gives an improved line to line resolution. The combination of the imaging and patterning capabilities of the STM indicate that STM based lithography will be particularly suited to a mix and match technology.

Issues related to transferring such lithographic techniques out of the research lab have been discussed. Significant challenges, particularly related to the speed of the lithography, are apparent. However, the technology exists to significantly impact these problems. Whereas a lithography tool capable of commercial mask making will require a significant investment, a tool for specialized lithography suited to the research and development environment is possible using existing technology.

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