IMPLEMENTATION OF SDC - SDF ARCHITECTURE FOR RADIX-4 FFT

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ABSTRACT

Very large scale integration and Digital signal processing are the very crucial technologies from the last few decades. DSP applications require high performance, low area and low power VLSI circuits. This paper is discussing about FFT which is one of the vital component in the digital signal processing. In this Paper, we propose a single path delay commutator–feedback (SDC-SDF) Architecture for Radix-4 FFT and presented its simulation and synthesis results. The Radix-4 FFT architecture consists of log4 N-1 SDC Stages and 1 SDF stage. Previously, the radix-2 SDC-SDF (Single path delay commutator-feedback) FFT architecture was includes log2 N-1 SDC Stages and 1 SDF stage. The proposed Radix-4 SDC-SDF architecture reduces the number of multiplications and additions as well as number of stages which achieves reduced area and low power. The resultant architecture is simulated using Modelsim, design verification and synthesis results are done using Xilinx ISE. The proposed architecture is compared with Radix-2 SDC-SDF FFT and it can achieve less area as well as low power consumption.

KEYWORDS

Radix-2 FFT, Radix-4 FFT, Single path delay commutator – feedback (SDC-SDF), Bit reverser.

1. INTRODUCTION

The Fast Fourier Transform (FFT) is one of the vital components in the field of digital signal processing. It is very helpful to calculate the discrete Fourier transform (DFT) accurately. DFT is one of the important operations in the field of digital signal processing. The DFT, with a transform length N equal to a power of 2, is usually implemented with the fast Fourier transform. Hardware designers are always tried to develop good architectures for the computation of the FFT to get high performance and real-time requirements of modern applications. Pipelined hardware architectures provide high throughputs and low latencies suitable for real time, as well as a low area and power consumption.

Fast Fourier Transform (FFT) is the vital component in orthogonal frequency division multiplexing (OFDM) systems [1]. OFDM has been adopted in a wide range of applications from wired- communication modems, such as digital subscriber lines , to wireless communication modems, such as IEEE802.11 Wi-Fi, IEEE802.16 Wi-Max or 3GPP long term evolution(LTE), to process baseband data.

Previously, some of them worked in this area and they also implemented some FFT architectures. They are Multi-path delay commutaor, single-path delay feedback and single-path delay commutator. MDC architecture [3]-[6] is used typically to process multiple- input data streams because of its high throughput rate. But it is not suited for single input data stream.MDC architectures require more hardware utilization compared to combined SDC-SDF architecture. The SDC-SDF (Single path delay commutator-feedback) architecture reduces the memory size and it can utilize multipliers fully. However the utilization of adders is still very low. SDC architecture is seldom used to process the single-input data stream, because it uses more memory resources than SDF and has a more complicated control.

Radix-2 FFT architecture mainly performs two operations. They are addition and subtraction. After completion of subtraction operation it indeed involves complex multiplication.

An FFT algorithm for radix's other than radix-2 one of the most important is radix-4. The radix-4 FFT was only used when N is the power of 4. We can achieve less computational complexity by using higher radix. The operation of radix-4 FFT is similar to the radix-2 FFT.

In radix-4 FFT, the sequence is divided into 4 sub sequences and each of which is again divided into 4 sub sequences and so on. In radix-4 FFT, the butterfly is based on the four point DFT. So radix-4 algorithm requires somewhat fewer multiplications than the radix-2 algorithm.

In this paper, we propose an efficient combined SDC-SDF (Single path delay commutator-feedback) radix-4 FFT architecture, which contains $\log_4 N$-1 SDC Stages and 1 SDF stage, and 1 bit reverser. This architecture can produce the output sequence as the same order of input [19].

2. THE COMBINED SDC-SDF RADIX-2 FFT

The existing single path delay commutator-feedback (SDC-SDF) radix-2 FFT architecture contains 1 pre-stage, $\log_2 N$-1 SDC stages, 1 post-stage, 1 SDF stage, and 1 bit reverser as shown in figure 1(a) [1]. The pre stage modifies the complex input data to a new sequence that is   real part and the corresponding imaginary part.

The SDC stages contain an SDC PE; it can achieve 100% arithmetic resource utilization through both complex adders and complex multipliers. The SDC PE, shown in figure 1(b), contains a real add/sub unit, a data commutator, and an optimum complex multiplier unit. In the stage t, the data commutator modifies its input data to generate a new data sequence and the index difference to get the new sequence is $N/2^t$, where t indicates the index of the SDC stage. The output of data commutaor is input to the real add/sub unit. The real add/sub unit consists of one adder and one subtracter.These two operations are performed for each input data.

Figure 1(b) is SDC PE for Radix-2 FFT consists of optimum complex multiplier unit. It contains 2 multiplexers, 2 multipliers, 1 real adder, and 1.5 word memory. The signal s operates the operation of the real adder that is both addition and subtraction operations.
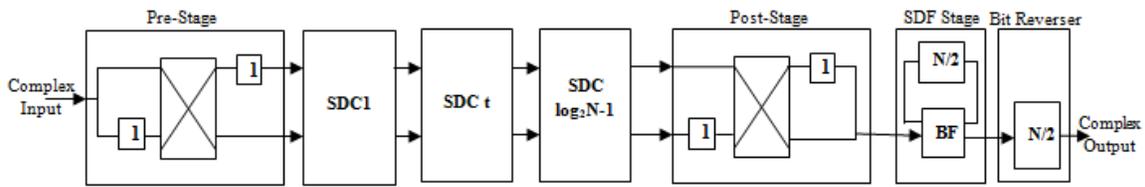
Figure 1(a). The combined SDC-SDF architecture for Radix-2 FFT
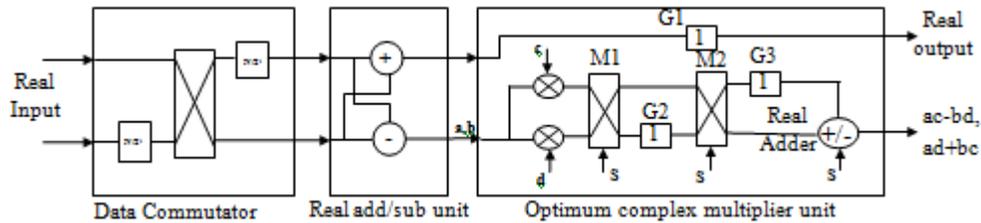
Figure 1(b). The SDC PE for Radix-2 FFT

The post stage changes back the new sequence to the complex format. The last stage is the single path delay feedback stage, which is similar to the radix-2 butterfly, requires a complex adder and a complex subtracter. By using the modified addressing method, the bit reverser requires only N/2 data buffer and we get the data in normal order.

3. PROPOSED SYSTEM

The main advantage of proposed SDC-SDF (Single path delay commutator-feedback) Radix-4 FFT architecture is we are applying inputs through single path and we are getting outputs through single path. The proposed single path delay commutator processing engine can require less number of complex multipliers and adders compared to the existing SDC-SDF (Single path delay commutator-feedback) Radix-2 FFT architecture.

The proposed SDC-SDF (Single path delay commutator-feedback) Radix-4 FFT architecture requires 1 Pre-stage, $\log_4 N - 1$ SDC stages, 1 Post-stage, 1 SDF stage and 1 bit reverser as shown in figure 2(a).

This architecture is based on Radix-4 Butterfly operation. That is 4 Operations are performed at the same time. The pre-stage changes the complex input data into real part followed by the imaginary part. For example initially the data in the form of 0_r,0_i,1_r,1_i etc., we get the output of pre stage as 0_r,1_r,2_r,3_r in the 1st cycle and 0_i,1_i,2_i,3_i in the 2nd cycle. Like that the pre-stage modifies the Complex input data into real part and the following imaginary part.

Next, the output of pre-stage is input to the SDC stages. Single path data commutator stages are depends on N value. The proposed architecture consists of $\log_4 N - 1$ or $\frac{1}{2} \log_2 N - 1$ SDC stages. Single path delay commutator processing engine consists of data commutator, Radix-4 butterfly and complex multipliers 1 and 2 as shown in figure 2(b). Data commutaor shuffles real input data to new data sequence, whose index difference is 3N/4, N/2, N/4. After generating the new data sequence, before going to the butterfly4, they were multiplied by complex multipliers1. Here k value varies from 0 to 3.

The operation of data commutator was performed in 4 cycles. In the first cycle k=0, second cycle k=1, third cycle k=2 and finally fourth cycle k=3. Depending on the k value the output of data commutators were multiplied by complex multipliers1.

Next block is radix-4 butterfly. In this it get the data from complex multipliers1. The main advantage of Radix-4 butterfly is they perform 4 operations at the same time. Internally radix-4 butterfly consists of adders/subtractors. It gets the 4 inputs and performs the addition/subtraction between these 4 sequences and finally generates the 4 outputs. The output of butterfly4 is multiplied by complex multipliers 2. This multiplication also depends on k value. Finally we get the 4 outputs as real output, complex output1, complex output2 and complex output3.
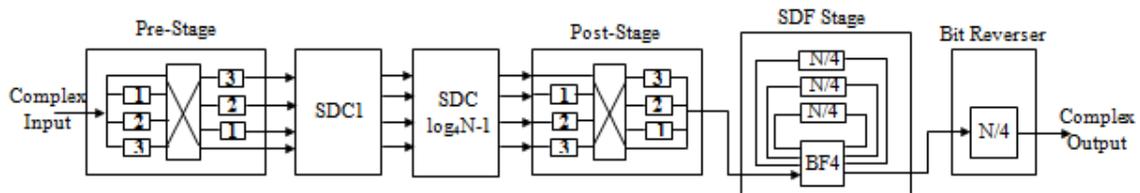
Figure 2(a). Proposed Architecture for combined SDC-SDF Radix-4 FFT
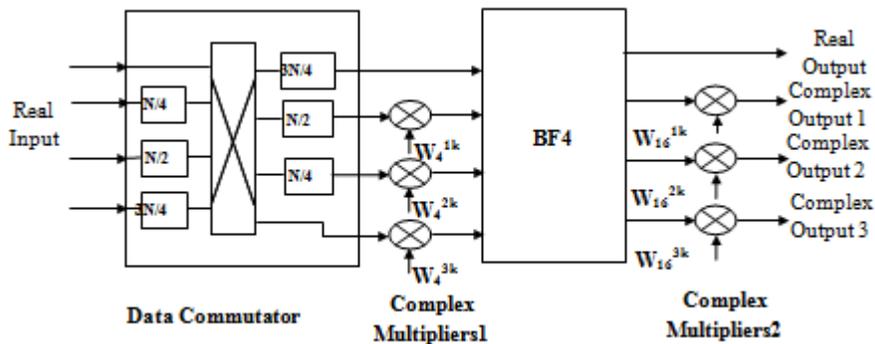
Figure 2(b). The single path delay commutator processing engine for Radix-4 FFT

The process can be continued by applying to the other couples (inputs) to the SDC1 and so on. If we perform the above process towards $\log_4 N - 1$ single path delay commutaor stages to Completion. Finally, we can complete the maximum part of the radix-4 FFT operation.

The output of SDC stages is input to the post stage. This stage was exactly opposite to the pre-stage. The post-stage shuffles the new sequence to complex input data. Next stage is SDF stage. It gets the input from post-stage. Single path data feedback consists of radix4 butterfly and thrice N/4 delay elements. The advantage of single path delay feedback stage to changes the data sequence, and then the delay memory is reduced to N/4 for the bit reverser. This combined SDC-SDF (Single path delay commutator-feedback) architecture produces the output in normal order as same as the order of input.

4. RESULTS AND COMPARISON

The design of combined SDC-SDF (Single path delay commutator-feedback) architecture for Radix-4 FFT has been made by using Verilog Hardware Description Language (Verilog HDL).

The simulation results has been evaluated by using Modelsim 6.3c and synthesis Performances are estimated by using Xilinx 14.1
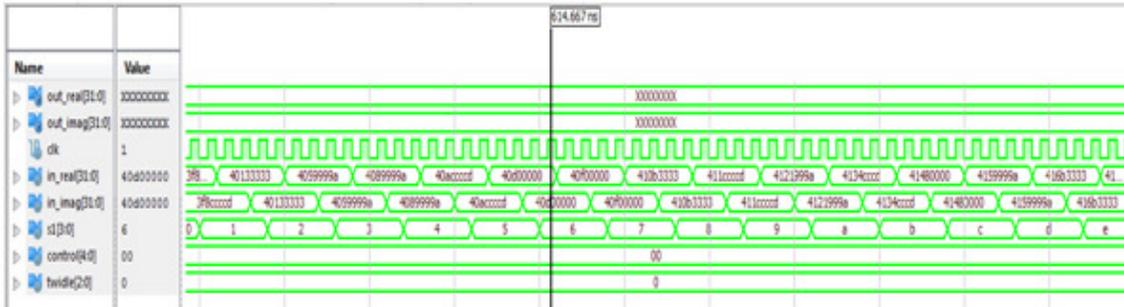
Figure 3(a). Simulation Waveform of Radix-4 SDC-SDF FFT

In Figure 3(a).complex input consists of real part and imaginary part. Here, in_real is the real part and in_imag is the imaginary part. Here, we are applying 16 inputs (complex) of 32 bit range through single path, clk, control as well as twiddle of 3 bit. Signal s of 4 bit represents number of inputs.
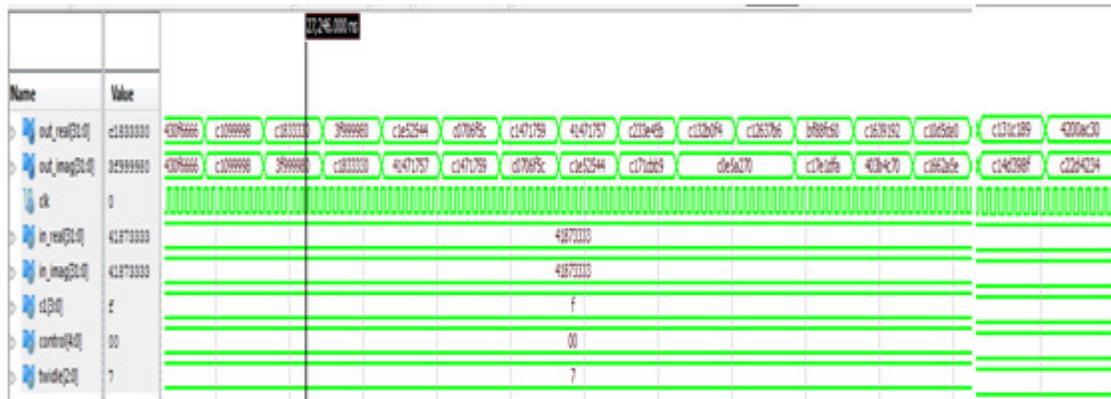
Figure 3(b). Simulation Waveform continue1 of Radix-4 SDC-SDF FFT

In Figure 3(b).complex output consists of real part and imaginary part. Here, out_real is the real part and out_imag is the imaginary part. After receiving 16 inputs (complex data), we are getting outputs (out_real and out_imag) through single path of 32 bit range.
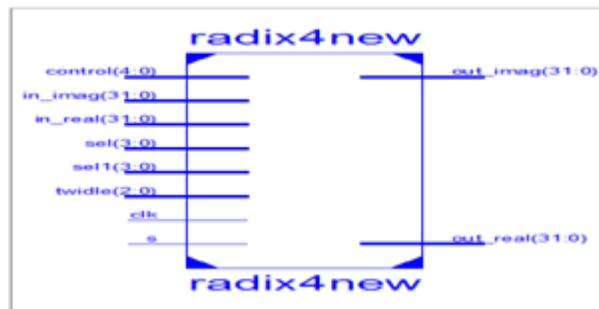
Fig. 4(a) RTL Schematic of Radix-4 SDC-SDF FFT

In Fig.4 RTL Schematic shows input and output signals.clk, in_real of 32 bit, in_imag of 32 bit, control of 5 bit, twiddle of 3 bit and s are inputs. Out_real of 32 bit and out_imag of 32 bit are outputs.
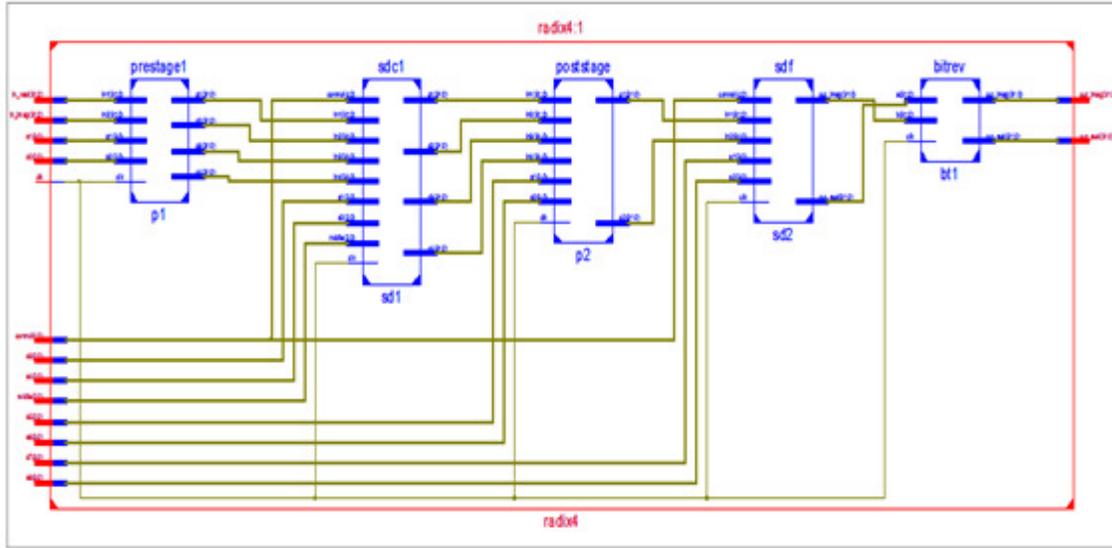
Fig. 4(b): RTL Schematic detailed view of Radix-4 SDC-SDF FFT

In Fig. 4(b) RTL Schematic detailed view of SDC-SDF (Single path delay commutator - feedback) Radix-4 FFT shows 5 blocks. They are 1 Pre-stage, 1 SDC Stage, 1 Post-stage, 1 SDF stage and 1 Bit-Reverser. The design was verified through this RTL Schematic view.

Table1: Design Summary of Single path delay comutator-feedback Radix-4 FFT

S.No.	PARAMETERS	VALUE
1.	No. of slice registers (in %)	2
2.	Number of slice LUTs (in %)	61
3.	Number of DSP 48E 1s (in %)	9
4.	Min. Clock period	39.473 ns
5.	Frequency	25.334 MHz
6.	On-chip logic	0.007
7.	Dynamic Power	0.047 W
8.	Quiescent Power	0.073 W
9.	Total Power	0.120 W

Single path delay commutaor–feedback Radix-4 FFT is compared with SDC-SDF (Single path delay commutaor–feedback) Radix-2 FFT in various parameters like dynamic power, quiescent power, number of slice registers, number of slice LUTs, and number of DSP 48E 1s. The implementation results give the same outputs, but in power consumption and area is less compared with SDC-SDF Radix-2 FFT.

Table2: Comparison between Single path delay comutator-feedback Radix-4 FFT and Radix-2 FFT

S.No.	Parameters	SDC-SDF Radix-2 FFT	SDC-SDF Radix-4 FFT
1.	No. Of slice registers (in %)	3	2
2.	Number of slice LUTs (in %)	72	61
3.	Number of DSP 48E 1s (in %)	25	9
4.	Dynamic Power	0.048 W	0.047 W
5.	Quiescent Power	0.073 W	0.073 W
6.	Total Power	0.122 W	0.120 W
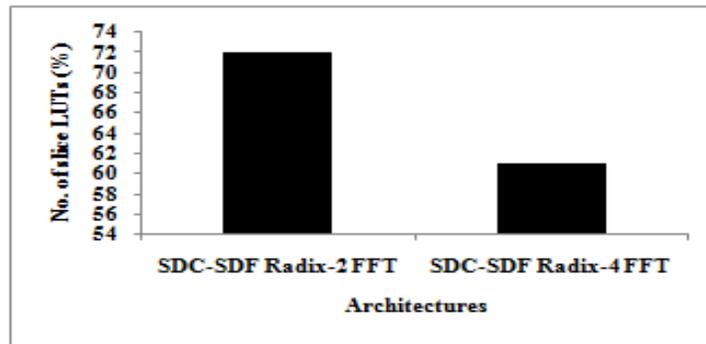
Fig.5 Comparison of Number of slice LUTs of SDC-SDF of Radix-4 and Radix-2 FFT

From Fig.5 we understood the Number of slice LUTs of single path delay commutator-feedback (SDC-SDF) Radix-4 FFT is less compared with SDC-SDF Radix-2 FFT. It says that output of SDC-SDF Radix-4 FFT is obtained as fast as compared to SDC-SDF Radix-2 FFT.
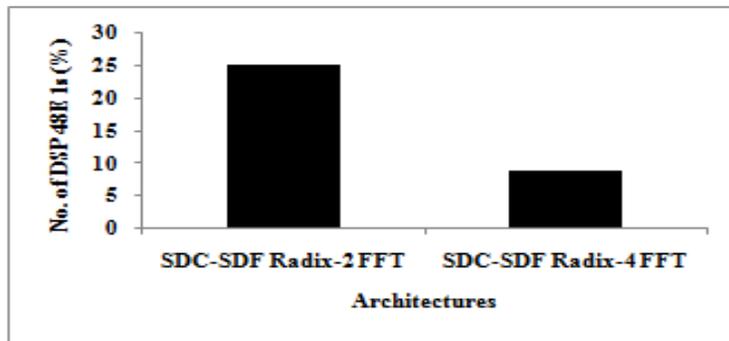
Fig.6 Comparison of Number of DSP 48E 1s of SDC-SDF of Radix-4 and Radix-2 FFT

From Fig.6 we understood the Number of DSP 48E 1s of single path delay commutator-feedback (SDC-SDF) Radix-4 FFT is less compared with SDC-SDF Radix-2 FFT. It says that output of SDC-SDF (single path delay commutator-feedback) Radix-4 FFT is obtained as fast as compared to SDC-SDF Radix-2 FFT.
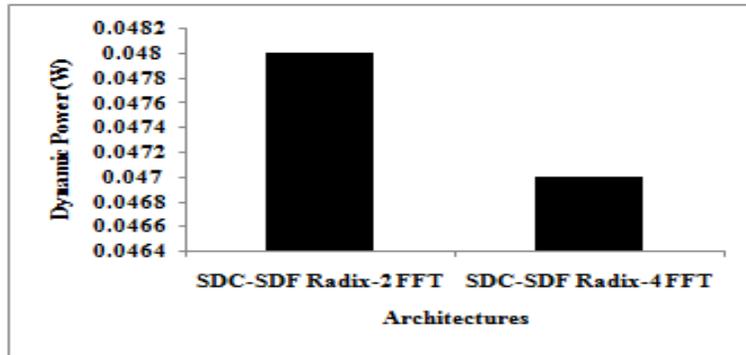
Fig.7 Comparison of Dynamic Power of SDC-SDF of Radix-4 and Radix-2 FFT

From Fig.7 we understood the Dynamic Power of single path delay commutator-feedback Radix-4 FFT is low compared with SDC-SDF Radix-2 FFT. It says that the SDC-SDF Radix-4 FFT is architecture performance is increased.
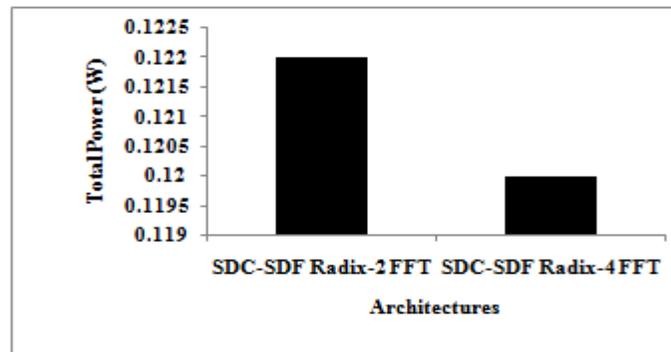
Fig.8 Comparison of Total Power of SDC-SDF of Radix-4 and Radix-2 FFT

From Fig.8 we understood the Dynamic Power of single path delay commutator-feedback (SDC-SDF) Radix-4 FFT is low compared with SDC-SDF Radix-2 FFT. It says that the SDC-SDF Radix-4 FFT is architecture performance is increased.

5. CONCLUSION

The proposed SDC-SDF (Single path delay commutator-feedback) radix-4 FFT architecture produces the output data in the same order as input. The proposed architecture reduces number of complex multiplications as well as number of stages compared with the radix-2 FFT architecture. The Single path delay commutator-feedback Radix-4 FFT architecture is simulated using Modelsim and design verification, area and power reports were done using Xilinx ISE 14.1. Finally, the proposed architecture can achieves reduced area and low power consumption.

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