Oxide Surface Roughness Optimization of BiCMOS BEOL Wafers for 200 mm Wafer Level Microfluidic Packaging Based on Fusion Bonding

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Abstract

200 mm wafer level microfluidic packaging is developed by low temperature oxide-oxide fusion bonding. The requirement for high quality fusion bonding is to have less than 1 nm microroughness on the wafer surfaces. An optimization process of the oxide deposition and planarization is done on the wafer surfaces. It is achieved to lower the microroughness from 2.08 nm to 0.4 nm without backside processes on the BiCMOS wafer and to 0.615 nm with backside processes on the BiCMOS processes after optimization.

Introduction

Silicon based 200 mm wafer level microfluidic packaging is a promising method for increasing the reliability and throughput of the systems and decreasing the overall costs [1]. In order to achieve the Si based wafer level microfluidic packaging, 200 mm wafer to wafer bonding is required. Plasma enhanced oxide-oxide fusion bonding is one of the potent methods to realize the wafer level packaging of microfluidics systems. For this type of bonding, there are strict surface quality requirements of the wafers [2,3]. As in many other applications [4,5], due to the strict roughness requirements of the oxide to oxide fusion bonding high level optimization is required for the oxide on the surface of the back-end-of-line (BEOL).

In this study, surface roughness of the oxide layer on top of the highest level of the BEOL metallization layer is presented. The optimized process on the oxide deposition brings surface roughness levels down to 0.615 nm, lower than 1 nm roughness which is the most critical requirement for the 200 mm wafer level oxide to oxide fusion bonding. Besides the roughness, oxide spikes on top of the edges of the highest level of metallization are also eliminated. Therefore, the surface is optimized and prepared for the high quality oxide to oxide fusion bonding on 200 mm wafers.

Standard Process Flow and Surface Roughness

In our microfluidic lab-on-chip (LoC) technology [6], we are realizing the microfluidic channels by bonding Si wafer with channel structures on top of BiCMOS wafer. On the surface of the Si channel wafer, there is 1 µm thick oxide layer for oxide to oxide fusion bonding and on the surface of the BiCMOS wafer, there is 2 µm thick oxide layer on top of the highest level of the BEOL metallization.

In detail, the last metal layer of BEOL has 3 µm thickness, thus high density plasma (HDP) oxide is needed to fill the gaps between metal structures on the standard process flow. On the standard process flow, 1500 nm HDP oxide is used to fill the gaps between highest level metals. 4500 nm plasma enhanced tetraethyl orthosilicate (PETEOS) oxide deposition follows HDP oxide to cover the step heights created on top of the metal layers. Later the oxide is planarized until 2 µm thick oxide left on the metal in the standard BEOL process. The simple forces flow can be seen in the Figure 1.

Both of these wafers should satisfy the surface roughness requirements for the fusion bonding. On the Si channel wafer surface, since this oxide is directly deposited on standard 200 mm Si wafer with standard deposition techniques and CMP planarization, we achieve 0.49 nm roughness (Figure 2). However on the BiCMOS wafer, due to the highest level of metallization, the roughness is around 2.08 nm (Figure 3) which is higher than the requirements. Additionally there are spikes around 2 nm on top of the metal edges which are acting like small particles on the bonding surface. Therefore optimization is required on the surface of the BiCMOS wafer.

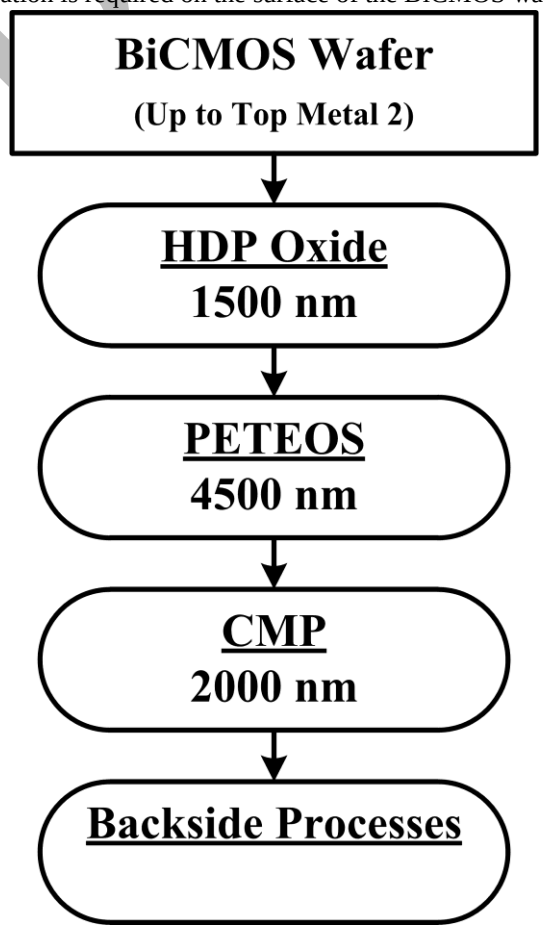

Fig. 1. Standard process flow for the microfluidic technology after highest level of metallization.

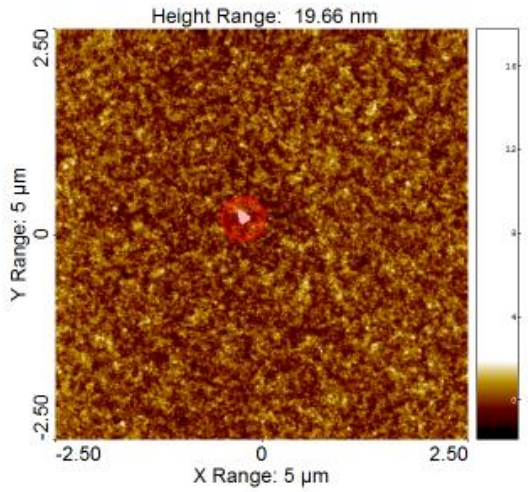

Fig. 2. AFM roughness analysis on the channel wafer. Rq=0.49 nm. Marked area removed in roughness analysis.

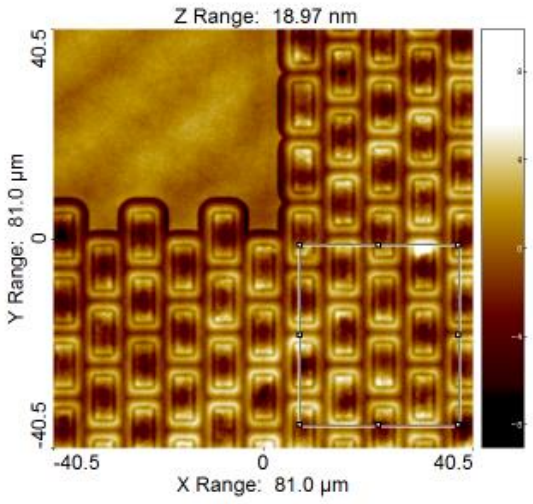

Fig. 3. Optical profiler image of the BiCMOS wafer. Rq=2.08 nm on the highlighted square.

Surface Roughness Optimization and Results

The optimization is started with varying this oxide stack thicknesses on top of the highest metallization level of the BEOL. The reason that it has been used two different oxides in the stack is to be able to fill the gaps between thick metal structures and get rid of the step height on the planarization. HDP oxide helps to fill the gaps in between the metal structures which have 3 µm thickness. PETEOS oxide deposition covers the step heights created by thick metal. Varying the oxide thicknesses in the stack changes the properties of the surface after planarization.

The oxide thicknesses in the stack are varied as in Table 1. The thickness of the HDP oxide is varied between 0 nm and 1500 nm; the thickness of the PETEOS oxide is varied between 4500 nm and 6000 nm; and the target thickness after CMP planarization is varied between 2000 nm and 2500 nm. The optimum stack and target thickness is obtained with AFM measurements. 1000 nm HDP + 5000 nm PETEOS oxide stack with 2500 nm target thickness gives the best roughness result of 0.4 nm which satisfies the requirement of oxide to oxide fusion bonding. It is clear from the results with the variations which can be seen in the table and the Figure 4 that when the planarized surface close to the HDP oxide, the surface roughness increases. This is caused by the stresses HDP and PETEOS oxide interface.

Table 1. Oxide stack variations

Variant No	Oxide stack			Roughness Result [nm]
	HDP Oxide [nm]	PETEOS Oxide [nm]	Target thickness [nm]	
1	1500	4500	2500	0.8
2	1500	5000	2500	1.1
3	1000	5000	2000	3
4	1000	5000	2500	0.4
5	0	6000	2000	0.9
Fig. 2	1500	4500	2000	2.08

The high density created by electric fields on the deposition of the HDP oxide. The electric field density on the edges of the metal is higher than the remaining parts, therefore the oxide deposited on the edges of the metal structures have higher densities and higher stresses. When PETEOS oxide deposited on top of HDP oxide, the stresses created on the interface between HDP and PETEOS moves up to the surface. Since the surface is planarized by CMP process and the thickness above HDP oxide is decreased, these stresses become more visible on the surface.

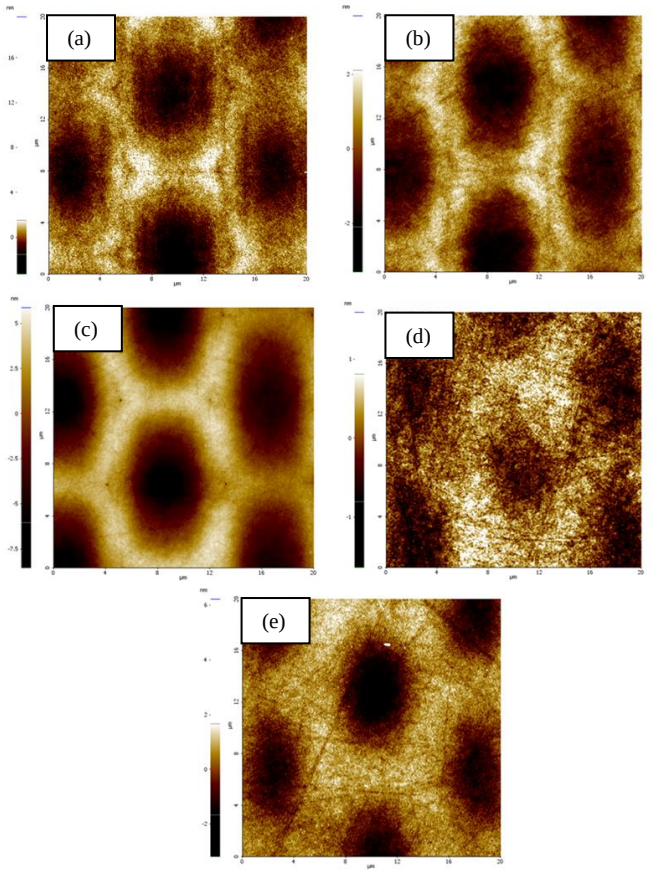

Fig. 4. AFM roughness analysis on the variants in Table 1. (a) variation no. 1. Rq=0.8nm. (b) variation no. 2. Rq=1.1nm (c) variation no. 3. Rq=3nm. (d) variation no. 4. Rq=0.4nm. (e) variation no. 5. Rq=0.9nm.

In our microfluidic LoC technology, we continue the fabrication of BiCMOS wafer with the backside process for the microfluidic inlet and outlet for the system [6]. After the backside processes, the surface roughness increases to 1.78 nm (Figure 5). The increase in the roughness is due to the wafer handling and the chuck contact of the front surface of the BiCMOS wafer. In order to get a flat surface after the backside processes, another CMP planarization is required. However the results from the oxide stack variations show that, as the target thickness of oxide after CMP decreases, the surface roughness increases. Consequently it is applied the two step planarization for the optimization.

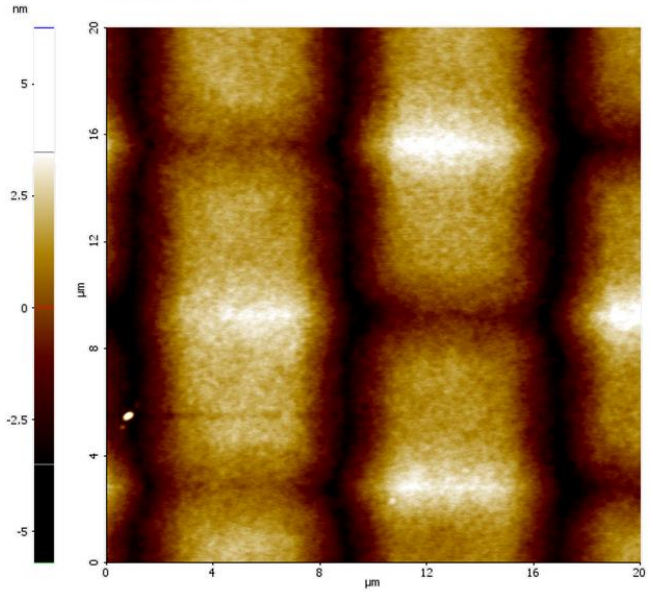

Fig. 5. AFM roughness analysis on the BiCMOS wafer after backside processing. Rq=1.78 nm

In order to have surface requirements for the wafer bonding, another PETEOS oxide deposition and planarization are applied on the surface after backside processes. The final process flow with the second oxide deposition and planarization after backside processes can be seen in the Figure 6. On the second deposition 1000 nm PETEOS oxide is used. After the deposition wafer surface is planarized back to the first target thickness. By this way any scratches and particles created on the front side of the BiCMOS wafer due to the contact with the chucks of the tools can be eliminated. The AFM measurements show that the surface roughness decreased to 0.615 nm (Figure 7) after the second planarization. At the end roughness requirements are met and they are ready for the fusion bonding to finalize microfluidic LoC systems.

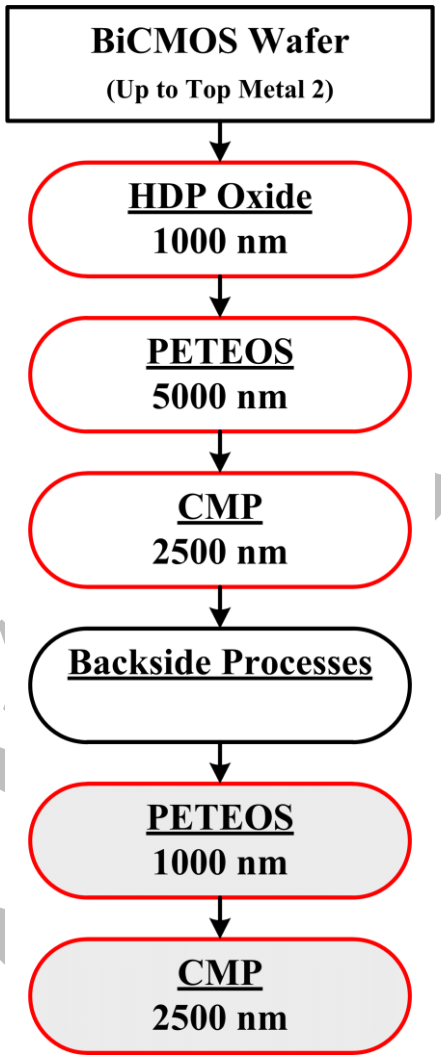

Fig. 6. Optimized process flow for the microfluidic technology after highest level of metallization.

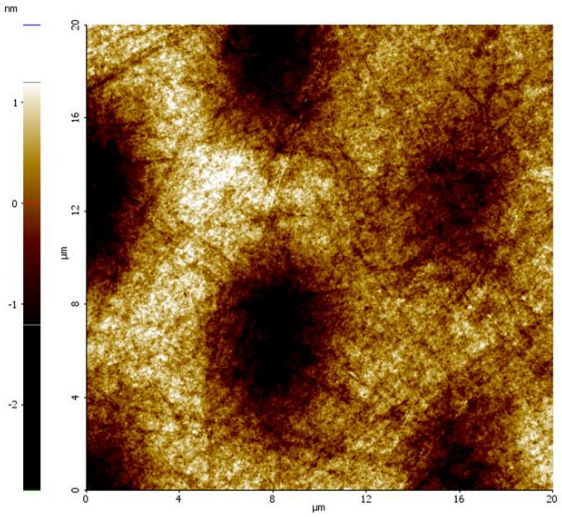

Fig. 7. AFM roughness analysis on the BiCMOS wafer after optimization. Rq=0.615 nm

Conclusion

In this work, surface roughness of the 200 mm BiCMOS wafer is optimized for low temperature fusion bonding to be used in microfluidic LoC systems. The measurement results show that it is required to have detailed investigation and optimization to have less rough surfaces for the high quality 200 mm wafer level fusion bonding. Since the last metal layer on the BEOL of the BiCMOS layer is 3 µm, HDP is used to fill the gaps between the metal structures. Without backside process, by using 1000 nm HDP + 5000 nm PETEOS oxide stack the surface roughness is decreased to 0.4 nm. After the backside process, with the help of the second oxide deposition and planarization, the surface roughness is decreased to 0.615 nm. This optimization method will increase the bonding quality for the 200 mm wafer level LoC microfluidic packaging, which leads to have high reliability and low cost on these systems.

Acknowledgments

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References

1. Kaynak, M., "BiCMOS Integrated Microfluidic Platform for Bio-MEMS Applications," *IEEE MTT-S International Microwave Symposium (IMS)*, Tampa, FL, 2014.
2. Christiansen, S. H., "Wafer direct bonding: From advanced substrate engineering to future applications in micro/nanoelectronics." *Proceedings of the IEEE*, 94(12), 2006, pp. 2060-2106.
3. Alam, A. U., "The effects of oxygen plasma and humidity on surface roughness, water contact angle and hardness of silicon, silicon dioxide and glass." *Journal of Micromechanics and Microengineering*, 24(3), 2014, 035010.
4. Ismail, M. S., "Polysilicon and Titanium Disilicide + Polycide Fusion Bonding for #-D Microdevices Applications," *5th Technical Digest, Solid-State Sensor and Actuator Workshop*, 1992, pp. 86-89.
5. Peng, L., "Development of multi-stack dielectric wafer bonding." *Electronic Packaging Technology (ICEPT), 2016 17th International Conference on*, 2016, pp. 22-25
6. Inac, M., "BiCMOS Integrated Microfluidic Packaging by Wafer Bonding for Lab-on-Chip Applications," *Proc 67th IEEE Electronic Components and Technology Conference (ECTC)*, Orlando, FL, 2017, pp. 786-791.