HIGH SPEED AND LOW POWER FLASH ADC DESIGN

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ABSTRACT:

The Analog to Digital converters play an imperative role in today's electronic systems world. Current applications need High Speed and Low Power ADC. Flash ADC is most prevalent not only for its highest transformation rate but also for its use in other ADC types and its varied applications. Traditional N-bit flash ADC necessitates 2^{N-1} comparator and same number of preamplifier. if we use multiplexer to design FLASH ADC number of Comparator and Preamplifier get reduced also use of mux in Thermometer to binary code encoder will reduce delay which will ultimately reduce overall power consumption ,area and will rise the speed of operation. KEYWORDS: Flash ADC, Multiplexer, Pramplifier, Comparator Thermometer To Binary code Encoder.

I. INTRODUCTION:

Flash ADC's, also known such as parallel ADCs, are the firmest in converting an analog signal to a digital signal. Which are used in various applications in which higher speed and resolution required such as wireless communications and digital audio and video, Radar Processing ,High Density Disk drive,[1][2].There are numerous types of architectures, each with distinctive characteristics and different limitations [1].One of the design which is used for converting continuous time changing signal to digital signal is Flash ADC [1].

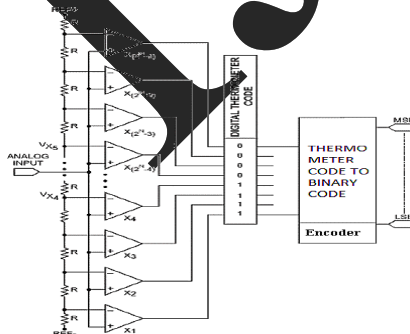## II. EASE OF USE:

A. TRADITIONAL FLASH ADC:

Fig 1 Traditional Flash ADC

The Resistor ladder setup generates the reference voltages for the every Comparator. The reference voltage for each Comparator is1 LSB less than the locus voltage for

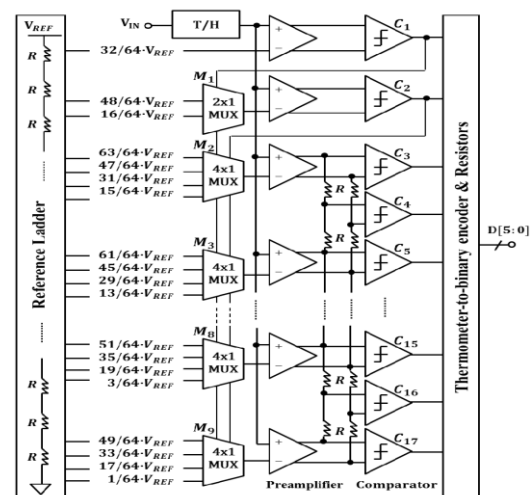the Comparator promptly upstairs it. When the input voltage (positive terminal) is superiorthan the locus voltage (negative voltage) of Comparator it produces a "1", otherwise, the Comparator productivity is "0". If the analog input is in among V_{x4} and V_{x5} , then the Comparators X1 throughX4 foods "1"s and all the left over Comparators produce "0"s. The Comparators will generate a Thermometer code of an input signal. This code will then encode into a Binary form by T To B Converter. They are typically stumpy Gain since at great Frequencies it is not easy to obtain together wide Bandwidth and high Gain. The main problem with the Traditional flash architecture is that the number of comparators surges diacritically with the number of bits. Due to the huge number of comparators the number of bits is usually inadequate, since the area of chip and consumed power would be too bulky for upper determinations. The big number of comparators sources the large input capacitance [3]. To drive such a large input capacitance, preamplifiers are needed but preamplifiers consume extra power, so it is imperative to reduce the quantity of input preamplifier pairs [4]. The interpolation techniques are used to lessen the number of preamplifiers, but the quantity of comparators still remnants at $2^N - 1$ for an N-bit ADC. On the other hand, the future ADC architecture using multiplexers needs less quantity of comparator and preamplifier too.

B. PROJECTED FLSH ADC DESIGN:

Fig 2 New Flash ADC Design

can be abridged by half, resulting in the total count of comparators of $2^{(N-2)} + 1$. The number of preamplifiers required is also abridged from $2^{(N-2)} + 1$ to $2^{(N-3)} + 2$ since the interpolate by two technique used.

Abbreviations and Acronyms

LSB-Least Significant Bit , MSB –Most significant Bit

C. TABLES AND FIGURE OF RESULT:

TABLE I.   PARAMETERS

SPECIFICATION	REF NO[7]	REF NO[8]	REF NO[9]	PROJECTED DESIGN
TECHNOLOGY	0.35um	90nm	90nm	0.18um
SUPPLY VOLTAGE (v)	3.3	1	1.2	1
POWER(mw)	19.2	72	12	0.23
ENOB(BIT)	-	-	4.94	5.95
RESOLUTION	6	6	6	6

TABLE II.   NUMBER OF COMPARATOR AND PREAMPLIFIER

No. of Bit (N)	Traditional Flash ADC		New Designed Flash ADC	
	Comparator(2^{N-1})	Preamplifier (2^{N-1})	Comparator $(2^{N-3}+1)$	Preamplifier $(2^{N-3}+2)$
4	15	15	5	4
6	63	63	17	10
8	255	255	257	130
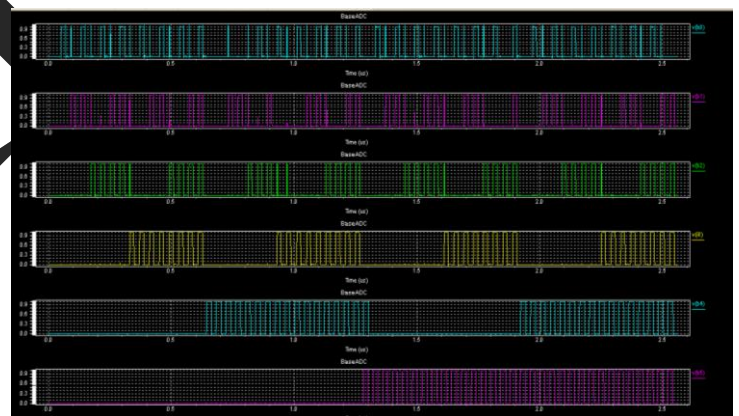
Fig 4. Newly Designed Flash ADC waveform 1

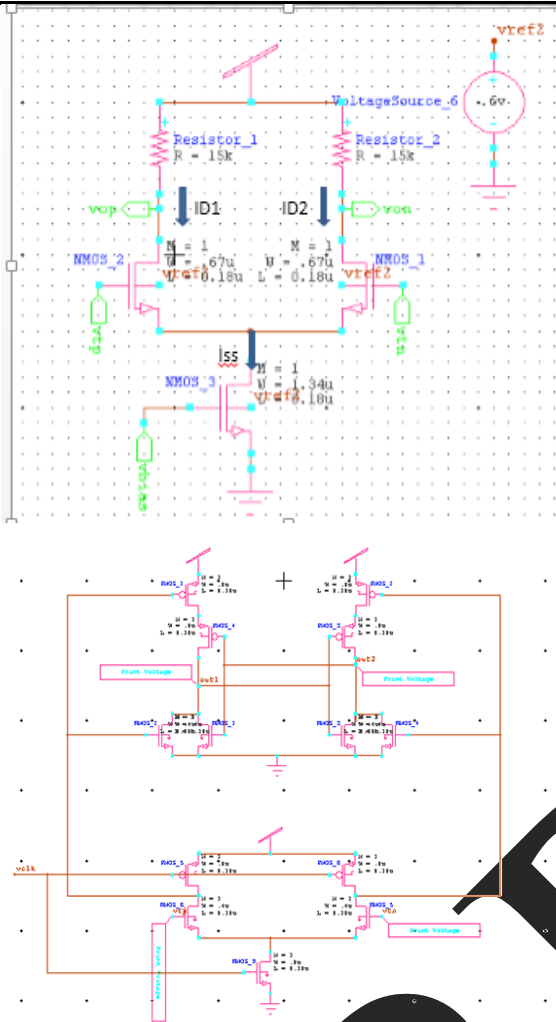Fig 5. Newly Designed Flash ADC waveform 2

Fig 3 Preamplifier and latch Comparator[5]

The first comparator, C_1 compares the sampled and amplified input signal with the central reference level, $32/64 \cdot$ VREF1.It chooses the MSB of the digital output and the MSB becomes the switch signal for the MUXs,M1 – M9. The subsequent comparator, C_2, does the same but its reference signal is either $16/64 \cdot$ VREF 2 or $48/64 \cdot$ V throughthe (2x1)-MUX, which is determined by the switch signal from the production of the first comparator. And then these twoMSBs, the outputs of the first and subsequent comparators, decide thereference voltages for the left over comparators, C_3 to C_{17}through (4x1)-MUXs.Thequantity ofpreamplifiersreduce by (4x1)-MUXs, the interpolation techniqueusing two resistors is applied. The outputs of the left overcomparators are set into appropriate values and then alldigital bits are output at the matching time.Projected design needs only $2^{(N-3)} + 2$ preamplifiers and $2^{(N-2)} + 1$ comparators. The quantity of comparators needed for the projected ADC can be calculated as below. the first comparator (C_1) picks the MSB with the central referencelevel, and due tothe use of the subsequent comparator (C_2) with the $1/4 \cdot$ VREF and $3/4 \cdot$ VREF the quantity of comparators apart since these two (C_1 and C_2)

CONCLUSION:

The FLASH Analog to Digital converter architecture is the good solution for high Speed Analog to Digital converter Design. To achieve Power and Speed trade of we used Dynamic latch Comparator along with multiplexer and interpolation technique to reduce comparator count. Design is done in 180nm Tanner Tool, power Consumption for this circuit is $2.3 * 10^{-4}$w and delay is **3.4us** which is very less. So low power and high speed operation achieved

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