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Metal-Oxide-Semiconductor-Only Process Corner Monitoring Circuit

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***Abstract*—**A process corner monitoring circuit (PCMC) is presented in this work. The circuit generates a signal, the logical value of which depends on the process corner only. The signal can be used in both digital and analog circuits for testing and compensation of process variations (PV). The presented circuit uses only metal-oxide-semiconductor (MOS) transistors, which allow increasing its detection accuracy, decrease power consumption and area. Due to its simplicity the presented circuit can be easily modified to monitor parametrical variations of only n-type and p-type MOS (NMOS and PMOS, respectively) transistors, resistors, as well as their combinations. Post-layout simulation results prove correct functionality of the proposed circuit, i.e. ability to monitor the process corner (equivalently die-to-die variations) even in the presence of within-die variations.

***Keywords*—**Detection, monitoring, process corner, process variation.

I. Introduction

WITHIN decades, scaling of complementary metal-oxide-semiconductor (CMOS) technologies has played a critical role, significantly improving performance of devices and circuits [1]. In modern deep submicron technologies, different factors including newer effects in MOS transistors impede the continuous scaling. PV [2], [3] are considered to be a very important to target since they adversely affect integrated circuits' (IC) performance, particularly decreasing their yield.

In addition to PV characterization [4], lots of techniques and circuits have been developed [5]-[8] to design robust circuits, detect PV, compensate their impact. Development of PV detection and compensation circuits is in its turn challenging. Modern PV monitoring circuits use several metrics to get information on PV - logic gate delays and slew rates [7], [8], transistor leakage currents [5], [6], transistor threshold voltage, dynamic current etc.

II. Existing Techniques

Most of modern PCMCs use a common principle of "measurement", when a variable (metric) subject to variation is compared with a reference one. The widely used reference variables (or sources) are voltage, current [6] and frequency [5]. After comparison with a reference variable, digital or analog signals are generated, the value of which characterizes the process corner. These signals are then used as PV indicators, or for compensation [9] in different analog and digital circuits.

In [5] the subthreshold leakage current of MOS, the transistor is used for PV monitoring; a simplified block-diagram of the circuit is shown in Fig. 1. It consists of a reference current and voltage sources (I_{ref} and V_{ref} respectively), current mirror (transistors M_0 and M_1) and a transistor (M_2) operating in subthreshold region.

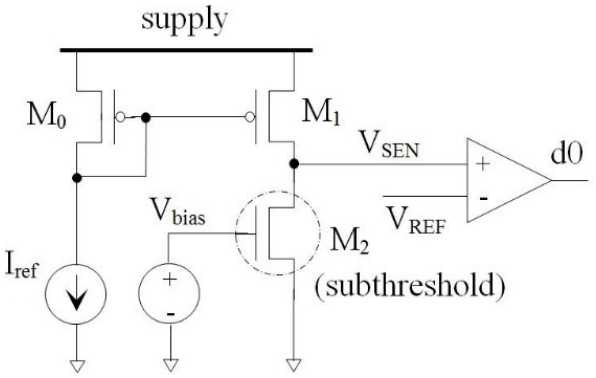

Fig. 1 Simplified block diagram of the PCMC proposed in [5]

For the proposed leakage sensing circuit to reflect only the variation in M_2 and not the variation in the rest of the circuit, both I_{ref} and V_{bias} must be designed to be PV insensitive. V_{SEN} is the drain voltage of M_2 that indicates the leakage level and is determined by the equilibrium of the M_1, M_2 drain currents and corresponds to the voltage at the intersection point of the load lines, as in Fig. 2. Since the current I_{ref} is insensitive to PV, while I_{M2} strongly depends on PV (via threshold voltage, etc.), output voltage V_{SEN} changes with PV. E.g. in "fast" corner I/V characteristics of the M_2 "move up", consequently, smaller output voltage is generated, and thus, depending on process corner (or PV), high or low voltage is generated. V_{SEN} is then compared with V_{REF}, generating a digital signal (d0).

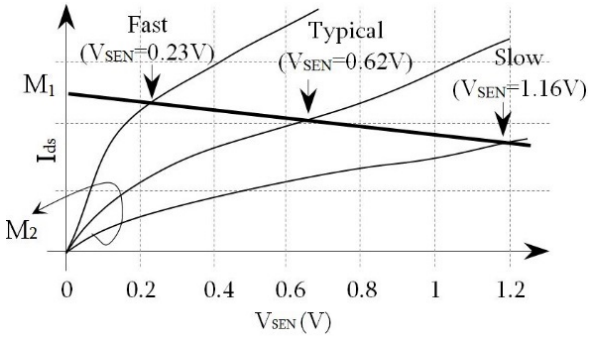

Fig. 2 Current-voltage characteristics of transistors M_1 and M_2 of the PCMC proposed in [5]

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A block diagram of the slew-rate monitoring circuit, described in [7] is shown in Fig. 3. It consists of an oscillator, comparators, XOR gate, multiplexer and a charge pump. The oscillator generates a digital signal, which drives comparators A and B. They have different voltage threshold levels (80% and 20% of the supply, respectively). These levels are used to measure rise and fall times of a single pulse. Comparators' output signals drive the XOR, which generates two subsequent pulses. The pulse width of the first (R) and second (F) pulses are equal to the rise and fall slews of the input signal respectively. By selecting these pulses (at different time points) multiplexer "MUX" generates two signals (PR and PF): one corresponding to the rise edge and another to the fall edge. The signal "PR" charges the capacitor of the charge pump (CP), while "PF" discharges it back. The output voltage of CP is proportional to the difference between rise and fall slews of the input signal. The output voltage can then be used in voltage controlled oscillator (VCO). Measuring VCO's frequency PV can be monitored.

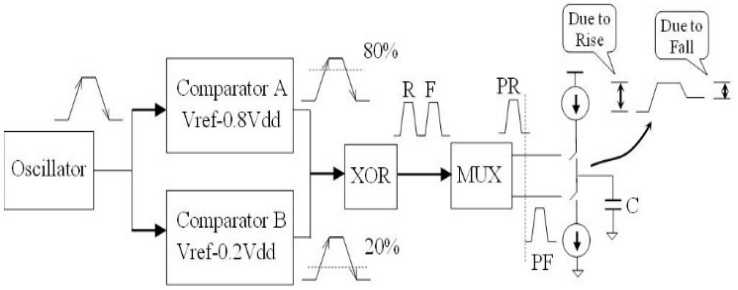

Fig. 3 Simplified structure of the PCMC, proposed in [7]

Most of the modern PCMCs suffer from several drawbacks, which limit their usage in various applications. One drawback is the usage of reference voltage/current sources. There are tradeoffs between reference voltage/current variation and area/current consumption, since very accurate sources use bipolar transistors and resistors, and have larger area, consume more current, while low-area sources based on only MOS transistors, have lower accuracy (larger variation). These tradeoffs affect PCMC's performance significantly. The next factor is the presence of one or more converters, e.g. voltage-to-voltage/code converter, current-to-frequency converter (oscillator), all of which suffer from PV, i.e. usage of parameter conversion creates additional process dependency, worsening PCMC's performance.

III. Proposed Circuit

The proposed PCMC is shown in Fig. 4. It is a self-biased [10] circuit with positive and negative feedback loops. The first loop consists of transistors M_1 and M_2, while the second loop consists of transistors M_3-M_6. Due to specific "shape" of voltage transfer characteristics (V_1 vs. V_{out} and V_2 vs. V_{out}) of both loops stable operating points, and hence, output voltage (V_{out}) are formed.

The operation principle of the circuit is based on a "shape" of the transfer characteristics which are designed in a way that in some corners the circuit has a non-zero operating point (the plots have a non-zero crossing point), while in other corners it has zero operating point (the plots cross at zero). Thus, due to process corner change the output voltage (V_{out}) changes from certain voltage to 0 (or vice versa). To illustrate the operation principle of the circuit, it is necessary to first derive transfer characteristics of both loops.

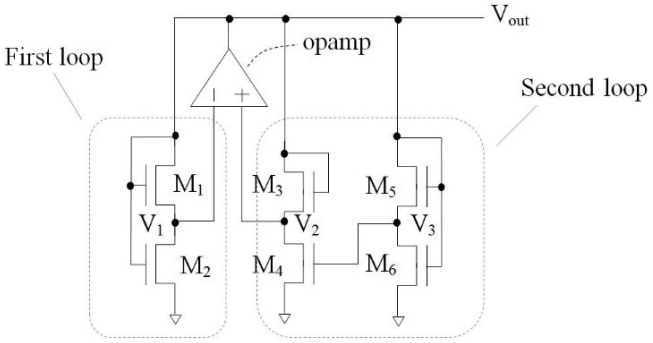

Fig. 4 Structure of the proposed PCMC

Since the transistors operate in different regions (strong inversion, weak inversion), it is necessary to derive the transfer characteristics using different equations for corresponding regions. In the first loop at small (smaller than threshold voltage of transistors) input voltages (V_{out}), both transistors M_1 and M_2 operate in the subthreshold region where current-voltage dependence is exponential [11]. Since the dependence (V_1 vs. V_{out}) cannot be expressed analytically, we do vice versa, by calculating the dependence of V_{out} on V_1

$$V_{out} = V_1 - V_T ln\left(1 - s_1 e^{\frac{V_1}{mV_T}} + s_1 e^{\frac{V_1(1-m)}{mV_T}}\right) \quad (1)$$

where V_T is the thermal voltage, $s_1=\beta_{m2}/\beta_{m1}$, $\beta_i=\mu_n C_{ox} W_i/L_i$, μ_n is the mobility of carriers in channel, C_{ox} is oxide capacitance per unit area, W_i/L_i are channel width/length of i-th transistor. At large (larger than threshold voltage of transistors) input voltages (V_{out}) both transistors M_1 and M_2 operate in strong inversion region [10], transistor M_1 is in saturation, while the M_2 is in linear region. Using the square law model [10] for current-voltage characteristics of the transistors, we obtain:

$$V_1 = (V_{out} - V_{th})\left(1 + \frac{\sqrt{s_1 - 1}}{s_1 + 1}\right) \quad (2)$$

where V_{th} is the threshold voltage (zero-bias) of n-type MOS (NMOS) transistors. At the input voltages close to threshold voltage there is no simple analytical equation for the transistors to derive the transfer characteristics. Such analysis, however, is not necessary, since (1) and (2) are enough to explain the principle of operation of the proposed circuit. Transfer characteristics (first loop) described by (1) and (2) are shown in Fig. 5 (curve V_1). At small input voltages the characteristics do not depend on process corner (or, equivalently, threshold voltage), while at large values there is negative dependence. Note that in modern submicron and deep submicron CMOS technologies, the threshold voltage has much higher variation than the other parameters, such as oxide thickness, mobility, channel length modulation parameter, etc. [12]. For this reason, under PV we understand threshold voltage variation. Also, since the proposed circuit uses long-channel transistors, short-channel effects [11] are not taken into account.

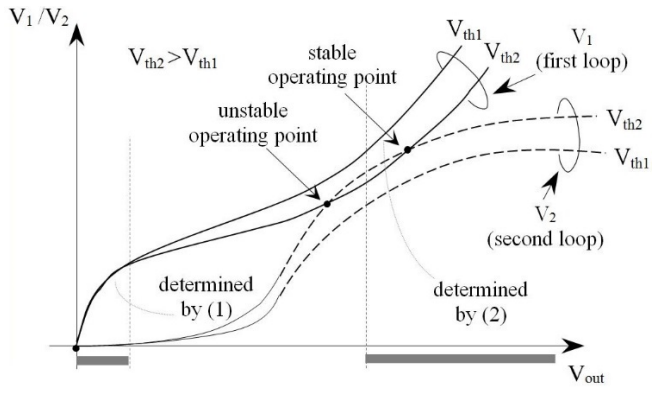

Fig. 5 Transfer characteristics of the first and second loops of the proposed PCMC

In the second loop, transistors M_5 and M_6 work in the same regions as transistors M_1 and M_2. At small values of V_{out} both transistors M_3 and M_4 operate in subthreshold region, while at large values (greater than the threshold voltage) M_3 operates in strong inversion region. M_4 remains in subthreshold region, since its gate voltage (V_3) is smaller than the threshold voltage, which can be proved by applying (2) to those two transistors. This is true as long as V_{out} is much greater than threshold voltage ($V_{out} >> 2V_{th}$). Since the operating range of the circuit V_3 is smaller than $2V_{th}$ (but larger V_{th}), we will assume the subthreshold region for M_4 and strong inversion region for M_3; using the same equations for both transistors, we will obtain for voltage V_3:

$$V_2 = V_{out} - V_T d e^{\frac{cV_{out} - (c+1)V_{th}}{2mV_T}} \quad (3)$$

where $d=\sqrt{(2\beta_{m4}/\beta_{m3})}$, $c=1+\sqrt{(b-1)/(b+1)}$, $b=\beta_{m6}/\beta_{m5}$. Transfer function described by (3) is shown in Fig. 5 (curve V_2).

Fig. 5 shows that there are three crossing points of curves V_1 and V_2 - one zero and two nonzero points. One of those two points is unstable, so the system cannot remain in that state indefinitely. Thus, there are two stable (working) operating points. Depending on corner (threshold voltage value) the circuit changes its state from non-zero to zero operating point (or vice versa) generating a digital signal (V_{out}).

To prove that the proposed circuit can detect the process corner, we show that curves V_1 and V_2 have a nonzero crossing point at certain values of threshold voltage, but have zero crossing point at other values, i.e. we show that "shift" of the curves causes crossing point "shift". For that purpose, the derivatives of both voltages with respect to threshold voltage are calculated. Note that V_{out} is assumed constant and the derivatives are calculated for a range near the stable operating point. Also, variation of the oxide thickness and the rest of parameters are assumed constant, since they are too small. Using (2) and (3) derivatives of V_1 and V_2 are calculated:

$$\frac{\partial V_1}{\partial V_{th}} = -\left(1 + \frac{\sqrt{s_1 - 1}}{s_1 + 1}\right) < 0 \quad (4)$$

$$\frac{\partial V_2}{\partial V_{th}} = \frac{V_{out} - V_{th}}{V_T V_2} \cdot \frac{c+1}{2m} > 0 \quad (5)$$

Equations (4) and (5) show that both derivatives have different signs, which means that curves V_1 and V_2 (Fig. 5) move in opposite directions, which in its turn means there is change in operating point (hence V_{out}) location. Thus, threshold voltage change leads to V_{out} change. Properly designing the circuit swing of V_{out} can be made high enough to be used as a digital signal in digital and analog circuits.

Since the voltages V_1 and V_2 are smaller (close to 0.2V) than the threshold voltage, the operational amplifier (OA) uses PMOS transistors in the input differential stage. The structure of the OA is shown in Fig. 6. It is a simple two-stage amplifier which main purpose is to provide high gain. Since there are no strict requirements on the OA, many other structures, providing high gain can be used [10]. Due to its high gain the OA equalizes the voltages V_1 and V_2 generating a stable operating point.

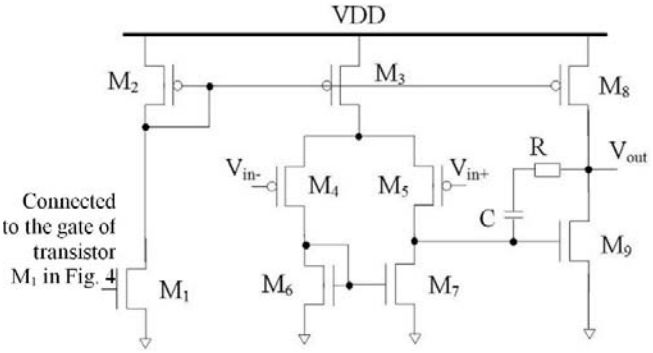

Fig. 6 Structure of the operational amplifier (OA) used in the proposed PCMC

Note, that since the circuit has zero operating point, which is stable, it may remain in that state indefinitely after "power-up", which will cause circuit malfunctioning. To avoid that, the

voltage V_{out} should be forced to large value (above stable operating point). Corresponding circuit (forcer) is not shown, since it is not critical block and can be implemented in various ways. After forcing and then releasing (the forcer is off), the system will fall into one of the stable operating points depending on process corner.

While the proposed PCMC deals with process corners, the temperature is assumed constant during its operation. This condition is easily implemented, since the proposed circuit operates when the IC is in testing mode. During testing, the temperature is set to a certain value and kept constant. For this reason, all the equations and statements are derived based on the assumption of constant temperature.

The circuit in Fig. 5 uses only NMOS transistors; consequently, its operating points and output voltage are determined by their parameters, i.e. threshold voltage of NMOS transistor; that is, threshold voltage variation of NMOS transistor is detected via the proposed circuit. In a case if variation of more parameters needs to be detected, the circuit should be modified. In a case of threshold voltage of PMOS transistor, those should be used in the circuit. If channel length variation needs to be detected, short-channel transistors should be used as well. In addition, depending on the application the circuit will be used in, detection of more than one parameter may be needed (e.g. threshold voltage of PMOS and NMOS transistors, channel length simultaneously).

IV. Results

The proposed PCMC has been designed using standard 28 nm CMOS technology. Functional verifications are done via simulator Finesim (Synopsys Inc.). The layout implementation is done using Custom Designer (Synopsys Inc.). For complete verification of the circuit's performance both regular/skewed and Monte-Carlo corners have been used during simulation. The circuit's functionality has also been verified for different values of threshold voltage of NMOS transistor. The temperature is set to 25 ºC (constant).

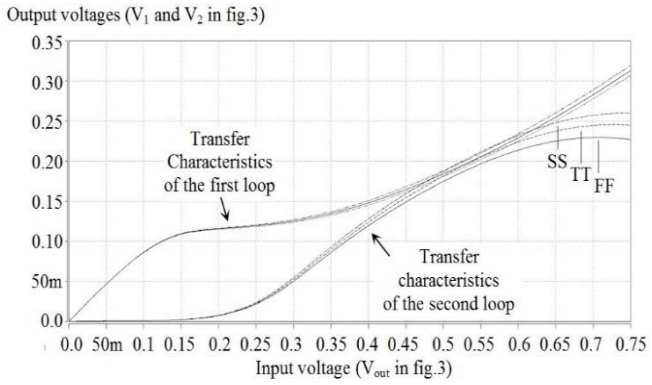

Fig. 7 Transfer characteristics of the first and the second loops (Fig. 4) corresponding to different process corners

Since the behavior of the proposed circuit is determined by the transfer characteristics of both loops (first and second loops in Fig. 4), they have been obtained separately for different process corners (Fig. 7) and threshold voltage values (Fig. 8). Plots show that in both cases that the transfer characteristics have stable zero and non-zero operating points. Also, process corner or threshold voltage change leads to crossing/operating point change (i.e. their "detection" is possible). Note the similarity between the curves of Figs. 4 and 6, which means that (1)-(3) describe the characteristics quiet well.

To directly check detection/monitoring capability, the output signal (versus threshold voltage shift) has been plotted (Fig. 9). The figure shows that starting from some values of threshold voltage shift the V_{out} drops to 0. Corresponding "transition" value, referred to as the switching point, is marked by dot A. There is one key point here to discuss. It is related to V_{out} drop. The key point is that the V_{out} derivative (with respect to threshold voltage) is indefinite at the switching point. Only in this case can it be used as the digital signal for other blocks.

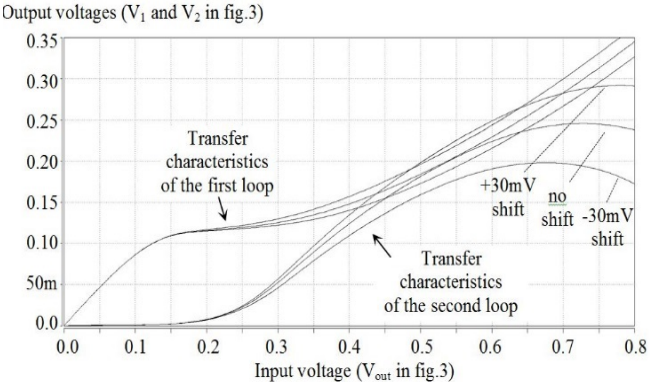

Fig. 8 Transfer characteristics of the first and the second (Fig. 4) loops corresponding to different values of the threshold voltage shift

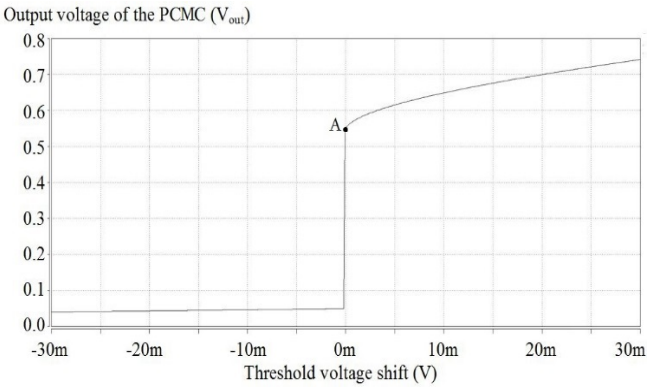

Fig. 9 Dependence of the output voltage (V_{out}) on threshold voltage shift

Since the purpose of the proposed PCMC is to monitor the process corner, i.e. die-to-die variations [3], [4], its function has been checked across different corners. In reality, however, there are also within-die variations [3], which impact the circuits' behavior. To verify the robustness of the proposed circuit in the presence of within-die variations, Monte-Carlo simulations have been run (1000 corners), which includes both process corner (slow, typical and fast) and local mismatch of all transistors. The results are given in Fig. 10.

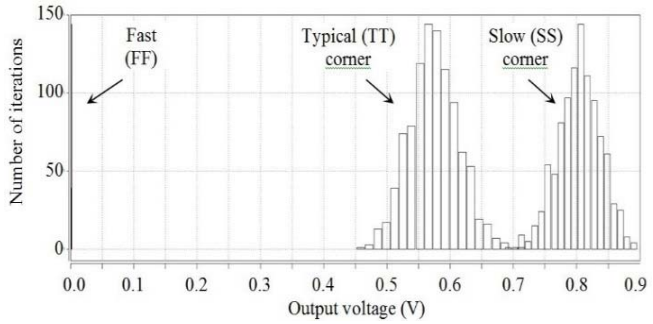

Fig. 10 Dependence of V_{out} on number of Monte-Carlo iterations

Results show that even in a presence of within-die variations the circuit can monitor process corners. Note that the output voltage is high (logic "1") in both typical and slow corners, i.e. the circuit does not detect those corners. On the other hand, it is 0 in fast corner. Thus, high voltage at the output will denote slow or typical, and low voltage at the output will denote fast corner. The key feature of the proposed circuit is its ability to detect at least one corner; and in the case of more corners, it should be modified slightly. If it is necessary to have higher accuracy, e.g. divide the range between fast and slow corners on more "sub ranges", more output signals will be needed. Particularly, to exactly detect the mentioned three corners, it is possible to add another loop similar to the first loop (Fig. 4) with different transfer characteristics. With that loop being active, the output voltage will be low in fast and typical corners, while high in only slow corner. Thus, we will be able to exactly determine the process corner by measuring the output voltage by activating those loops sequentially.

To ensure that the OA is stable as well, the AC characteristic for slow, typical and fast corners are obtained (Fig. 11). The plots show, that the worst DC gain of the OA is ~69 db, the phase margin ~68 deg. Thus, the OA has sufficient gain and stability margin.

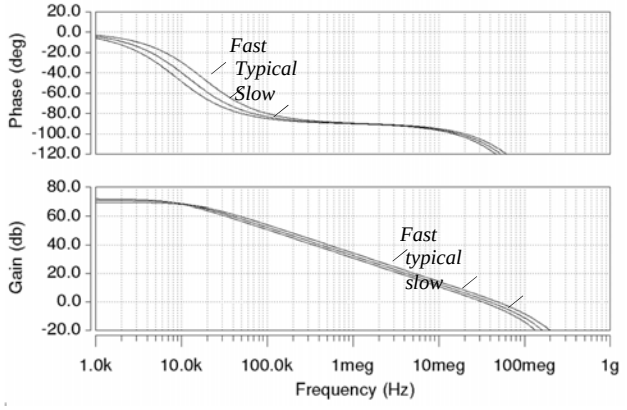

Fig. 11 AC characteristics of the OA (Fig. 6)

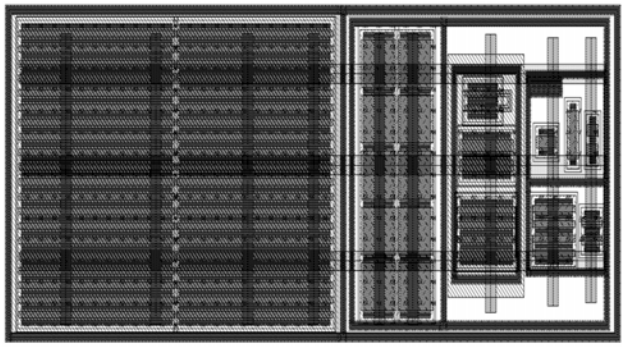

Fig. 12 Layout of the proposed PCMC

Fig. 12 shows layout of the proposed PCMC implemented in standard 28 nm CMOS technology. The main requirement for proper layout is matching of corresponding transistors. Particularly, transistors in first and second loops (Fig. 4) should be matched as much as possible. Differential pair and mirror transistors (Fig. 6) should be matched as well. The matching is critical for the circuit, since it will lead to a smaller impact of within-die variations on circuit functionality.

The area of the proposed circuit is 330um^2, current consumption is 20 uA. Note that since the circuit operates in testing mode, it operates in a limited period of time. Once the IC is used in regular mode (after testing), the proposed PCDC is off and does not consume any current.

Post extraction simulation results confirm that the proposed circuit is fully functional and can detect process corner even in the presence of within-die variations.

V. Conclusion

A PCMC has been presented in the current work. The circuit monitors process corner by generating a digital signal (voltage), which can be used in digital and analog circuits. The key feature of the circuit is that it utilizes only MOS transistors, which allows achieving small area, current consumption and high detection accuracy. The circuit is easily implemented in CMOS technology, and can be further modified if monitoring of more parameters or corners is needed. Post extraction simulation results confirm that the circuit can detect process corner in the presence of within-die variations. Simplicity of its structure does not require additional functional pins or any additional testing operations when used on a chip. This leads to a reduction of testing time and cost of ICs.

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