eProcessor

D2.2

Dissemination and communication report

V1.0

Document information

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Author(s)	Yannis Papaefstathiou (EXA)
Contributors	All
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Version	Author(s)	Comments and Description of change
0.0	Yannis Papaefstathiou (EXA)	Initial ToC and assignment to partners
0.5	Yannis Papaefstathiou (EXA)	All Contributions in place
1.0	Yannis Papaefstathiou (EXA)	Final version integrated and reviewed by EXTOLL

EuroHPC Joint Undertaking

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Executive Summary

The goal of the deliverable is to report the dissemination and, communication activities within the 1st period of the project. All project partners contributed to this deliverable.

Following the plan established in D2.1 eProcessor's dissemination strategy "make sure that all research carried out will reach all the key target groups in the HPC community and beyond". Within the covered period, the project used different dissemination channels and activities to make sure that all the targeted decision makers and stakeholders have access to all eProcessor developed dissemination and communication material, such as:

- A web page and social media for general dissemination and repository
- Participation in meetings/workshops/conferences relevant to the HPC community
- Publication of scientific papers
- Organization of a workshop as well as joint activities (i.e. collaboration workshop) with related HPC projects

Contents

1 Introduction

This document describes the Dissemination and Communication Activities that were carried in the 1st period of the project (M1 – M18).

The initial main aims of the deliverable are:

- to keep a record of all communication and dissemination events/actions carried out by all the partners in the framework of the project.
- to demonstrate the effectiveness of the promotion of the project results through web and social media, publications (conferences and journals), organization of workshops, summer schools etc.
- To highlight the dissemination material produced and used in this period.
- to demonstrate the contributions to specific HPC activities/events.
- to set a plan for the events and the actions that should be carried out in the 2nd period of the project so as to be able to meet the project KPIs.
- to ensure that information is shared with appropriate audiences on a timely basis and by the most effective means.

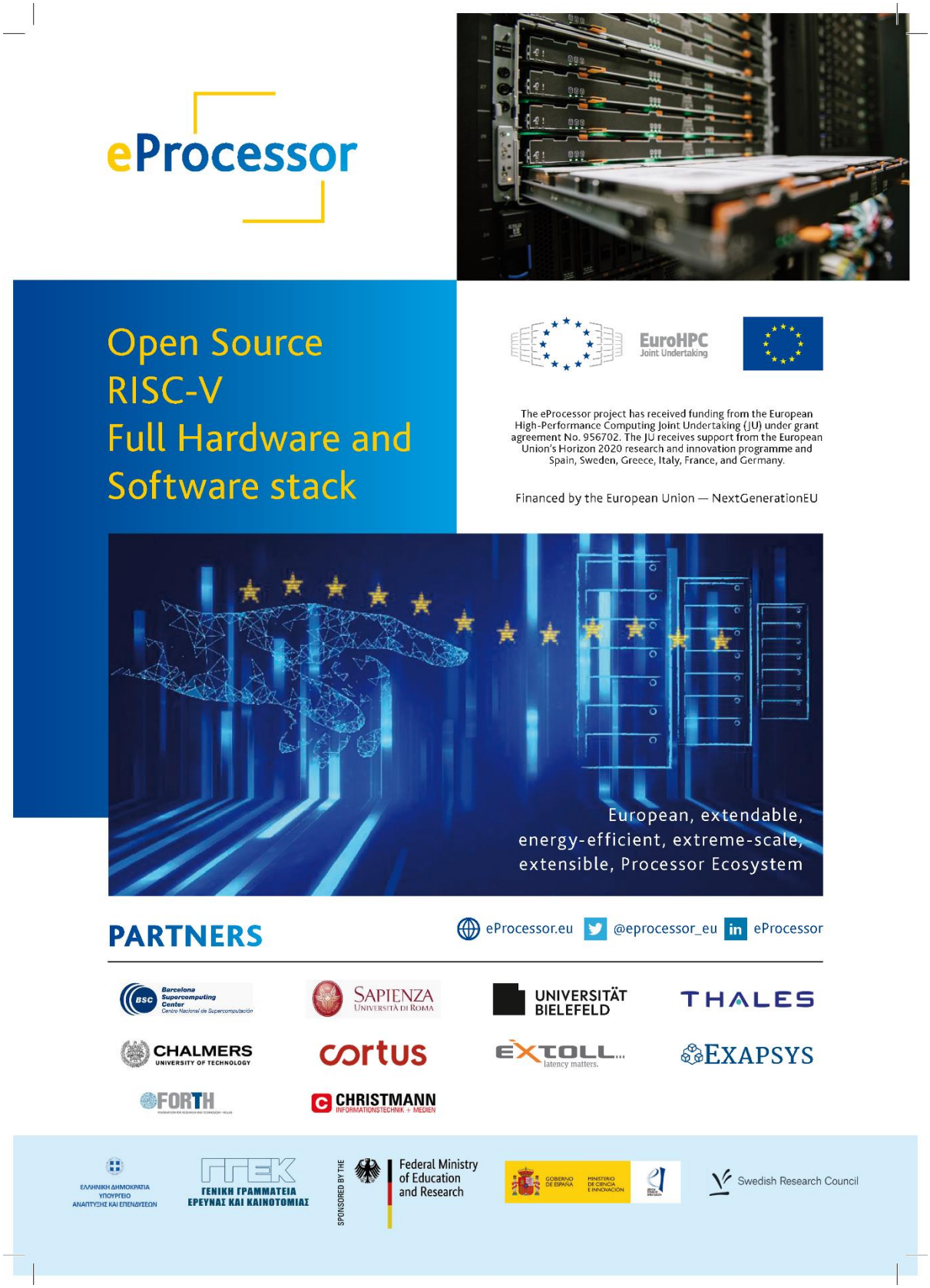
It should be noticed that EXAPSYS, that is in charge of the dissemination and communication activities of the whole project, signed the funding contract with the Greek Funding Authority in July 2022; until then it was not clear how/whether the dissemination costs listed in the Grant Agreement would be charged so as to be eligible for national funding as well. After the signing of the national contract, it has been clear that there should be a contract amendment (i.e. moving the dissemination costs to subcontracting costs) so as to be able to hire the external body who will be responsible for the production of communication and dissemination material, the organization of corresponding events, etc. Based on this fact it is expected that such a company will be hired in early December 2022.

2 Overall Dissemination and Communication Report

2.1 New Dissemination material

Within the 1st period of the project we have designed and used a poster, a flyer and a slide deck which have been used in the workshops, conferences and fairs we have presented eProcessor. Below is the current version of the poster :

In the next figures we have the initial version of the A4 flyer (2 pages) we developed which is currently used in the different dissemination events:



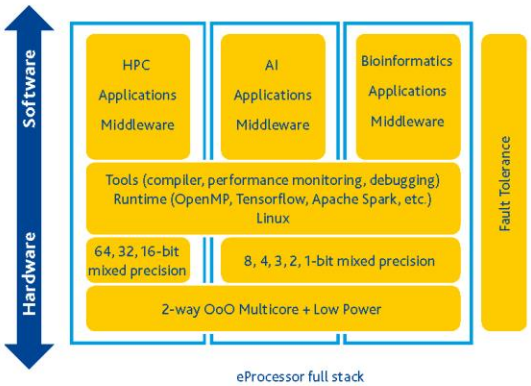
OBJECTIVES

- The **eProcessor project** aims to build a new open source Out of Order (OoO) processor and deliver the first open source European full-stack ecosystem based on this new RISC-V CPU.
- **eProcessor technology** will be extendable (open source), energy efficient (low power), extreme-scale (high performance), suitable for uses in HPC and embedded applications, and extensible (easy to add on-chip and/or off-chip components).
- The project is **an ambitious combination** of processor design, based on the RISC-V open source hardware ISA, applications and system software extending pre-existing Intellectual Property (IP), combined with new IP that can be used as building blocks for future HPC systems, both for traditional and emerging application domains.

Thus eProcessor aims at :

1. Expanding European capabilities around the development of an actual IC chip.
2. Improving and extending the open system software stack for RISC-V, providing new software to run on this novel hardware.
3. Demonstrate, validate and benchmark using applications from the area of Smarthome and Surveillance.

APPROACH



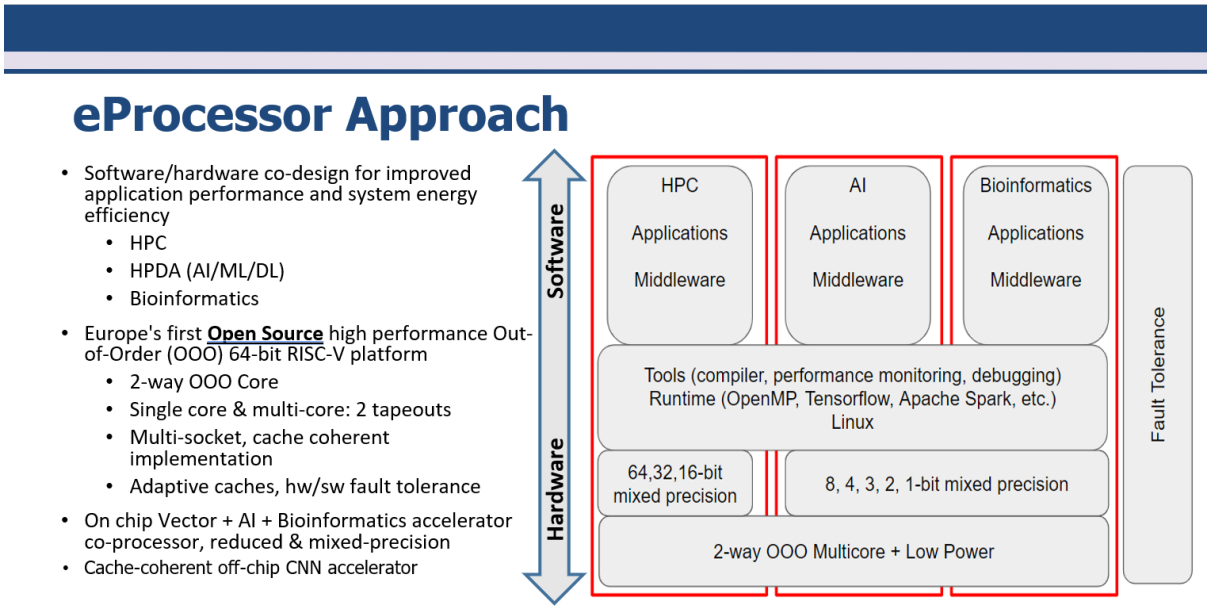
eProcessor full stack

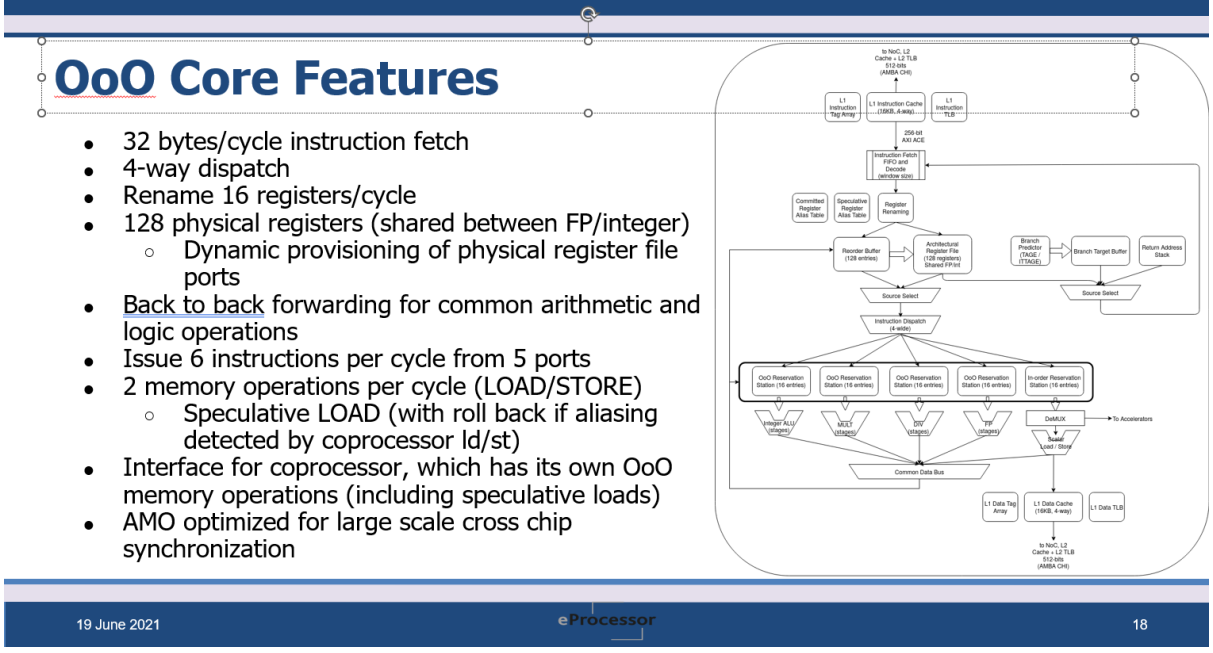
- Software/hardware co-design for improved application performance and system energy efficiency
  - HPC
  - HPDA (AI/ML/DL)
  - Bioinformatics
- Europe's first Open Source high performance Out-of-Order (OoO) 64-bit RISC-V platform
  - 2-way OoO Core
  - Single core & multi-core: 2 tapeouts
  - Multi-socket, cache coherent implementation
  - Adaptive caches
- On chip Vector + AI accelerator
  - New Bioinformatics accelerator co-processor
- Coherent off-chip accelerator: CNN

AMBITION

- eProcessor goes beyond the traditional **HPC** usage domain, expands to **High Performance Data Analytics (HPDA) and Deep Learning and AI workloads**, and mixed-precision processing technologies for genomic processing in the Bioinformatics domain.
- Explore new areas in reduced precision, sparsity, and software/hardware co-design.
- Allow the OpenMP runtime and compiler to guide cache coherence optimizations and to implement energy-efficient scheduling and synchronization; as well as to integrate Tensorflow and Apache Spark ML.
- Advance the state-of-the-art for the ML accelerators by developing arithmetic units to support simultaneously a wide range of **reduced and mixed precision** (1, 2, 4, 8-bit) as well as explore new formats (8- and 16-bit bfloat) for reduced precision floating-point for ML training;
- Improve application performance using cooperative **adaptive on-chip memories** (scratchpad for last-level cache)
- Devise a **Coherent CPU/Accelerator Interconnect and NoC**;
- Provide **Fault Tolerance** for critical processor structures such as L1 Data & Instruction caches, L2 cache, TLB, and register files with various error detection strengths (parity or lightweight ECC).

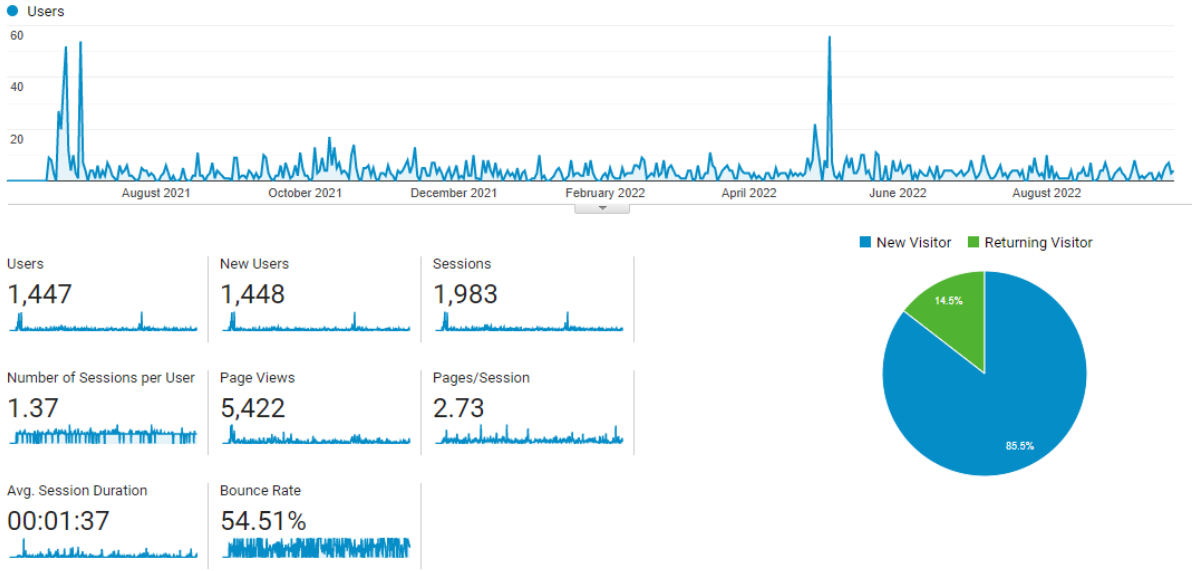
The next figures demonstrate some of the slides from the slide deck used for the presentation of eProcessor at the relevant events





2.2 Website

The Website has been up, fully populated and continuously updated since the beginning of June 2021. Based on Google Analytics, since then the eProcessor website has almost 1500 views (1447 as of 23rd September 2022). As shown in the following figure the traffic was higher when we launched the site and advertised it through our social media and when the project has been covered by press (e.g. after the presentation in HiPEAC computing week).



One important point is, that the largest percentage of the visitors come from the U.S.A. (16,68%) followed by visitors from the countries that participate in the project (e.g. Spain, Germany, Italy, Greece).

	Country	Users	Users
		1,447 % of Total: 100.00% (1,447)	1,447 % of Total: 100.00% (1,447)
1.	United States	246	16.68%
2.	Spain	173	11.73%
3.	Germany	129	8.75%
4.	France	113	7.66%
5.	Greece	103	6.98%
6.	Italy	80	5.42%
7.	China	61	4.14%
8.	Canada	60	4.07%
9.	Netherlands	60	4.07%
10.	Sweden	59	4.00%

2.3 Social Media

The innovation manager keeps monthly statistics of the social media accounts. Those statistics are stored in the project's restricted Sharing space.

2.3.1 Twitter

Twitter activity is monitored via the Twitter Analytics feature. Every month, we record:

- Total number of followers
- Number of tweets
- Number of impressions
- Number of engagements

In the following table you can see the recorded data for the five 3-month periods from June 2021, when the eprocessor twitter account was set up, to the end of August 2022.

Period	Followers	Tweets	Impressions	Engagements
06/21 – 08/21	27	3	1800	75
09/21 – 11/21	60	4	4500	180
12/21 – 02/22	63	0	326	11
03/22 – 05/22	77	3	3000	110
06/22 – 08/22	85	2	1400	89

As expected the impression, engagements and followers depend heavily on the number of tweets; it is expected that within the 2nd period of the project we will have more activity in our twitter account mainly due to the following two reasons :

1) We will have the first tangible results to demonstrate to the community
2) Now that the pandemic era seems to be behind us, eProcessor will participate in more events including fairs, workshops, conferences, exhibitions etc.

2.3.2 LinkedIn

LinkedIn's activity is monitored via the LinkedIn Analytics feature. Each calendar month, we record:

- Total number of followers
- Number of posts
- Number of visitors
- Number of page views
- Number of clicks
- Number of impressions

In the following table you can see the recorded data from Linkedin for the four 3-month periods from June 2021 when the eprocessor twitter account was set up to the end of August 2022.

Period	Followers	Posts	Visitors (unique)	Page Views	Clicks	Impressions
06/21 – 08/21	55	3	132	44	4	411
09/21 – 11/21	63	2	14	34	1	31
12/21 – 02/22	65	0	8	16	2	31
03/22 – 05/22	73	2	84	24	6	238

06/22 – 08/22	77	2	54	26	56	786

Just as with the twitter data, the involvement of the end users heavily depends on the number of posts; it is expected that within the 2nd period of the project we will have more activity in our linkedin account mainly due to the reasons listed in the last sub-section.

2.4 Presentations, Publications, Organization and Participation in events

Currently, the innovation manager (and still also dissemination leader) keeps a shared spreadsheets with all the presentation and publication activities which are also listed in the website. Below the details of all the publications of eProcessor that were accepted during the 1st period of the project

M. P. Bacardit, L. Bautista-Gomez and O. Unsal, "FPGA Checkpointing for Scientific Computing," *2021 IEEE 27th International Symposium on On-Line Testing and Robust System Design (IOLTS)*, 2021, pp. 1-7, doi: 10.1109/IOLTS52814.2021.9486693.
Jing Chen, Madhavan Manivannan, Mustafa Abduljabbar, and Miquel Pericàs, "ERASE: Energy Efficient Task Mapping and Resource Management for Work Stealing Runtimes." ACM Trans. Archit. Code Optim. (TACO) 19, 2, Article 27 (June 2022)
Jing Chen, Madhavan Manivannan, Bhavishya Goel, Mustafa Abduljabbar, and Miquel Pericas, "STEER: Asymmetry-aware Energy Efficient Task Scheduler for Cluster-based Multicore Architectures", IEEE 34th International Symposium on Computer Architecture and High Performance Computing (SBAC-PAD 2022).
A. Ejaz and I. Sourdis, "FastTrackNoC: A NoC with FastTrack Router Datapaths," *2022 IEEE International Symposium on High-Performance Computer Architecture (HPCA)*, 2022, pp. 971-985, doi: 10.1109/HPCA53966.2022.00075.
Miquel Moreto Santiago Marco-Sola, “Accelerating the Wavefront Alignment Algorithm on CPUs, GPUs and FPGAs”, *4th HPC Workshop on Accelerator Architecture in Computational Biology and Bioinformatics (AACBB),* 18th June 2022, New York City, USA
Mateo Vazquez Maceiras, Muhammad Waqar Azhar, Pedro Trancoso, “VSA: A Hybrid Vector-Systolic Architecture”, *40th IEEE International Conference on Computer Design (ICCD)* · October 23 - 26, 2022 · Lake Tahoe, USA (to appear)

Moreover, the overall project and/or certain subcomponents of our approach were presented in events listed in the following table. More details about those events can be found in the dissemination actions of the individual partners as listed in Section 3, while the most important of them were also announced and/or reported in the news/event part of eProcessor website together with photos and/or videos.

eProcessor workshop, HiPEAC Computing System Week 2022, 28th of April 2022, Tampere, Finland
Organization of special session on European Acceleration Technologies in ASAP 2022, 13th July 2022, Gothenburg, Sweden
2021 RISC-V Int'l ISC virtual booth, 24th June – 2nd July 2021
2nd workshop on RISC-V and OpenPOWER in HPC at the ICS International Conference on Supercomputing 2021, 10th June 2021
Presentation in special session "MARIA: Memory Access for RISC-V Vector Architectures" at the "ASAP 2022" conference, 13th July, Gothenburg, Sweden
Participation in "Vector Processing Unit Workshop", 20th of April 2022
Presentation of the eProcessor architecture and application in Edge Exascale using RISC-V, DL4IoT: Workshop on Deep Learning for IoT at HiPEAC '22 Conference, 20th June 2022, Budapest Hungary

The most important events are a) the special full-day workshop organized solely by eProcessor, as part of HiPEAC CSW, in Tampere in April 2022, and b) the special session for eProcessor organized in ASAP 2022 ; in both of them the overall architecture as well as several innovative features of eProcessor's subcomponents were presented.

Three partners of eProcessor also participated in the EuroHPC collaboration event organized in Madrid from 19th - 20th September 2022 which focused on identifying and presenting collaboration actions between the EuroHPC projects. eProcessor seems to have distinct collaboration opportunities with DEEP-SEA, READ-SEA and Textarossa projects. which will be investigated further.

Moreover, the project has also been presented in a number of events as part of more general presentations/lectures/interviews. In the following table we outline those presentations.

Interview at the "L'altra radio" radio programme on the 26th of May 2021
Lecture on "Scalable cache coherence solutions" including eProcessor activities in ACM summer school in computer Architecture
Talk titled "CHALMERS ACTIVITIES IN EUROHPC JU" including discussion of eProcessor activities, DATE 2021

eProcessor was presented at a University of Cyprus seminar, July 2022.
Educational laboratory activities in the academic programme of the Master Degree in Electronics Engineering (course “Digital Integrated System Architectures I”, held by M. Olivieri and F. Menichelli).
CHR employees were interviewed by a local newspaper about the eProcessor project, 3rd November 2021
eProcessor poster presented in the UNIBI “Smart Mirror” live demo and flyers distributed in 3 events (Embedded World 2022 in Nuernberg, Germany, the IoT Week 2022 taking place in Dublin, Ireland and the HiPEAC 2022 in Budapest, Hungary)
Smart mirror demonstrator/use-case and eProcessor flyers, HMI 2022 (30. May 2022 - 02. June 2022)
Parallel Programming’ course at Koç University, part of eProcessor-Sparcity EuroHPC collaboration plan, 8th November 2021
Hannover Messe 2022, 30th May – 2nd June 2022

2.5 KPIs

The following KPIs together with their targeted values, have been identified to keep track of the progress of the dissemination and communication activities of the project and analyzed in D2.1.

Below are the current values/evaluation results for all of them. All of them are progressing as scheduled. While some of the values may seem low, we have a specific plan for the 2nd period of the project where they are associated with the actual results of the project (i.e. hardware, software, methods) which will materialize in the 2nd period. In general the consortium strongly believes that all the KPIs will be met while we expect to go beyond several of them.

KPI	Target value	
Knowledge Transfer	• At least 15 scientific publications and articles (publications, peer-reviewed articles, papers, etc.) in conferences and events; • At least 4 Whitepapers (business and/or scientific) or General publications in journals or other peer-reviewed publications.	• 6 scientific papers have already been presented and/or accepted for publication in highly respectful conferences (one cannot still be added to the website since the conference is in November 2022) • A schedule has been agreed for the 4 whitepapers/general public publications which will be on the following topics : a) Overall architecture of eProcessor , b) Single core chip and associated SW, c) multi-core chip and associated SW, d) Final evaluation of eProcessor full HW and SW stack
Participation and Organization of Technical and Scientific Events, Conferences, Workshops, Hackathons, etc. (in collaboration or not)	• At least 10 participations in events, workshops and conferences; • 3 events/workshops organized through the project lifecycle; • Organize at least 2 launch events; • Organize at least 3 small face to face sessions or workshops; • Organize at least 2 webinars.	• eProcessor has already participated in 7 workshops and conferences • 2 events have already been organized as part of CSW 2022 and ASAP 2 while at least one other will be organized when the multi-core chips will be up and running • The launch events could not be organized due to Covid-19 and the restrictions when the project started. We plan to organize similar launch events as soon as the single-core and the multi-core devices are brought into live • 1 has been organized as part of the EuroHPC collaboration event workshop in Madrid (19-20 September 2021), two more are scheduled so as to discuss and present the results of the two chips (single and multi-core) that will be implemented • The plan is to have the webinars when we will have actual eProcessor HW and SW to work so as to mainly

		demonstrate how they can accelerate real-world HPC applications
Number of significant actions in Collaboration	• Contact and establish collaboration with at least 5 projects; • At least 25 direct contacts and speaking engagements with stakeholders.	• Collaboration with at least 5 projects has been started through, mainly, the EuroHPC collaboration events • Through the different events in which eProcessor partners presented our novel approach more than 20 stakeholders have been notified and shown initial interest in the eProcessor developments
Marketing Collateral Materials	• Target number for newsletters and/or blog posts: 1 every 6 months • Leaflets, flyers, brochures, posters, videos regularly updated.	• The target has been met since we have 3 blog posts in the first 18 months of the project and we will keep on this pace. • A Leaflet/flyer and a poster have been presented and used for the dissemination of the eProcessor results , while a video will be produced when eProcessor will have the 1st HW and SW up and running
Promotion	• At least 3 Press release campaigns; • At least 2 launch campaigns.	• 2 Press releases, in Spain, have been made, as well as one at a European Level. 2 more are planned when the eProcessor single and multi-core chips will executed their first basic benchmarks • As also stated above the launch campaigns could not be organized due to Covid-19 and the restrictions when the project started. We plan to organize similar launch events as soon as the single-core and the multi-core devices are brought into live
Online Channels	• Dynamic interaction on Social Media channels; • Dynamic production of landing pages and content on website; • Targeting 2000 visits per year to the website; • Targeting 1000 unique visitors to the website.	• This is accomplished as shown in Section 4.2 • The website is described in D2.1 and it is continuously updated • The targets have not been met yet but we strongly believe we will have more than 2000 visits per year and over 1000 unique visitors after we add the eprocessor open-source HW and SW in the site for download, as well as the 1st evaluation results

3 Individual Dissemination Report

3.1 BSC

During the first period of the project, BSC contributed to the Thematic Session at the HiPEAC Computing System Week 2022, which took place on 28th of April 2022 in Tampere, Finland. This thematic session was entitled "The eProcessor RISC-V HW/SW ecosystem". During the session, BSC contributed with an initial overview of the eProcessor project, describing its main objectives and organization. After introducing the project, the session continued with the technical contributions that are part of the different work packages. In this block, BSC contributed technical descriptions of the work that is being done in WP5, WP4 and WP3. In particular, in the context of WP5, BSC described the design of the eAccelerator and its features for executing vector instructions, as well as the hardware support for fault tolerance. In the context of WP4, BSC detailed the compiler support that is being implemented in LLVM to generate the vector instructions that are executed by the aforementioned accelerator, the performance monitoring tools (e.g., Perf, Extrae, Paraver) that are being developed to analyze the performance of the eProcessor architecture, and the application-level checkpointing library that is being developed as software support for fault tolerance. In the context of WP3, BSC presented the HPC, the Bioinformatics and the DeepHealth application use cases of interest for the project, as well as the microbenchmark suite that is used to drive design decisions in the early development stages of the eProcessor architecture. Finally, BSC withdrew the main conclusions of the session and responded to the questions of the audience.

BSC also contributed with a first news piece titled "eProcessor in a Nutshell : The Future is Here !" on the eProcessor Blogspot in August 2021. Here BSC presented the main ideas and objectives of the project, including a brief discussion on open-source hardware for HPC, the hardware/software co-design approach adopted in the project, the combination of industry standard methodology and cutting-edge research to accelerate exploitation, and the application use cases of interest. Then, the blog entry details the different areas of work of the project (from applications all the way down to chip physical design) and their corresponding leading institution and principal investigator.

BSC also contributed to the 2nd workshop on RISC-V and OpenPOWER in HPC that was held at the 2021 ICS International Conference on Supercomputing in Barcelona on 28th June 2021. As part of this workshop, BSC gave an on-line talk titled 'Contributing to the open RISC-V ISA through novel eProcessor hardware', which can be found on YouTube (https://www.youtube.com/watch?v=oVHzvf3-w5A&t=1496s&ab_channel=WorkshoponRISC-VandOpenPOWERinHPC, starting at minute 26). This talk was focused on the description of the eProcessor architecture, so it summarized the main work that is being done in WP5. In particular, the talk explains the characteristics of the out-of-order core, the eAccelerator, the off-chip CNN accelerator, the interconnection network, the last level cache, and the IOMMU.

Another dissemination activity carried out by BSC was an interview at the "L'altra radio" radio programme on the 26th of May 2021. The interview, which is in Spanish and Catalan, can be found online (https://www.rtve.es/alacarta/audios/laltra-radio/radio/5916339/, starting at minute 40). The nature of this interview was mostly addressed to the general public.In the interview we explained the objectives of the project, the benefits it provides to the society and its functionalities, and its relevance in the European roadmap for HPC.

BSC participated in a special session at the "ASAP 2022" conference. This conference took place in Gothenburg, Sweden on 12th-14th of July 2022 (online presentation on 13th of July) (https://www.asap2022.org/program/agenda). The special session was entitled "MARIA: Memory Access for RISC-V Vector Architectures". In this session, we presented the Vector Processing Unit's architecture, called "MARIA", which was designed for the eProcessor accelerator (eAccelerator).

At BSC, a "Vector Processing Unit Workshop" took place on 20th of April 2022. In this workshop we described the "MARIA Vector Architecture" (present in the eAccelerator) and the differences between the EPI's VPU architecture (Vitruvius Vector Architecture).

BSC has also created a project page on its website (https://www.bsc.es/research-and-development/projects/eprocessor-european-extendable-energy-efficient-energetic-embedded), has promoted this project writing dedicated news on its insitutional site (https://www.bsc.es/news/bsc-news/bsc-working-towards-the-first-completely-open-source-european-full-stack-ecosystem-based-new-risc-v) and has re-tweeted and shared any posts on the dedicated eProcessor Twitter and LinkedIn pages. Example to be seen here:

Source:
https://twitter.com/eprocessor_eu/status/1525900942259912704?s=20&t=uhFZ2fRv4TQ9OvkJNYZ6MA

3.2 CHAL

During the first period of the project, Chalmers disseminated eProcessor activities as follows:

- NoC techniques first introduced in eProcessor were published and presented in the paper by Ahsen Ejaz and Ioannis Sourdis, titled "FastTrackNoC: A NoC with FastTrack Router Datapaths" in 28th IEEE International Symposium on High-Performance Computer Architecture (HPCA-28), virtual event. https://ieeexplore.ieee.org/document/9773241
- Ioannis Sourdis and Nehir Sönmez organized and chaired a special session on European Acceleration Technologies in ASAP 2022: https://whova.com/embedded/session/lgczTA366WFuty%40wIrkmhEvisiIOucUs5RjjDH-hORk%3D/2479699/?widget=primary In that session eProcessor activities were presented. In particular:
    - Pedro Trancoso from Chalmers gave a presentation titled "On-Chip AI Acceleration in eProcessor", and

  - Abraham Josafat Ruiz Ramirez from BSC presented “MARIA: RISC-V Vector Processing Unit”
- In ACM summer school. Per Stenstrom gave a lecture on “Scalable cache coherence solutions” including eProcessor activities related to the HomeNode design. https://europe.acm.org/2022-hpc-summer-school
- At DATE 2021 University Fair event. Per Stenstrom gave a talk titled “CHALMERS ACTIVITIES IN EUROHPC JU” including discussing eProcessor activities. https://date22.date-conference.com/programme
- The work on resource management, which targets the minimization of energy consumed by task-based parallel applications on asymmetric multicores featuring externally controlled voltage-frequency settings, has been published in a paper accepted in the ACM Transactions on Architecture and Code Optimization: Jing Chen, Madhavan Manivannan, Mustafa Abduljabbar, and Miquel Pericàs. 2022. ERASE: Energy Efficient Task Mapping and Resource Management for Work Stealing Runtimes. ACM Trans. Archit. Code Optim. 19, 2, Article 27 (June 2022)
- The previous work was highlighted during an invited talk by Miquel Pericas at the MATEO 2022 workshop in Barcelona, Sept 1st, 2022. A recording of the talk can be found here: https://drive.google.com/file/d/1uqa3qgHOZza5UwuwKpEXhT1fbnwefIqW/view (jump to 16:13)
- A new paper extending this work to runtime-controlled DVFS in cluster-based asymmetric multicore platforms, has been recently accepted at the IEEE 34th International Symposium on Computer Architecture and High Performance Computing (SBAC-PAD 2022). The paper title is: "STEER: Asymmetry-aware Energy Efficient Task Scheduler for Cluster-based Multicore Architectures" and the authors are Jing Chen, Madhavan Manivannan, Bhavishya Goel, Mustafa Abduljabbar, and Miquel Pericas.
- At the HiPEAC ACACES 2022 summer school, July 10-16 2022, a work related to Chalmers contributions to the eAccelerator was submitted as an abstract and presented as a poster with title “VSA: A Hybrid Vector-Systolic Architecture”, Mateo Vazquez Maceiras, Muhammad Waqar Azhar, Pedro Trancoso
- Seminar at the University of Cyprus, July 2022 by Pedro Trancoso with title “Game of Domains: The accelerators are coming” where among other topics, the Chalmers contributions to the eAccelerator of eProcessor were presented.
- A paper describing the hardware developed by Chalmers for the acceleration of AI applications on the eAccelerator has been recently accepted for publication at the 40th IEEE International Conference on Computer Design (ICCD 2022), Lake Tahoe, USA, October 23-26 2022. The paper title is “VSA: A Hybrid Vector-Systolic Architecture" by Mateo Vazquez Maceiras, Muhammad Waqar Azhar, Pedro Trancoso.

A blog entry describing the fundamentals of cache coherence and an overview of the directory cache coherence solution developed by Chalmers in the eProcessor project was published on the eProcessor website on October 8, 2021. The blog entry can be read here: https://eprocessor.eu/eprocessor-caches-in-a-nutshell/

3.3 FORTH

During the first period of the project, FORTH contributed substantial technical content for the eProcessor Thematic Session at the HiPEAC Computing System Week in Tampere, Finland (28th April, 2022). Specifically, FORTH provided content for WP3 regarding microbenchmarks, slides for WP4 regarding the lightweight Linux OS kernel support for RISC-V, OpenAMP for asymmetric multiprocessing, and porting of the DynamoRIO dynamic instrumentation tool for RISC-V. In the context of WP5, the contributions concerned the design of the Shared L2 Cache, the dynamic Cache/Scratchpad memory, and the RISC-V IOMMU developed for the eProcessor project. Moreover, as WP Leader of WP6, FORTH prepared and edited the final slide deck, with contributions from the involved partners (BSC, EXAPSYS, CORTUS,

Chalmers, EXTOLL, Thales), to present the work on architectural simulations, the FPGA emulation infrastructure developed for the eProcessor project, the activity on FPGA emulation of the single-core eProcessor system, and the plans for the upcoming multi-core system emulation linked together with off-chip accelerators like the CNN FPGA accelerator.

FORTH also presented the eProcessor project at the "DL4IoT: Workshop on Deep Learning for IoT '' on June 20th, 2022 which was held with the HiPEAC '22 Conference in Budapest, Hungary. Manolis Marazakis gave a talk titled "European Open-Source RISC-V Processor Ecosystem (eProcessor)" which offered a full overview of the project and focused on the System Software aspects of the project (following Figure).

Moreover, FORTH contributed with a blog post titled: "The RISC-V IOMMU of eProcessor" for the eProcessor website in September 2022. The blog post introduces the benefits of IOMMUs and offers a first glimpse of the RISC-V IOMMU features developed for the eProcessor systems.

3.4 UNIRM

UNIRM's dissemination and communication activities regarded:

- Use of the developed RTL hardware units for educational laboratory activities in the academic programme of the Master Degree in Electronics Engineering (course "Digital Integrated System Architectures I", held by M. Olivieri and F. Menichelli). The attendance of the course is circa 50 people per year, of which 70% Italian and 30% foreign students.
- Preparation of a scientific article focussed on the design and evaluation of the small precision arithmetic units (8 bit Floating Point Unit and 4,2,1 bit Integer Unit) developed in eProcessor, to be submitted to a IEEE journal.

3.5 COR

Cortus has issued a press release regarding the development of the high-performance Out-of-Order (OoO) processor core which is at the heart of the European eProcessor project (https://www.cortus.com/2021/06/14/556/)

3.6 CHR

Christmann has been involved in the following dissemination activities related to eProcessor:

- In November 2021 some CHR employees were interviewed by a local newspaper about the eProcessor project. The article was printed and also released online on 3rd November 2021.

Mittwoch, 3. November 2021 Peiner Land

Ilseder Firma stellt Mini-Prozessor für EU-Supercomputer her

Vier Experten des Unternehmens Christmann Informationstechnik + Medien erstellen leistungsstarken Prozessor

Von Thomas Kröger

Sie arbeiten in Groß Ilsede an einem Mini-Prozessor für den neuen EU-Supercomputer (v. l.): Stefan Krupop, Gunnar-Billung-Meyer und Wolfgang Christmann. Foto: Thomas Kröger

Groß Ilsede. An einem spannenden europäischen Forschungsprojekt ist die Groß Ilseder Firma Christmann Informationstechnik + Medien beteiligt.

- In close cooperation with UNIBI Christmann was present with booths at three fairs and conferences taking place in parallel: The Embedded World 2022 in Nuernberg, Germany, the IoT Week 2022 taking place in Dublin, Ireland and the HiPEAC 2022 in Budapest, Hungary.
  All three booths had a poster detailing the eProcessor project and its goals and presented the UNIBI “Smart Mirror” as a live demo. This Smart Mirror is a future use case for the eProcessor microserver module once it becomes available. Also shown at all three booths was the “t.RECS” microserver platform that will be used as a carrier for the eProcessor microserver module and will also enable coupling two of these modules in a “dual socket” like configuration.

3.7 UNIBI

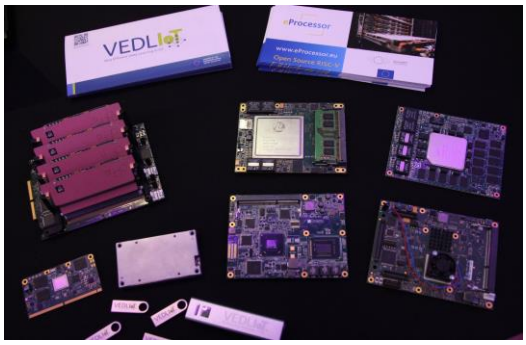
In the following, the dissemination activities of Bielefeld University are listed. As already stated before, most of the dissemination in the context of conferences or exhibitions happened jointly together with Christmann.

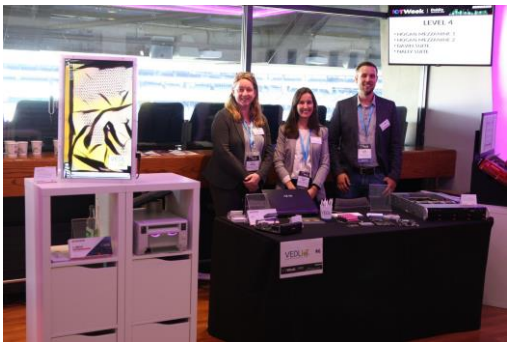
- HMI 2022 (30. May 2022 - 02. June 2022): With 2500 exhibitors and 75000 visitors, Hanover Fair (Hannover Messe) is one of the largest trade shows in the world. eProcessor has been presented to interested visitors on the booth showing the Smartmirror demonstrator/use-case and eProcessor flyers. The HMI event has been one of the first physical events with eProcessor flyers and demos.

- HiPEAC CSW 2022 (26. April 2022 - 28. April 2022): As part of the eProcessor session at the spring HiPEAC Computer systems week 2022 in Tampere, Finland, the hardware integration and smart mirror use case has been presented during a hybrid event, reaching up to 50 people locally and a remote audience of the same size. The session provided in-depth technical discussions of the complete eProcessor RISC-V HW/SW ecosystem.

- Embedded World 2022 (21. June 2022 - 23. June 2022): eProcessor and VEDLIoT shared a project booth during Embedded world. Project flyers, the project poster and a live demonstrator were presented to an audience of around 18.000 visitors. In addition, the t.RECS platform, which is used for eProcessor integration and evaluation, was also presented at the booth of congatec GmbH, a company specialized in providing computer on modules in the COM-HPC and COM Express form factor.

- IoT Week 2022 (20. June 2022 - 23. June 2022): During IoTWeek, eProcessor and VEDLIoT joint forces presenting both projects on a combined project booth. A live demonstrator and project flyers have been presented to approx. 8000 visitors.





- HiPEAC 2022 (20. June 2022 - 22. June 2022): During the HiPEAC conference, a major European forum for experts in computer architecture, programming models, compilers and operating systems for general-purpose, embedded and cyber-physical systems, eProcessor has been presented using a live demo, posters and flyers on a project booth and during the poster sessions. An expert audience of around 600 visitors has been reached.

In addition to this, an interview has been given to the HiPEAC magazine, explaining the goals of eProcessor and the importance of an RISC-V Open-Source ecosystem. eProcessor was also visible on the respective social media channels during and after the event.

- HiPEAC 2022 DL4IOT workshop (20. June 2022 - 22. June 2022): During the same event, an eProcessor presentation was part of the DL4IoT workshop at HiPEAC. Presented by FORTH, the architecture and application in Edge Exascale applications using RISC-V has been highlighted. The workshop had around 50 attendees.

- In addition to activities around conferences and exhibitions, the use of RISC-V in general and eProcessor in particular is also promoted in new computer on module standards. The eProcessor microserver itself is realized as a COM-HPC module, adopting a new computer on module form factor. As active members of the respective PICMG workgroup, RISC-V specific aspects are being integrated in new releases of COM Express or COM-HPC, creating true heterogeneous compute platforms.

3.8 EXTOLL

During the first period of the project, EXTOLL sent contributions to the eProcessor thematic Session at the HiPEAC Computing System Week in Tampere, Finland (28th April, 2022). EXTOLL contributed to the WP5 slides with an overview of the chip-to-chip link IP used in the eProcessor project.

3.9 THALES

During the first period of the project, Thales sent contributions to the eProcessor thematic Session at the HiPEAC Computing System Week in Tampere, Finland (28th April, 2022). This thematic session was entitled “The eProcessor RISC-V HW/SW ecosystem”. In particular, Thales contributed to WP3 slides with an introduction of the Surveillance Border Control use case involving drones for detecting boats along maritime borders. This presentation also

discussed the envisioned technical solution related to the energy efficiency problem of the use case: enabling a hybrid accelerated execution of the application on an heterogeneous system composed of the eProcessor chip linked to an FPGA loaded with an off-chip CNN accelerator from Thales. Both sub-systems will be connected in a memory-coherent way thanks to the various IPs of different partners from eProcessor (Extoll, FORTH and Chalmers). To enable efficient computation offloading, there is a need for software support. The envisioned software flow for porting and executing the surveillance application on the target heterogeneous system was introduced in the other contribution from Thales related to activities from WP4. In particular, the idea of partitioning the execution between hardware-accelerated neural network layers on the off-chip accelerator and specific software-implemented layers on the eProcessor chip was proposed and presented during the thematic session.

3.10 EXA

EXAPSYS is leading the communication and dissemination tasks. Thus, it is responsible for the website, the social media accounts, production of initial communication material etc. In terms of EXA's participation to dissemination events, the company decided not to participate to any of them because the research results produced by the company (i.e. the output of the simulations) were not ready before the end of June 2022; since then the company has prepared a short paper (in collaboration obviously with the designers of the processing core) which will be submitted to a relevant conference/workshop soon.

As also mentioned in the introduction, the dissemination actions of EXA, in general, were severally hindered by the fact that the contract with the Greek Funding Authority was signed in July 2022 and until the company could not hire the specialized company requested for the production of professional communication and dissemination material and/or the organization of dissemination events.

4 Conclusions

In this deliverable we first described the common dissemination and communication actions for the 1st period of eProcessor including the statistics of our website and our social media account, the eProcessor publications and the participation in the different events. Moreover, the dissemination and communication KPIs were listed and their current status highlighted as well as the plans for meeting them within the duration of the project. Then each partner analytically presents the dissemination actions overtaken within the 1st period of the project.