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Analysis and Design of Simultaneous Dual Band Harvesting System with Enhanced Efficiency

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Abstract**—**This paper presents an enhanced efficiency simultaneous dual band energy harvesting system for wireless body area network. A bulk biasing is used to enhance the efficiency of the adapted rectifier design to reduce V_{th} of MOSFET. The presented circuit harvests the radio frequency (RF) energy from two frequency bands: 1 GHz and 2.4 GHz. It is designed with TSMC 65-nm CMOS technology and high quality factor dual matching network to boost the input voltage. Full circuit analysis and modeling is demonstrated. The simulation results demonstrate a harvester with an efficiency of 23% at 1 GHz and 46% at 2.4 GHz at an input power as low as -30 dBm.

Keywords**—**Energy harvester, simultaneous, dual band, CMOS, differential rectifier, voltage boosting, TSMC 65nm.

I. Introduction

In a body sensor network, it is crucial that the sensor has unlimited lifetime and that its footprint remains small enough to be comfortably used on or inside the human body. Usually, sensor nodes use a battery as a power supply. However, this limits the life time of the node. Alternatively, energy harvesting using ambient RF energy can provide an unlimited source of power. RF energy is available from different communication services such as TVs, cell phones and radios and is distributed over a frequency range between 900 MHz and 2.4 GHz. However, this energy is limited due to the free space attenuation as well as other losses in the wireless channel such as multipath, fading, reflection and absorption. The free space loss is a function of the distance between the source of the RF signal and the device as given by the Friis equation [1]. These losses reduce the amount of the received power which is already limited by the Federal Communications Commission (FCC) regulations [2].

In order to take full advantage of the available wide range of RF power, a multi-frequency energy harvester is a feasible solution to extend the bandwidth and to provide multiple power supplies. In many applications, multiple voltage sources are required. For instance, a supply voltage of 1 V is needed for an analog block in RFID circuits or sensor nodes. While, a 0.4V or less is enough for digital blocks. Usually, a DC-DC converter is used to solve this problem in single converter applications, however, this solution might compromise the efficiency. Furthermore, it's possible nowadays to design a dual or multi band RF rectifier using single antenna thanks to the different architectures has been proposed for the dual band antenna [3]-[6]. These structures opened the door for area efficient simultaneous multi band RF harvesting without the need to multiple antennas.

Recently several work has been proposed for the dual RF band harvesting system, however, the simultaneous scavenging efficiency needed to be further improved. For instance, in [7], a simultaneous dual band energy harvester is presented. The design uses a "pre-set biasing network" to reduce the threshold voltage. It uses an array of large off-chip resistors and capacitors that limit the efficiency to 9.1% at 900MHz and 8.9% at 2GHz. In [8], a slightly improved efficiency was achieved for dual band rectifier. However, this enhancement related to the use of Schottky diodes as they have lower turn on voltage. However, these diodes are not preferred with CMOS fabrications as they require extra processing steps. In [9], a dual band RF rectifier is implemented using variable capacitance to resonate at two different frequencies and switch between them based on the amount of the input power. Although this work presents a high efficiency rectifier, it didn't harvest from dual RF bands simultaneously and didn't generate a multiple voltage sources. Actually only a single source at each allocated frequency was presented.

In this research, our target is to maximize the simultaneous power transfer in dual frequency bands. For this purpose, this work demonstrates an enhanced efficiency dual band energy harvester.

The paper is organized as follows. In Section II, the boosting network is discussed. Section III analyze the dual impedances and the principle of operation. In Section IV, an enhanced differential rectifier is presented. The simulation results for a new dual frequency energy harvester are discussed in Section V. The conclusion is drawn in Section VI.

II. The Matching Network

The impedance matching network between the antenna and the rectifiers play important rule in power transfer. To achieve maximum power transfer, a matching network ensures that the harvester impedance matches the antenna impedance. Also, the matching network can be used to improve the rectifier sensitivity by boosting the input power to a higher level. Fig. 1 represents the equivalent circuit of the energy harvester circuit where the energy converter is modeled with a parallel capacitor and resistor. By using a parallel to series transformation and using Kirchhoff's Law (KVL), we can

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obtain the boosting voltage (V_{boost}). (1) determines the capacitor voltage which is equivalent to V_{boost}. Knowing that $Q_C = \frac{1}{\omega\, C\, R}$. It's clear that, by increasing Q, the boosted voltage amplitude will also be increased. In other words, the matching network can be used to optimize power transfer and voltage boosting therefore we used a high Q matching network in this design.

Table I represents the L-matching network specifications for 1GHz and 2.4GHz in terms of area. As can be seen, although, dual inductors are used, the size of the harvester is still very compact. Actually, choosing the frequency was selected based on the available ambient bands and with minimum area.

$$V_c = V_{boost} = I \times Z = \frac{V_{in}}{R} \times \frac{1}{\omega\, C} \quad (1)$$

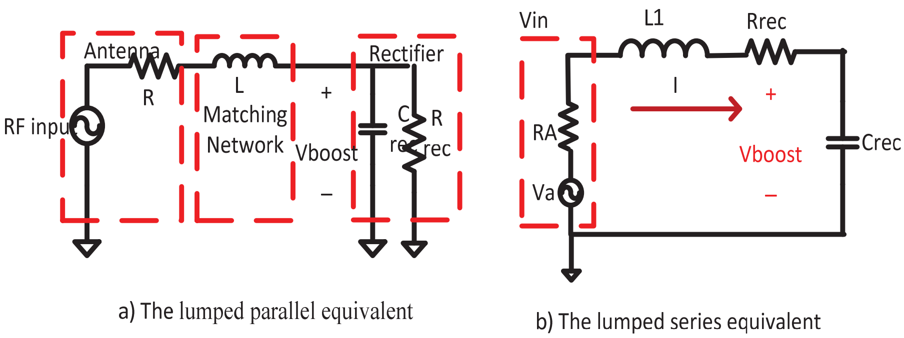

Fig. 1 Modelling of the boosting network in RF-DC system

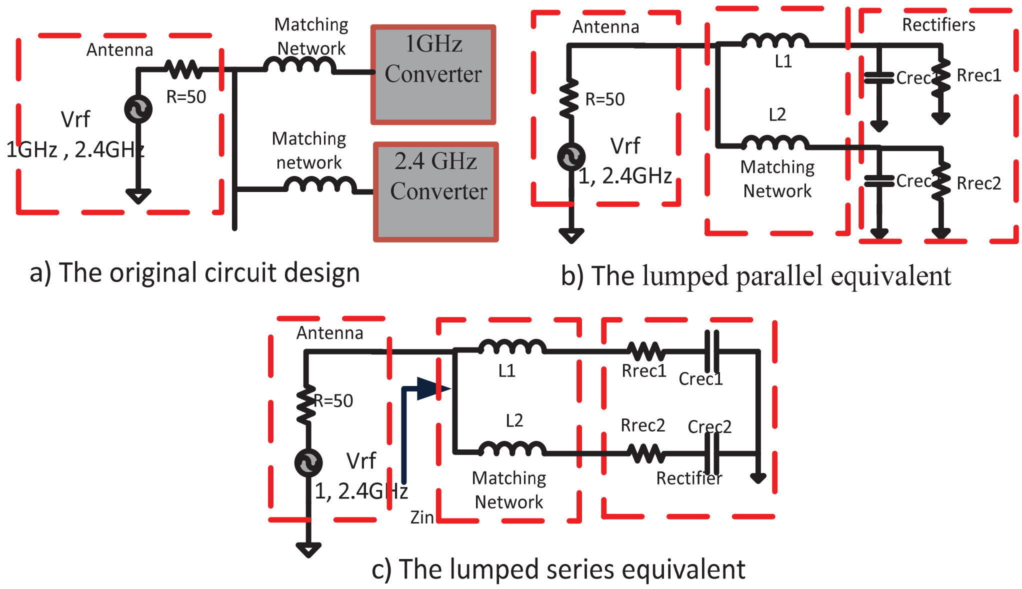

Fig. 2 Modelling the impedance of the dual frequency harvester

TABLE I
L-MATCHING NETWORK SPECIFICATIONS

	L (nH)	Q	turns	Width (µm)	Length (µm)
Rec 1	8.1nH	13	5	364.99	357.495
Rec 2	1.289	18	2	306	295

III. DUAL BAND MATCHING NETWORK ANALYSIS

Fig. 2 (a) represents the simultaneous dual band RF-DC harvesting system. This work is using a multi band single antenna that resonates at two targeted frequencies ω_1 and ω_2 as shown in Fig. 2 (b) where each converter is represented by a parallel resistor and capacitor. Each converter is designed to resonate at its specific frequency in a way that $\omega_2 = 2.4\, \omega_1$. At ω_1, the impedance for the first converter is purely resistive. It is equal to $Z_1(\omega_1) = R_1$ and matched to the antenna impedance. However, for the second converter which does not resonate at ω_1, the impedance is not purely resistive, and thus does not match to the antenna impedance. Similarly, at ω_2, the first converter does not resonate, the impedance is not resistive and does not match the antenna impedance, while for the second converter, and the impedance is purely resistive $Z_2(\omega_2) = R_2$. From Fig. 2 (c), the impedance of each converter at ω_1, ω_2 are expressed as:

$$Z_2(\omega_1) = R_2 - 2jQ_2R_2 \quad (2)$$

$$Z_1(\omega_2) = R_1 + 2j \quad (3)$$

In summary, our analysis shows that each converter input impedance Z_2 and Z_1 observed at the non-resonate frequencies (ω_1, ω_2) respectively is a function of the inductor Q-factor. Based on that and in order to maintain a high impedance at these frequencies, a large Q-factor is required.

IV. The RF-DC Converter Design

RF energy harvester is a key building block in many wireless applications like WBAN, WSN and RFID. It converts the AC signal to DC voltage. The classic Dickson multiplier [10] consists of a cascade of diode-connected MOS transistors. At each node of the diode chain, the RF signal is injected through a pair of coupling capacitors. Through charge sharing, the output voltage of each stage will be effectively multiplied with respect to that of its input. The dimension of the transistor (W/L), the number of stages (N) and the size of the coupling capacitor (C) are key design parameters. For example, increasing N increases the harvested DC voltage, constrained on the losses that result from the parasitic capacitance. The design requirements are the efficiency, the output DC voltage and the sensitivity required to turn on the CMOS rectifier.

The power conversion is defined as the ratio of the DC output power to the RF input power and it is an important parameter to measure the harvester efficiency. The Dickson multiplier suffers from a very poor power conversion efficiency (PCE) due to the losses associated with the Vth required to bias the MOS transistor. The DC output voltage in this type of CMOS converters [10] is defined by:

$$V_{DC} = 2.N(V_{in-} V_{th}) \tag{4}$$

The lower V_{th} the higher output voltage and hence better efficiency. Actually, as the gate voltage is increased, the MOSFET on-resistance is reduced as expressed in (5) and effectively, a better PCE can be achieved.

$$R_{on} = \frac{1}{\mu\, C_{ox}\left(\frac{W}{L}\right)(V_{gs}-V_{th})} \tag{5}$$

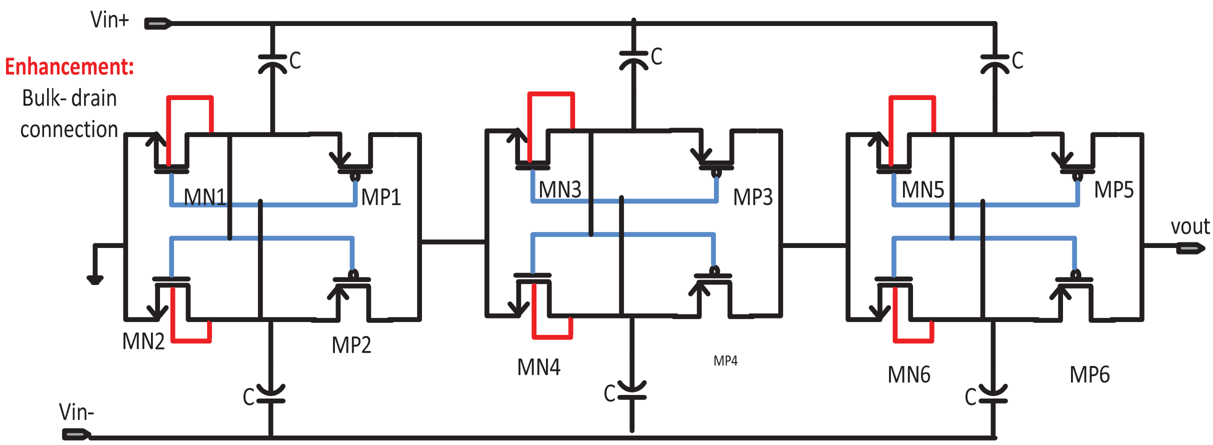

Fig. 3 The adopted differential rectifier [11] enhanced with dynamic bulk biasing

In this work, we adopted the V_{th} cancellation technique proposed in [11] to design two CMOS rectifiers working at 1GHz and 2.4GHz. Fig. 3 shows a three stages differential rectifier with bulk biasing. To enhance the efficiency and reduces the losses associated with turn on voltage, we dynamically biased the bulk by tying it to the drain terminal to utilize the relation in (6):

$$V_{TN} = V_{TN0} + \gamma\sqrt{|2\phi_f + V_{SB}| - \sqrt{2\phi_f}} \tag{6}$$

where, V_{TN} is the threshold voltage of NMOS, V_{TN0} is the zero bias threshold voltage with V_{SB}=0, γ is called the body factor. TSMC 65nm technology offers deep N-well layer and this can be used to isolate the bulk when it's forward biased. Fig. 4 represents the output voltage of the dual band system as a function of input voltage. This technique helped to increase the output voltage of the adopted design with a 25% at 1GHz and 2.4GHz respectively as shown in Fig. 5. The rectifier output was measured at one, two and three stages in Fig. 6 and as can be seen, a three stages is necessary to reach 1V supply, also, this technique helped to improve the sensitivity as well and dropped it to -30dBm.

V. The Dual Band Energy Harvester

The harvester is implemented with TSMC 65-nm technology and the simulations are carried out using Cadence / Spectre. The minimal input power is 36 mW which corresponds to 60 mVpk using a 50 Ω matching impedance, and the load impedance is 30 KΩ. The system performance was optimized to enhance the efficiency using extensive parametric analysis. It was found that for a minimum channel length L=150 nm, the optimum channel width W=450 μ m for NMOS and two times the width for PMOS transistor with Crec=7 pF. Fig. 7 represents the harvester power conversion efficiency curves at 1 GHz and 2.4 GHz. The efficiency was 23% at 1 GHz and 46% at 2.4 GHz respectively. Table II summarizes this work as compared to previously published work. As can be seen, this work provides better PCE at low input as 60mV for simultaneous harvesting while keeping the sensitivity low as – 30dBm.

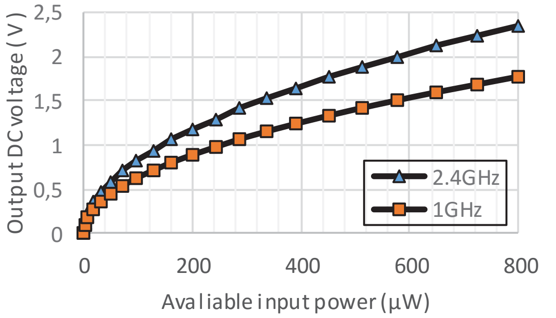

Fig. 4 The output voltage of the proposed dual band harvester system using bulk biasing technique

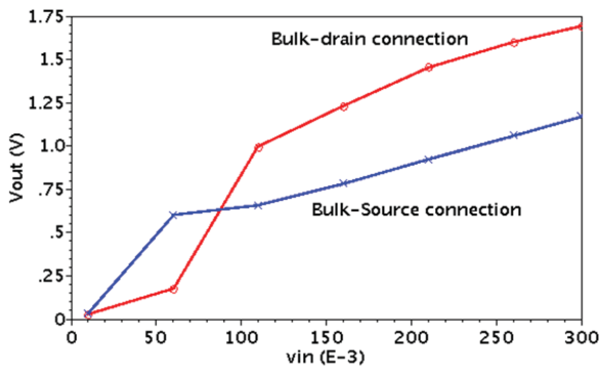

Fig. 5 A comparison between the output voltage when Vbulk=Vsource and when Vbulk=Vdrain

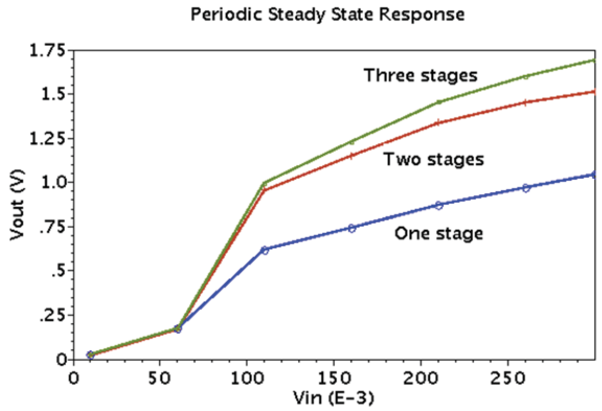

Fig. 6 The output voltage of the bulk biasing differential rectifier for different numbers of stages at 2.4GHz and R_L=30KΩ

TABLE II
PERFORMANCE COMPARISON

	This work	[9]	[7]	[8]
Min. input voltage	60mV	40mV	-19.3dBm 35mV	-10dBm -15dBm
Output voltage	1.3V@1GHz 1.1@2.4GHz	0.9V@0.95GHz 1V@2.4GHz	1V @0.9GHz 1V@1.9GHz	—
Load resistance	30KΩ, 30KΩ	50 KΩ	1.5MΩ 1 MΩ	—
No. of rectifiers	2	1	2	2
Efficiency PCE%	25% @ 1GHz* 42% @ 2.4GHz	55%@ 0.95GHz 64%@ 2.4GHz	11% @ 0.9GHz 14% @ 1.9GHz	39%** @575MHz 78%** @900MHz
Simulations dual freq.	1GHz 2.4GHz	Not simultaneous	900MHz 1.9GHz	500MHz 900MHz
CMOS Technology	65nm	0.13um	0.13um	Not in CMOS

*The P_{in} was calculated for 50Ω antenna impedance and measured at -14.3dBm input power.
** This PCE at 0 dBm.

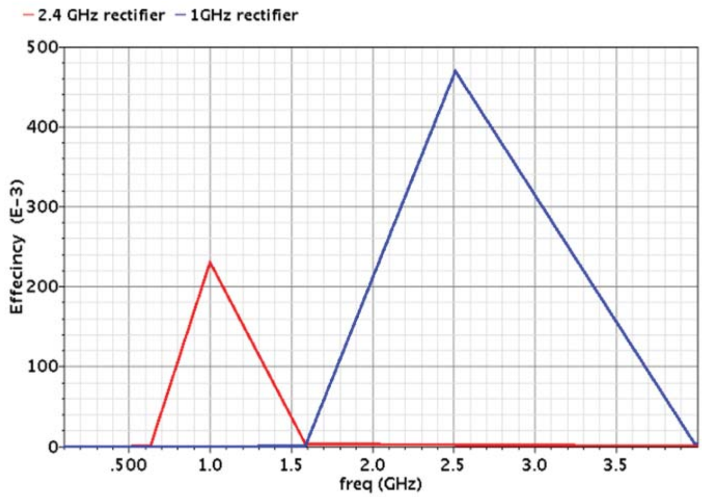

Fig. 7 The power conversion efficiency at $V_{IN=}$60mV, Ra=50Ω and R_L=30KΩ

VI. CONCLUSION

RF energy harvesting is a promising solution to replace or recharge a battery in the wireless body area network. In this paper, an analysis was conducted to find the rectifier voltage gain. A dual band harvester with insensitive Vth design was proposed with detailed analysis. The simulation results demonstrate a harvester with an output voltage equal to 1 V at 2.4 GHz and 0.75 V at 1 GHz respectively and at input power as low as 36 mW. The load impedance is 30 KΩ and PCE were 25% at 1 GHz and 42% at 2.4 GHz respectively.

REFERENCES

[1] E. P. J. Tozer. *Broadcast Engineer's Reference Book* 2004.
[2] Federal Communications Commission. *ISM Band Communication Equipment Regulation, FCC 15.247* (https://www.fcc.gov/Bureaus/Engineering_Technology/Documents/)
[3] Jie-Huang Huang, Jin-Wei Wu, Yi-Lin Chiou and C. F. Jou. A 24/60GHz dual-band millimeter-wave on-chip monopole antenna fabricated with a 0.13-μm CMOS technology. Presented at Antenna Technology, 2009. iWAT 2009. IEEE International Workshop On. 2009, DOI: 10.1109/IWAT.2009.4906869.
[4] Qi Luo, H. M. Salgado and J. R. Pereira. Compact printed monopole antenna array for dualband WLAN application. Presented at EUROCON - International Conference on Computer as a Tool (EUROCON), 2011 IEEE. 2011. DOI: 10.1109/EUROCON.2011.5929189.
[5] XuLin Quan, RongLin Li, YueHui Cui and M. M. Tentzeris. Analysis and design of a compact dual-band directional antenna. *Antennas and Wireless Propagation Letters, IEEE 11*pp. 547-550. 2012. DOI: 10.1109/LAWP.2012.2199458.
[6] F. Kanwal, H. Sultan, M. Maqsood, Q. ul Islam and S. Gao. Novel dual-band antenna with simultaneous linear and circular polarizations. Presented at Antennas and Propagation Conference (LAPC), 2014 Loughborough. 2014. DOI: 10.1109/LAPC.2014.6996436.
[7] L. Bo, S. Xi, N. Shahshahan, N. Goldsman, T. Salter and G. M. Metze, "An Antenna Co-Design Dual Band RF Energy Harvester," *Circuits and Systems I: Regular Papers, IEEE Transactions,* vol. 60, pp. 3256,3266, Dec. 2013.
[8] Y. Uzun and E. Kurt. Design and simulation of a new dual-band RF energy harvester with high efficiency. Presented at Consumer Electronics (ISCE), 2015 IEEE International Symposium On. 2015. DOI: 10.1109/ISCE.2015.7177837.
[9] P. Kamalinejad, K. Keikhosravy, R. Molavi, S. Mirabbasi and V. C. M. Leung. Efficiency enhancement techniques and a dual-band approach in RF rectifiers for wireless power harvesting. Presented at Circuits and Systems (ISCAS), 2014 IEEE International Symposium On. 2014. DOI: 10.1109/ISCAS.2014.6865568.
[10] J. F. Dickson, "On-chip high-voltage generation in NMOS integrated circuits using an improved voltage multiplier technique," *Solid-State Circuits, IEEE Journal of,* vol. 11, 1976.
[11] K. Koji, S. Atsushi and I. Takashi, "High-Efficiency Differential-Drive CMOS Rectifier for UHF RFIDs," *Solid-State Circuits, IEEE Journal,* vol. 44, pp. 3011-3018, Nov. 2009.

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