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AIDAinnova

Advancement and Innovation for Detectors at Accelerators

Horizon 2020 Research Infrastructures project AIDAINNOVA

MILESTONE REPORT

HIGH GRANULARITY PROTOTYPE FABRICATION 2

MILESTONE: MS19

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Abstract:

Within WP5 (Development of Monolithic Active Pixel Sensors) Milestone MS19 contains the fabrication of several high granularity devices.

This milestone has been successfully achieved and is reported.

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Executive summary

The fabrication of the first high granularity prototypes (MS20), was followed by intense characterization work (D5.1) to benchmark the performance of the devices. A second submission and fabrication cycle of various new prototypes followed to build on, or improve, the previous generation of devices. The new devices include the Mini-MALTA3 (Tower-Jazz 180 nm), the Main Demonstrator 3 (LFoundry 110nm) and Mini-CACTUS-V2 (LFoundry 150 nm). The fabrication is completed, and the prototypes have entered their characterization phases.

1. INTRODUCTION

Depleted Monolithic Active Pixel Detectors (DMAPS) are a key technology for the AIDAinnova project as they constitute, according to most detector experts, the most interesting new direction of pixel detector development and are therefore a key approach for pixel detectors at present and planned accelerator experiments.

Within WP5, the development follows two approaches, one focusing on high granularity devices, targeting above all small pixel dimensions, the other targeting foremost the radiation hardness of devices, especially for applications at hadron colliders as the LHC. This Milestone Report presents the second prototyping cycle in the development and production of DMAPS devices targeted at high granularity:

(1) Mini-MALTA3 DMAPS in 180 nm Tower-Jazz CMOS technology
(2) ARCADIA Main Demonstrator 3 prototypes in 110 nm CMOS technology
(3) Mini-CACTUS-V2 prototypes in 150 nm CMOS technology

This report concentrates on the milestones achieved with the second cycle of prototypes.

2. HIGH GRANULARITY DMAPS PROTOTYPE DEVELOPMENT

The development of Depleted Monolithic Active Pixel sensors has followed so far two generally different design approaches: (a) large electrode design and (b) small electrode design. While within AIDAinnova (a) is the prime approach for high radiation hardness, (b) targets primarily high granularity, i.e. small pixels, and low-noise and low-power operation, albeit with good radiation tolerance. Within (b) we also included devices with excellent time performance, though this development is occurring also in (a). The fabrication of the first high granularity prototypes (MS20), was followed by intense characterization work (D5.1) to benchmark the performance of the devices. A second submission and fabrication cycle of various new prototypes followed to build on or improve the previous generation of devices. The new devices include the Mini-MALTA3 (Tower-Jazz 180 nm), the Main Demonstrator 3 (LFoundry 110nm) and Mini-CACTUS-V2 (Lfoundry 150 nm). The development of designs in this second batch of high-granularity devices is the theme of this report.

2.1. MINI-MALTA 3 TOWER-JAZZ 180 NM TECHNOLOGY

Following the success of the MALTA2 large-size demonstrator DMAPS chip, a new iteration of the chip, the MALTA3, is planned to further improve the device. MALTA3 aims to exploit the full reticle

size (3x2 cm^2), add a 1.28 GHz local clock, and improve other remaining MALTA2 issues (IC2, reset and pulsing via fast command, Aurora encoding, etc.). Such an ambitious ASIC benefits from an intermediate step. The mini-MALTA3 implements the crucial improvements but on a small-size multi-project wafer device.

The Mini-MALTA3 is a 5x4 mm^2 demonstrator with a 48x64 matrix of 36.4 μm^2 pixel pitch that uses the same front-end as MALTA2. It is optimized for timing performance by using a synchronization memory with 0.78 ns time resolution. It features a fast clock generation with the STFC PLL from an 80 MHz clock input to 1.28 GHz at the output. It implements an I2C slow control and shift register protocols. It uses the LAPA pseudo-LVDS driver for receiver and transmitter operations. The reset and pulsing are implemented via a fast command input. The output data is scrambled using Aurora. Characterization is ongoing and will be reported in future reports.

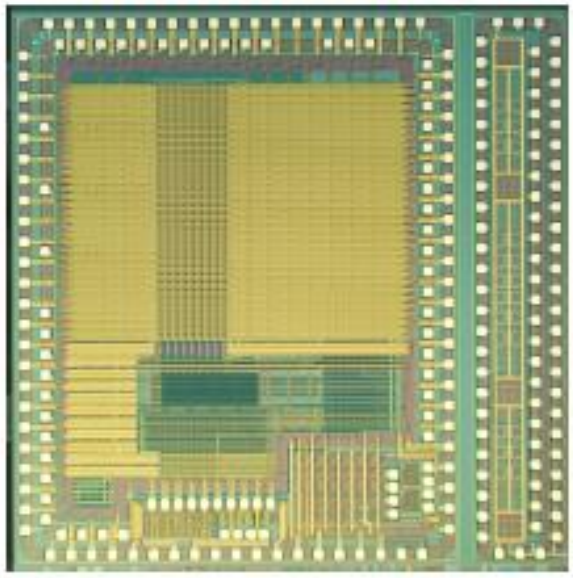

Fig 1. The mini-MALTA3 chip was submitted for fabrication in late 2023. The devices are currently being tested.

2.2. PROTOTYPE DEVELOPMENT IN LFOUNDRY 110 NM TECHNOLOGY (ARCADIA)

The ARCADIA (Advanced Readout CMOS Architectures with Depleted Integrated sensor Arrays) project aims to develop small electrode devices targeting high granularity and low power dissipation on thin substrates [2]. The first demonstrator (see the D5.1 report), was followed by an improved and more ambitious ASIC, the Main Demonstrator 3. The MD3 is a system-grade large size fully depleted MAPS (FDMAPS), with a 512x512 pixel matrix, pitch 25 µm, aiming to deliver low power (10 mW/cm^2) and high event rate capability. The fabrication run also includes a device with a small (4 x 16 mm^2) gain layer prototype (MADPIX). Initial testing of both prototypes indicate that the devices are operational.

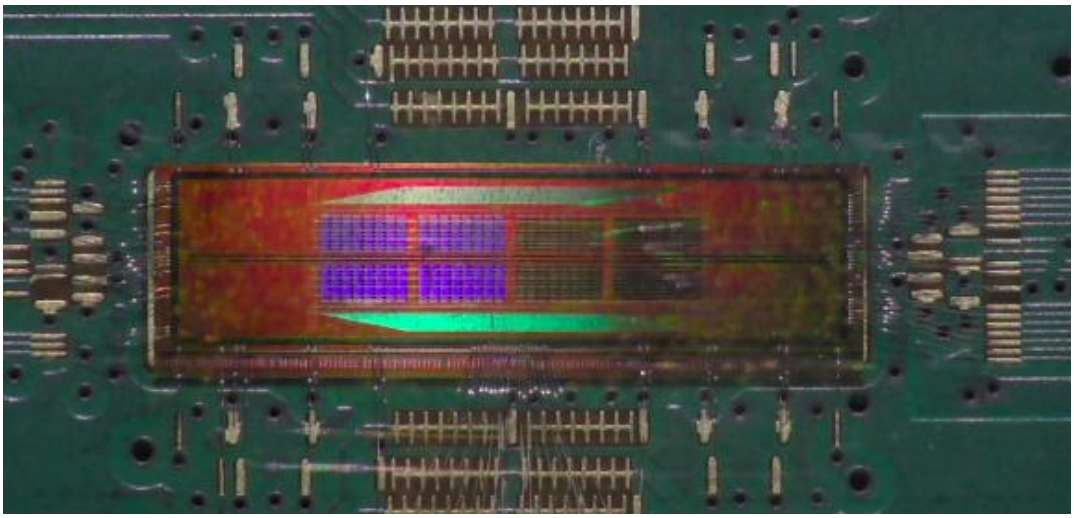

Fig. 2: Photograph of the ARCADIA MADPIX prototype mounted on a readout board.

2.3. PROTOTYPE DEVELOPMENT IN TOWER-JAZZ 65 NM TECHNOLOGY (TJ65)

Intense characterization work is still on-going in the 65 nm effort. The next submission is planned for the end of 2024. Encouraging results, including the first indications of the successful testing of stitched devices are included in the AIDAinnova P2 project report.

2.4. PROTOTYPE DEVELOPMENT IN LFOUNDRY 150 NM TECHNOLOGY (MINI-CACTUS-V2)

DMAPS exploiting both tracking and timing domains are an interesting option for future experiments. Within this work package an early prototype in the LFoundry 150 nm process called Mini-CACTUS has been fabricated to explore this possibility. A new prototype using the same technology, the Mini-CACTUS-V2, has been designed and fabricated with expected improvements in jitter and recovery time. The new device is about two times larger than the previous Mini-CACTUS devices, and it includes diodes with a size of 0.5 mm x 1 mm (baseline), 1 mm x 1 mm and 0.5 mm x 0.5 mm, and pixels of 50 µm x 150 µm and 250 µm x 50 µm. Different pre-amplifiers design were implemented, which in simulation improve the timing performance. Furthermore, the chip counts with a new multistage discriminator with programmable hysteresis and an improved layout for better mixed-signal coupling rejection [3]. The devices were recently received and will be evaluated in the next period.

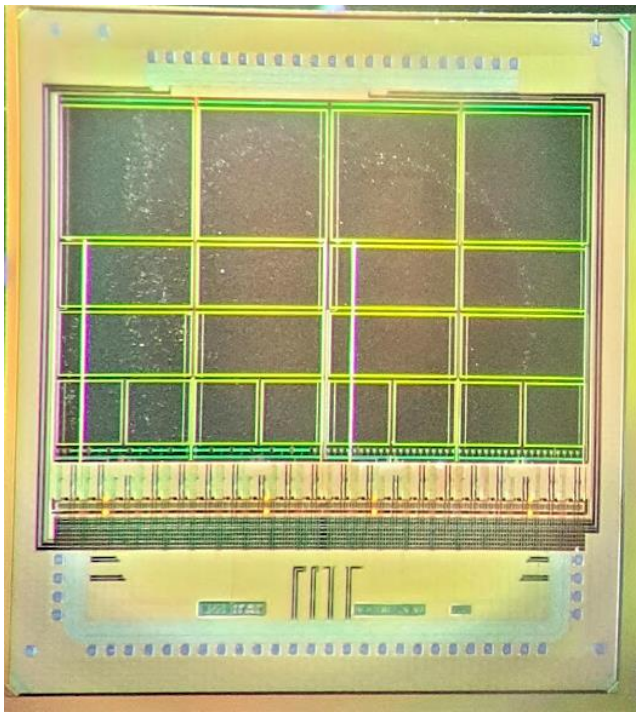

Fig. 3: The MiniCACTUS-V2 chip, recently received.

3. CONCLUSIONS

The second fabrication cycle of high-granularity DMAPS employing different CMOS technologies and different architectures was executed as originally planned leading to:

- A small size Mini-MALTA3 device to investigate the further improvements planned for the full size MALTA3 chip.
- A first full-size demonstrator ARCADIA-MD3 featuring small pixels, binary readout and backside biasing, together with the MADPIX DMAPS featuring gain
- A new prototype, Mini-CACTUS-V2, to explore achieving a time resolution beyond the results of the previous iteration

The devices have been made available to the groups participating in the work package and their performance is being evaluated. We conclude that with these successful chip submissions milestone M19 was fully met and can be considered to be accomplished.

4. REFERENCES

[1] D. Dobrijević, et al., “MALTA3: Concepts for a new radiation tolerant sensor in the TowerJazz 180 nm technology”, NIM A, vol 1040 1 October 2022, 167226, https://doi.org/10.1016/j.nima.2022.167226.

[2] L. Pancheri et al., "Fully Depleted MAPS in 110-nm CMOS Process With 100–300 µm Active Substrate," in IEEE Transactions on Electron Devices, vol. 67, no. 6, pp. 2393-2399, June 2020, doi:10.1109/TED.2020.2985639.

[3] Y. Gan, et al. “MiniCACTUS-V2: A HEP ASIC Prototype for 50ps Time Resolution”, *2023 30th IEEE International Conference on Electronics, Circuits and Systems (ICECS)*, Istanbul, 2023, pp. 1-4, doi: 10.1109/ICECS58634.2023.10382725.

ANNEX: GLOSSARY

Acronym	Definition
DMAPS	Depleted Monolithic Active Pixel Sensors