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Implementation and Comparison between Two Algorithms of Three-Level Neutral Point Clamped Voltage Source Inverter

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***Abstract*—**This paper presents a comparison between two Pulse Width Modulation (PWM) algorithms applied to a three-level Neutral Point Clamped (NPC) Voltage Source Inverter (VSI). The first algorithm applied is the triangular-sinusoidal strategy; the second is the Space Vector Pulse Width Modulation (SVPWM) strategy. In the first part, we present a topology of three-level NCP VSI. After that, we develop the two PWM strategies to control this converter. At the end the experimental results are presented.

***Keywords*—**Multilevel inverter, Space vector pulse width modulation (SVPWM), triangular-sinusoidal strategy.

I. Introduction

RECENTLY, developments in power electronics and semiconductor technology have lead improvements in lower electronic systems. Hence, different circuit configurations namely multilevel inverters have became popular and considerable interest by researcher are given on them [1-2]. Three-level Neutral Point Clamped (NPC) inverter shown in Fig. 1 has evolved into the standard for medium voltage motor drive systems as evidenced by the commercial availability of medium voltage drives based on both IGCT and high voltage IGBT devices. The topology has two important attributes that make it well suited to this market: lower harmonic content than a standard two level inverter, and the fact that the main switching devices are required to block only one-half of the dc bus voltage. This latter attribute has traditionally been exploited to allow for higher voltage drives since device voltages have been limited. However, it also implies that a drive of a given voltage can be obtained with lower voltage devices by employing the NPC topology.

Various PWM techniques for the three-level converter have been intensively studied since Nabae proposed the topology named neutral point clamped converter [3]. In various PWM techniques, the three-level SVPWM is one of most promising and widely applied PWM techniques in three phase systems. It is a naturally accepted view that three-level SVPWM is an extension of the conventional two-level SVPWM.

II. Modelling of Three-Level NPC Voltage Source Inverter

The three phases three-level NPC VSI is constituted by three legs and two DC voltage sources. Each leg has four bi-directional switches in series, and two diodes to get the zero voltage for V_{KM} (Fig. 1). Each switch is composed by a transistor and a diode in anti-parallel [4].

The switch connection function F_{KS} indicates the opened or closed state of the switch T_{KS}:

$$F_{KS} = \begin{cases} 1 & \text{if } T_{KS} \text{ close} \\ 0 & \text{if } T_{KS} \text{ open} \end{cases} \quad (1)$$

For a leg K of the three phases three-level NPC VSI, several complementary control laws are possible. The optimal control law of this inverter is:

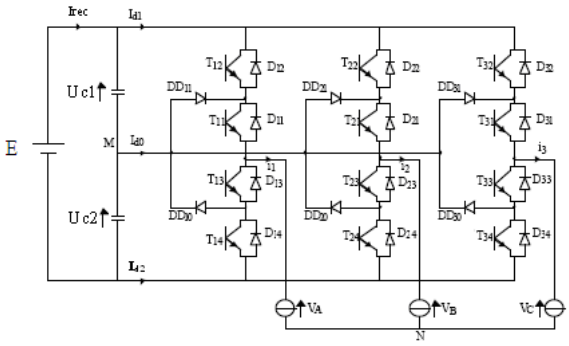

Fig. 1 Three-level NPC voltage source inverter

$$\begin{cases} F_{K4} = 1 - F_{K1} \\ F_{K3} = 1 - F_{K2} \end{cases} \quad (2)$$

Half leg connection function F_{Km}^{b} is defined as:

$$\begin{cases} F_{K1}^{b} = F_{K1} F_{K2} \\ F_{K0}^{b} = F_{K3} F_{K4} \end{cases} \quad (3)$$

m =1: for the lower half leg;
m =0: for the upper half leg.

As indicated in Table I, each leg of the inverter can have three possible switching states, P, O, or N. When the top two switches Ti1 and Ti2 are turned on, the switching state is P. When the medium switches Ti2 and Ti3 are turned on switching state is O. When the lower switches Ti3 and Ti4 are turned on, the switching state is N.

Fig. 2 shows the space vector diagram for three-level inverter. Since three kinds of switching states exist in each leg,

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this converter has 27 switching states, as indicated in the diagram. The output voltage vector can take only 18 discrete positions in the diagram because some switches state are redundant and create the same space vector.

TABLE I
STATES OF THREE-LEVEL INVERTER

Switching Symbols	Switching States				Output Voltage
	T_{i1}	T_{i2}	T_{i3}	T_{i4}	
P	ON	ON	OFF	OFF	U_{c1}
O	ON	OFF	ON	OFF	0
N	OFF	OFF	ON	ON	$-U_{c2}$

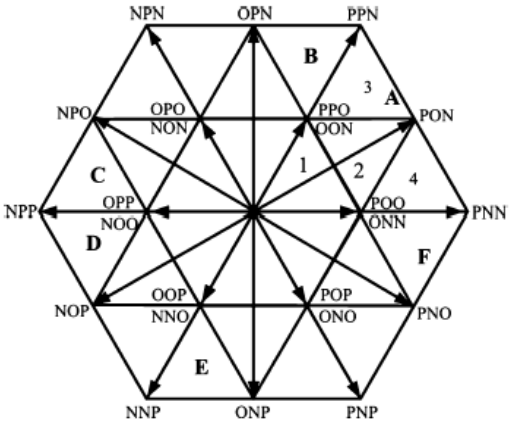

Fig. 2 Space vector diagram of a three-level inverter

III. THREE-LEVEL INVERTER CONTROL

A. Algorithm 1

This algorithm is based on the triangular-sinusoidal strategy with two carriers [5-6], is divided to four parts.

1. Part 1

Determination of the generating conversion functions n_{gK}:

$$n_{gK} = \frac{V_{sref}}{E/2} \tag{4}$$

2. Part 2

Determination of the half leg generating connection functions F^{b}_{Kmg}:

$$F^{b}_{K1g} = \frac{n_{gK}}{2}\ ,\quad F^{b}_{K0g} = -\frac{n_{gK}}{2} \tag{5}$$

3. Part 3

Determination of the half leg connection functions F^{b}_{Km}

$$\begin{cases} T_{K1} = T_h\,(1-\left|F^{b}_{K1g}\right|) \\ T_{K0} = T_h\,(\frac{1}{2}-\left|F^{b}_{K0g}\right|) \end{cases} \tag{6}$$

$$\begin{cases} \frac{T_h}{2}-\frac{T_{K1}}{2} \le t \le \frac{T_h}{2}+\frac{T_{K1}}{2} \Rightarrow \quad a_K = 1 \\ (t<\frac{T_h}{2}-\frac{T_{K1}}{2}) ou (t>\frac{T_h}{2}+\frac{T_{K1}}{2}) \Rightarrow a_K = 0 \end{cases} \tag{7}$$

$$\begin{cases} F^{b}_{K1g} > 0 \Rightarrow (F^{b}_{K1} = a_K)\,\&\,(F^{b}_{K0} = 0) \\ F^{b}_{K1g} \le 0 \Rightarrow (F^{b}_{K1} = 0)\,\&\,(F^{b}_{K0} = a_K) \end{cases} \tag{8}$$

4. Part 4

Determination of the control order of the switch B_{Ki}

$$\begin{cases} ((F^{b}_{K1}=1)\,\&\,(F^{b}_{K0}=1)) \\ \quad or \qquad\qquad\qquad \Rightarrow F_{K1}=1, F_{K2}=0 \\ ((F^{b}_{K1}=0)\,\&\,(F^{b}_{K0}=0)) \\ \quad or \\ ((F^{b}_{K1}=1)\,\&\,(F^{b}_{K0}=0)) \Rightarrow F_{K1}=1, F_{K2}=1 \\ \quad or \\ ((F^{b}_{K1}=0)\,\&\,(F^{b}_{K0}=1)) \Rightarrow F_{K1}=0, F_{K2}=0 \end{cases} \tag{9}$$

$$\begin{cases} F_{Ki}=1 \Leftrightarrow B_{Ki}=1 \\ F_{Ki}=0 \Leftrightarrow B_{Ki}=0 \end{cases} \tag{10}$$

The Fig. 3 shows the simple output voltage of the three-level NPC VSI controlled by the proposed algebraic strategy for m=12 and r=0.8. The spectral analysis of this voltage shows that the total harmonics distortion is higher than 60%.

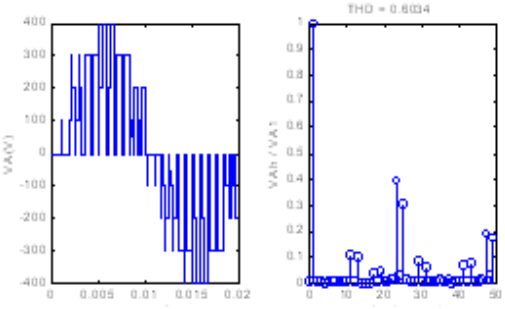

Fig. 3 Simple output voltage V_A and its spectral analysis for m=12, r=0.8

B. Algorithm 2

27 vectors can construct the space-vector diagram of a three level converter, shown as Fig. 2. There are 24 active vectors including 12 short vectors, 6 medium vectors and 6 long vectors, and the remaining three are zero vectors (PPP, OOO, NNN), which lie at the center of the hexagon [7-8]. The area of the hexagon can be divided into six sectors (A to F), each of which has four regions (1 to 4), with 24 regions of operation in

total. This algorithm used in this paper is composed by six steps described in the following Fig. 4.

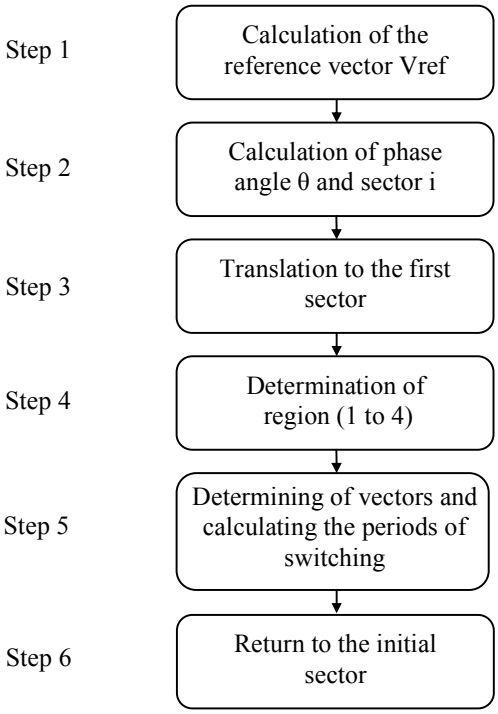

Fig. 4 Steps of SVPWM

The Fig. 5 shows the simple output voltage of the three-level NPC VSI controlled by the proposed Space Vector Pulse Width Modulation strategy for m=12 and r=0.8. The spectral analysis of this voltage shows that the total harmonics distortion is lower than 40.

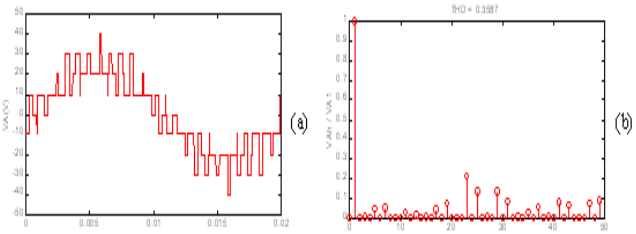

Fig. 5 Simple output voltage Va and its spectral analysis for m=24, r=0.8

IV. Experimental Result

The input voltage of the three-level neutral point clamped voltage source inverter is E = 60V. This converter fed a three phases R-L load where R=22Ω and L=340mH.

Figs. 6 and 9 present the voltage V_{AM} of the first leg of inverter controlled by algorithms 1 and 2. The output voltage V_A and its spectral analysis for the two algorithms are presented in Figs. 7, 8, 10 and 11.

One remarks that the total harmonics distortion obtained by the second algorithm is better than the THD obtained by the first algorithm.

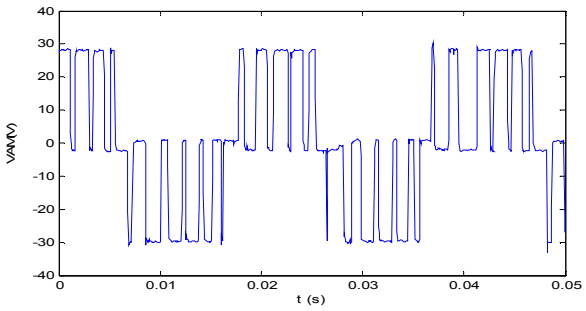

Fig. 6 Voltage V_{AM} (Algorithm 1)

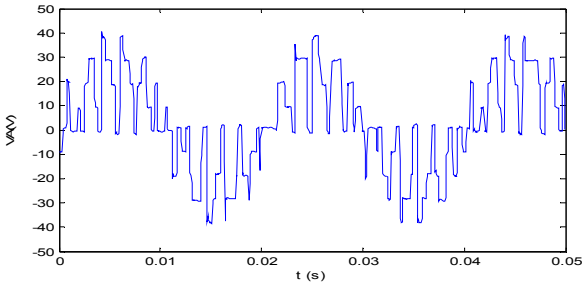

Fig. 7 Simple output voltage V_A (Algorithm 1)

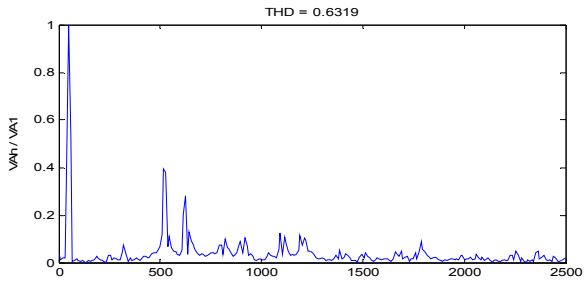

Fig. 8 Spectral analysis of output voltage V_A (Algorithm 1)

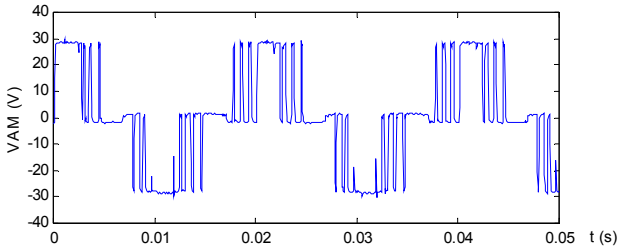

Fig. 9 Voltage V_{AM} (Algorithm 2)

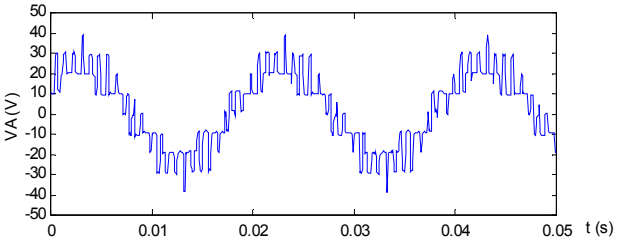

Fig. 10 Simple output voltage V_A (Algorithm 2)

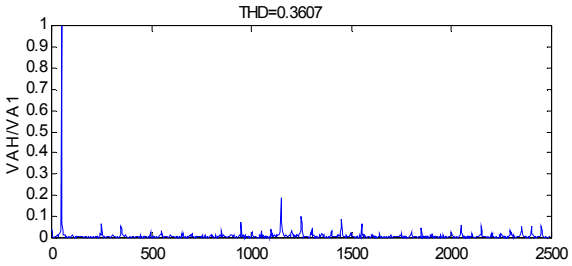

Fig. 11 Spectral analysis of output voltage V_A (Algorithm 2)

V. Conclusion

This paper presents the comparison between two algorithms of the three-level NPC converter. The modelling of this inverter shows that it is equivalent to two two-level inverters in series.

The triangular-sinusoidal and space vector PWM algorithms for a three level inverter have been simulated using C++. Simulation and experimental results have been given for R-L load. It has been shown that high quality of waveforms obtained by space vector PWM strategy.

References

[1] P.M. Bhagwat and V.R. Stefanovic, "Generalized Structure of A Multilevel Inverter", IEEE Trans. on I.A., Vol. IA-19, n.6, 1983, pp. 1057-1069.

[2] S.K. Mondal, J.O.P Pinto, B.K. Bose, "A Neural-Network-Based Space Vector PWM Controller for a Three-Level Voltage-Fed Inverter Induction Motor Drive", IEEE Trans. on I.A., Vol. 38, no. 3, May/June 2002, pp.660-669.

[3] A. Nabae, I. Takahashi, and H. Akagi, "A new neural-point-clamped PWM inverter," IEEE Trans Ind. Appl., vol. IA-17, no. 5, pp. 518–523, Oct. 1981.

[4] N. Celanovic, D. Boroyevich, "A Comprehensive Study of Neutral-Point Voltage Balancing Problem in Three-Level Neutral-Point-Clamped Voltage Source PWM Inverters," In IEEE Transactions on Power Electronics, Vol. 15, No. 2, pp. 242-250, 2000.

[5] S.R.Bowes, T Davis, Novel approach to the analysis of modulation processes in power convertors, IEE Proc, Vol 122,N°5,May 1975.

[6] F. Bouchafaa, E.M. Berkouk, M.S. Boucherit, "Modelling and control of a power electronic cascade for the multi DC bus supply" ,The International Journal for Computation and Mathematics in Electrical and Electronic Engineering Vol. 27 No. 5, 2008.

[7] Haibing Hu, Wenxi Yao, and Zhengyu Lu, "Design and Implementation of Three-Level Space Vector PWM IP Core for FPGAs," In. IEEE transactions on power electronics, Vol. 22, No. 6, november 2007

[8] S. K. Mondal, B. K. Bose, and V. Oleschuk, "Space vector pulse width modulation of three-level inverter extending operation into over modulation region," IEEE Trans. Power Electron., vol. 18, no. 2, pp.604–611, Mar. 2003.