

Analysis and Design of a Novel Active Soft Switched Phase-Shifted Full Bridge Converter

Naga Brahmendra Yadav Gorla, Dr. Lakshmi Narasamma N

Abstract—This paper proposes an active soft-switching circuit for bridge converters aiming to improve the power conversion efficiency. The proposed circuit achieves loss-less switching for both main and auxiliary switches without increasing the main switch current/voltage rating. A winding coupled to the primary of power transformer ensures ZCS for the auxiliary switches during their turn-off. A 350 W, 100 kHz phase shifted full bridge (PSFB) converter is built to validate the analysis and design. Theoretical loss calculations for proposed circuit is presented. The proposed circuit is compared with passive soft switched PSFB in terms of efficiency and loss in duty cycle.

Keywords—Active soft switching, passive soft switching, ZVS, ZCS, PSFB.

I. INTRODUCTION

PHASE shifted full bridge (PSFB) DC-DC converter is extensively used in applications such as automobile inverters, telecom power supplies, un-interrupted power supplies, stand-alone/grid connected inverters fed from renewable energy sources. The phase shift introduced between two legs creates additional freewheeling intervals in the primary side. Output voltage is a function of the phase shift. This topology uses transformer's leakage inductance and intrinsic capacitance of switching devices to achieve ZVS for the active switches [1]- [4]. Analysis of lagging, leading leg transitions and ZVS range calculations has been reported in [1], [5] respectively. In these topologies, energy stored in the leakage inductor may not be sufficient to achieve ZVS for the lagging leg under high input voltage and/or light load conditions.

PSFB with passive soft switching circuits for wide ZVS ranges has been presented in [6]- [10]. In these topologies, the additional series inductance in the primary of transformer adversely affects the performance of the converter causing the loss in duty cycle and severe voltage ringing across the devices in the secondary side [11].

All the active soft switched PSFB converters have auxiliary circuit added in parallel to the full bridge, which ensures soft switching for main switches. The active soft switching circuits for PSFB has been reported in [8]- [16]. The limitations in these topologies are narrow ZVS range of load, loss in duty cycle, the voltage stress across the devices in the secondary side, circulating loss in the primary side circuit etc.

A new active soft switching circuit for bridge converters is proposed in this paper which addresses some of the problems mentioned above. PSFB topology is chosen to validate the analysis. Proposed circuit is connected in parallel to the

lagging leg as shown in Fig. 1 to achieve ZVS for switches in lagging leg. Novelty of the circuit lies in achieving zero voltage switching for main switches in lagging leg, zero current switching for active switches in auxiliary circuit.

This paper is organized as follows: Steady state analysis with necessary mathematical expressions and waveforms of the proposed circuit is discussed in section II. Design strategy and experimental results of the proposed converter are covered in section III and IV respectively. Theoretical loss calculations and loss in duty cycle are presented in sections V and VI respectively. Section VII presents the conclusion and references.

II. STEADY STATE ANALYSIS

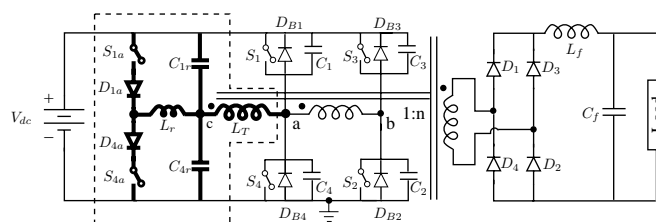


Fig. 1. Proposed active soft switched full bridge DC-DC converter with Auxiliary circuit.

Steady state analysis of proposed PSFB is presented in this section. Analysis of converter is divided into twelve intervals. In the following analysis, voltage drops across the devices are neglected. The output filter inductor is large enough to assume constant load current. Turns ratio between the primary of power transformer and coupled winding (L_T) is chosen as k_T . Switching sequence and switching transients are shown in Fig. 3. Magnified portion of the image selected by the rectangle box in Fig. 3 is depicted in Fig. 4. θ is the phase shift introduced between lagging and leading legs of PSFB. The auxiliary switches are gated prior to the corresponding main switches in order to ensure their ZVS.

Interval 0 ($t < t_0$): Prior to t_0 , anti parallel diode D_{B1} and S_2 are in conduction. Gating S_1 at $t=t_0$ ensures ZVS to the main switch S_1 . L_m is magnetizing inductance of transformer.

$$C_1 = C_2 = C_3 = C_4 = C; C_{4r} = C_{1r} = C_r$$

$$v_{C1}(t_0) = v_{C2}(t_0) = 0; v_{C3}(t_0) = v_{C4}(t_0) = V_{dc}; i'(t_0) = nI$$

Interval 1 ($t_0 < t < t_1$): This is positive power transfer interval wherein, main switches S_1, S_2 , output rectifier diodes D_1, D_2 are in conduction carrying full load current. Fig. 2(a) illustrates circuit conditions during interval 1.

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Voltage across the primary (v_{ab}) and reflected load current (i') during this interval are given as,

$$L_m \frac{di_m(t-t_0)}{dt} = v_{ab}(t-t_0) = V_{dc}$$

$$i_p(t-t_0) = i'(t-t_0) + i_m(t-t_0) = nI + i_m(t-t_0)$$

At $t = t_1$, gating to main switch S_2 is removed.

Interval 2 ($t_1 < t < t_2$): When gating to S_2 falls below the threshold level, primary current (i_p) which was initially flowing through S_2 , will now flows through the capacitor C_2 . C_2 across the switch S_2 is chosen such that turn-off of S_2 is a loss less transition. Rectifier diodes D_1 and D_2 continues to conduct since voltage across the primary of transformer is positive. Magnetizing current is assumed to be at i_m^* . Fig 2(b) explains circuit conditions during interval 2.

$$\frac{dv_{C3}(t-t_1)}{dt} = \frac{i_p(t-t_1)}{2C}$$

$$V_{dc} - L_m \frac{di_p(t-t_1)}{dt} - v_{C2}(t-t_1) = 0,$$

where $i_p(t-t_1) = i'(t-t_1) + i_m(t-t_1) = nI + i_m^*$

At the end of interval 2, S_3 is turned on with a delay t_d as shown in Fig. 3. The design should ensures that C_3 discharge completely and D_{B3} begins to conduct within the time delay.

Interval 3 ($t_2 < t < t_3$): This is freewheeling interval wherein, main switch S_1 and diode D_{B3} are in conduction as shown in Fig 2(c). Voltage across the primary of the transformer is zero, all the output rectifier diodes are in conduction sharing full load current equally. This makes the reflected load current in the primary of the transformer zero. Magnetizing current (i_m^*) freewheels in the transformer primary during this interval.

$$L_m \frac{di_m(t-t_2)}{dt} = 0; i_m(t-t_2) = i_m^*$$

$$i_p(t-t_2) = i'(t-t_2) + i_m(t-t_2) = i_m^*$$

$$i_{D1}(t-t_2) = i_{D3}(t-t_2) = \frac{I}{2}$$

Interval 3 ends at $t = t_3$, when gating to S_1 is removed.

Interval 4 ($t_3 < t < t_4$): This is the interval during which auxiliary circuit becomes active. Main switch S_1 is turned off and auxiliary switch S_{4a} is gated at $t = t_3$. Fig. 2(d) describes circuit conditions during interval 4. Voltage across the resonant inductor (v_{Lr}) is V_{dc} during this interval. Current through resonant inductor raises linearly as,

$$i_{Lr}(t) = \frac{V_{dc}}{L_r}(t-t_3)$$

$$i'(t-t_3) = n(i_{D1}(t-t_3) - i_{D3}(t-t_3))$$

At the end of this interval i.e., at $t = t_4$ auxiliary inductor current reaches load current, D_3 and D_4 starts conducting full load current.

$$T_1 = \frac{L_r n I}{V_{dc}}, \text{ where } T_1 = (t_4 - t_3) \quad (1)$$

Interval 5 ($t_4 < t < t_5$): Resonant elements L_r and C_{4r} resonates during this interval. Fig 2(e) shows the circuit

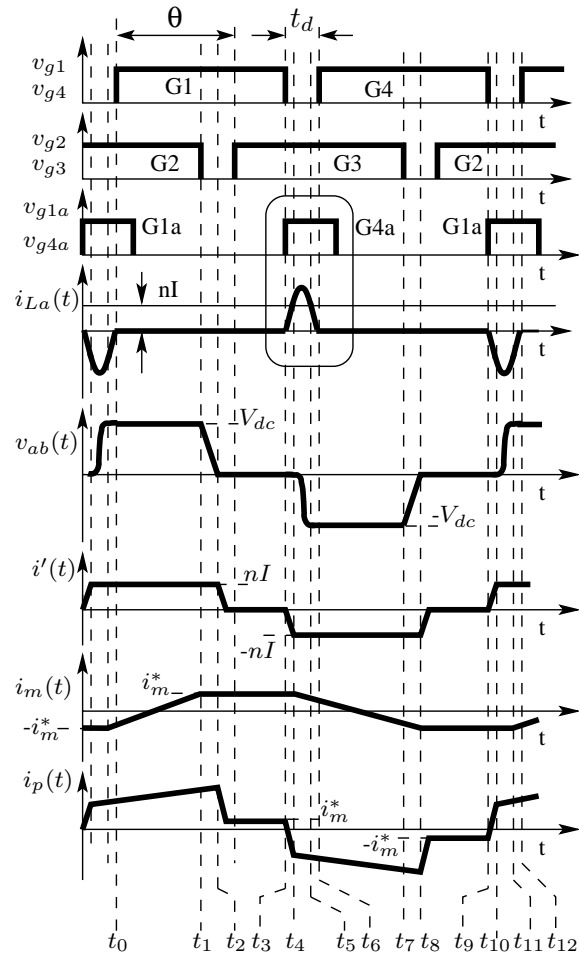


Fig. 3. Key waveforms for proposed Active Soft Switched PSFB DC-DC converter

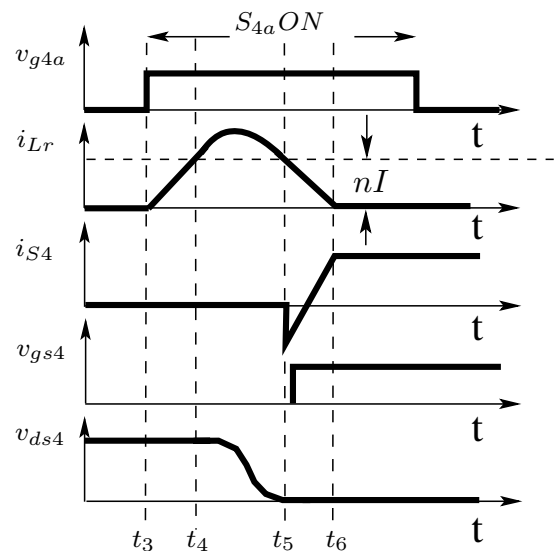


Fig. 4. Auxiliary interval waveforms

condition during this interval. Resonant inductor current (i_{Lr})

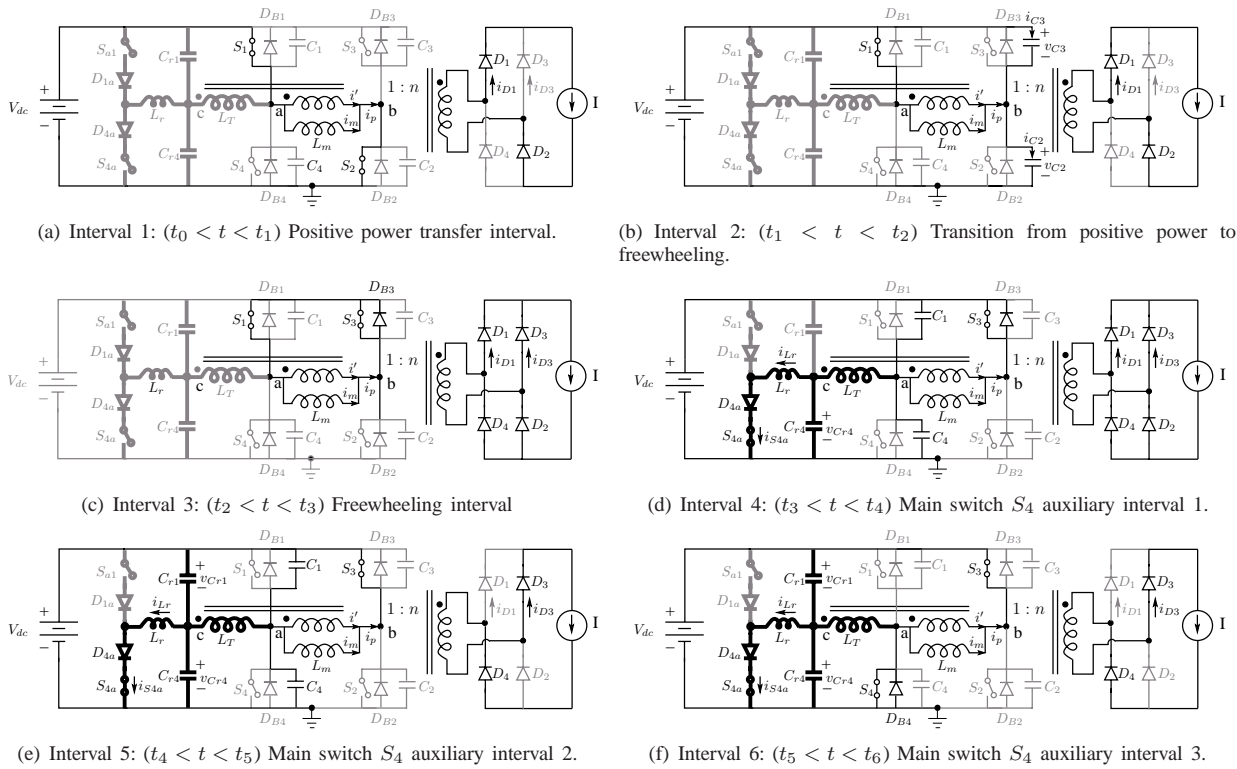


Fig. 2. Proposed active soft switched converter circuit conditions for intervals 1-6.

and resonant capacitor voltage (v_{Cr}) are given as,

$$i_{Lr}(t - t_4) = nI + V_{dc} \sqrt{\frac{C_r}{L_r}} \sin(w(t - t_4)) \quad (2)$$

$$v_{Cr}(t - t_4) = V_{dc} \cos(w(t - t_4)), \text{ where } w = \frac{1}{\sqrt{L_r C_r}}$$

At the end of this interval, at $t = t_5$

$$V_{dc} \cos(w(t_5 - t_4)) = \frac{-V_{dc}}{k_T}$$

$$T_2 = (t_5 - t_4) = \frac{1}{w} \cos^{-1}\left(\frac{-1}{k_T}\right) \quad (3)$$

At the end of this interval, voltage across resonant capacitor reaches $\frac{-V_{dc}}{k_T}$. This forward biases the anti parallel diode D_{B4} across the main switch S_4 as shown in Fig. 4.

Interval 6 ($t_5 < t < t_6$): Fig 2(f) shows the circuit condition during interval 6. Voltage across the Resonant capacitor is $\frac{-V_{dc}}{k_T}$ which resets the resonant inductor current to zero as,

$$i_{Lr}(t) = i_{Lr}(t_5) - \frac{V_{dc}}{k_T L_r} (t - t_5)$$

$$= (nI + V_{dc} \sqrt{\frac{C_r}{L_r}} \left(\frac{\sqrt{k_T^2 - 1}}{k_T}\right)) - \frac{V_{dc}}{k_T L_r} (t - t_5)$$

At the end of this interval, at $t = t_6$

$$T_3 = \frac{nI k_T L_r}{V_{dc}} + w_r \sqrt{k_T^2 - 1}; \text{ where, } T_3 = (t_6 - t_5) \quad (4)$$

Turning off S_{4a} after $i_{Lr}(t)$ becoming zero ensures ZCS during turn-off for the auxiliary switch. Gating S_4 after $t = t_5$ ensures ZVS during turn-on.

Interval 7 ($t_6 < t < t_7$): Main switches S_3 , S_4 output rectifier diodes D_3 , D_4 are in conduction during this interval.

$$L_m \frac{di_m(t - t_6)}{dt} = v_{ab}(t - t_6) = -V_{dc}$$

$$i_p(t - t_6) = i'(t - t_6) + i_m(t - t_6); i'(t - t_6) = -nI$$

Analysis of interval 8 to 12 is similar to that of intervals 1 to 7.

III. DESIGN STRATEGY

Design guidelines for proposed PSFB DC-DC converter is presented in this section.

A. Filter components design

- 1) The process of selecting filter inductor (L_f), filter capacitor (C_f) is same as the traditional PWM bridge converters.
- 2) In the proposed topology, voltage and current rating of the active and passive devices are same as the conventional PWM bridge converter.

B. Auxiliary circuit components design

The auxiliary circuit components design include design of resonant inductor and capacitor.

- 1) Ratio between resonant frequency f_r and switching frequency f_s is so chosen that losses due to resonant circuit should be low.

$$f_r = k * f_s = \frac{1}{2\pi\sqrt{L_r C_r}} \quad (5)$$

2) Interval 5 in steady state analysis describes the resonant intervals. During these intervals, auxiliary inductor L_r resonates with auxiliary capacitor C_r . The peak resonant inductor current (i_{PLr}) is given as,

$$i_{PLr} = nI + V_{dc} \sqrt{\frac{C_r}{L_r}} \quad (6)$$

3) The rate of rise of current in the auxiliary circuit during the interval 5 depends on L_r .

- Larger value of L_r increases the length of the interval T_1 as well as T_2 . Effective duty cycle also gets reduced because of Larger T_1 .
- Smaller value of L_r increases the peak of auxiliary inductor current which intern increases the conduction losses.

C. Choice of coupled inductor turns

Turns ratio between primary of power transformer and coupled inductor (k_T) decides the resonant period T_2 as well as resetting period for auxiliary inductor current T_3 .

- For a given k_T , resonant period T_2 is given by equation 3 and auxiliary current resetting period is given by equation 4.

Specifications of proposed active soft switched PSFB DC-DC converter for 350 W based on the above design strategies are shown in table I. The proposed circuit is compared with traditional passive soft switching circuit reported in [1] in terms of steady state losses and loss in duty cycle in the subsequent sections.

TABLE I

SPECIFICATIONS OF PROPOSED ACTIVE SOFT SWITCHED PSFB DC-DC CONVERTER

S.no	description	values
1	Supply voltage	40-57 Volts
2	Output voltage	400 Volts
3	Output power	350 Watts
4	Filter inductance	10 mH
5	Filter capacitance	5.6 μ F
6	Resonant inductance	1 μ H
7	Resonant capacitance	15 nF
8	Switching frequency	100 kHz

IV. RESULTS AND DISCUSSIONS

Table I shows the design specifications used in building laboratory test setup and in simulations. Efficiency of passive soft switched and Proposed active soft switched converter is compared in Table II.

Gating sequence of auxiliary switches and corresponding lagging leg switches are shown in fig. 5. Gating for auxiliary switch S_{4a} , auxiliary inductor current (I_{Lr}), gate to source and drain to source voltage of main switch S_4 are shown in fig. 6. It can be observed that, the auxiliary inductor current (I_{Lr}) raises from zero when gating is given to auxiliary switch S_{4a} . This reduces the turn-on losses in the auxiliary switch. Gating to auxiliary switch S_{4a} is removed when I_{Lr} is reset. This reduces the turn-off losses in S_{4a} . RMS current through the auxiliary switches (I_{Lr}) is less since it is operated for small durations. Hence conduction losses in the auxiliary switches

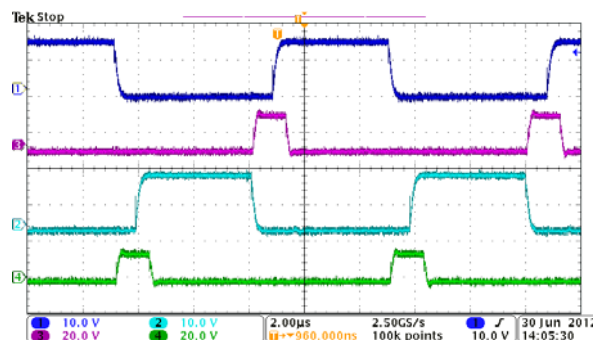


Fig. 5. (From top) gating to the switch S_1 (scale=10 V/div), gating to auxiliary switch S_{1a} (scale=20 V/div), gating to switch S_4 (scale=10 V/div), gating to auxiliary switch S_{4a} (scale=20 V/div), x-axis scale=2 μ s/div.

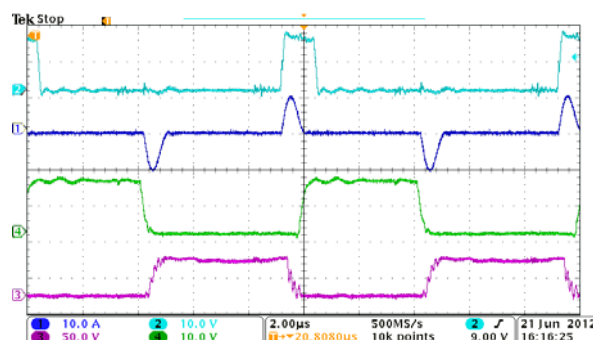


Fig. 6. (From top) gating to the auxiliary switch S_{4a} (scale=10 V/div), auxiliary inductor current (scale=10 A/div), gate to source voltage of S_4 (scale=10 V/div), drain to source voltage of S_4 (scale=50 V/div) at 20% load, x-axis scale=2 μ s/div.

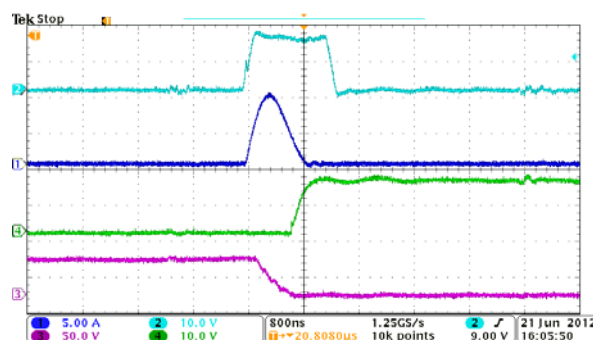


Fig. 7. (From top) gating to the auxiliary switch S_{4a} (scale=5 V/div), auxiliary inductor current (scale=5 A/div), gate to source voltage of S_4 (scale=10 V/div), drain to source voltage of S_4 (scale=50 V/div) at 20% load, x-axis scale=800 ns/div.

are less even though peak current is more than load current. Drain to source voltage for lagging leg switch is zero when it is switched on with auxiliary circuit. This reduces turn-on losses in lagging leg switches (fig. 7, fig 8) contributing an overall improvement in the conversion efficiency as shown in table II.

V. LOSS CALCULATIONS

Auxiliary inductor current is approximated as triangular wave for reducing the complexity of analysis. The RMS

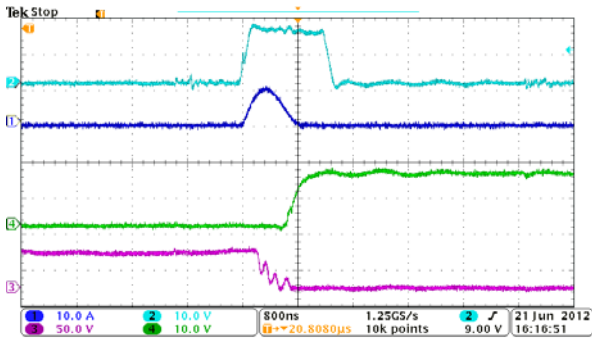


Fig. 8. (From top) gating to the auxiliary switch S_{4a} (scale=10 V/div), auxiliary inductor current (scale=10 A/div), gating to lagging leg switch S_4 (scale=10 V/div), drain to source voltage of S_4 (scale=50 V/div) at 80% load, x-axis scale=800 ns/div.

current through resonant inductor is given as

$$I_{Lr_{rms}} = I_{PLr} \sqrt{\frac{2(T_1 + T_2 + T_3)f_s}{3}} \quad (7)$$

where T_1, T_2, T_3 are given by equations 1, 3, 4 respectively.

Auxiliary circuit losses include conduction losses in auxiliary switches (S_{1a}, S_{4a}), and auxiliary diodes (D_{1a}, D_{4a}). The switching losses in active switches of the auxiliary circuit are zero due to ZCS as stated earlier (fig. 6). Auxiliary circuit loss is approximately 6.75% of passive soft switching losses.

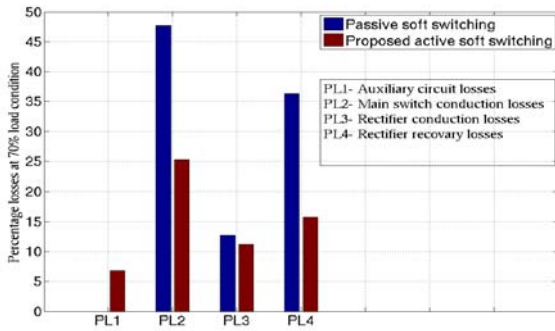


Fig. 9. Theoretical loss calculation of a 350 W proposed active soft switched PSFB and passive soft switched PSFB. The losses are calculated for several items: PL1-auxiliary circuit losses; PL2-main circuit conduction losses; PL3-rectifier diodes conduction losses; PL4-rectifier diode recovery losses at 70% load condition.

Theoretical loss calculations for 350 W proposed active soft switched PSFB and passive soft switched PSFB converter at 70% load conditions are compared in fig. 9. The proposed auxiliary circuit reduces the main switch switching losses, improving the over all conversion efficiency of converter as shown in Table II. Conduction loss in the main switches of proposed active soft switched PSFB is approximately half of passive soft switched PSFB due to the fact that the current during freewheeling intervals is magnetizing current instead of reflected full load current. Output rectifier diode current during freewheeling period is reduced to half of load current in the proposed active soft switched PSFB converter, in turn reduces the rectifier conduction and recovery losses considerably as

depicted in fig. 9. There is an over all reduction of 37.3% in losses with proposed active soft switched PSFB at 70 % load condition.

VI. LOSS IN DUTY CYCLE WITH PROPOSED ACTIVE AND PASSIVE SOFT SWITCHING

A. Passive soft switching

Loss in duty cycle for passive soft switching case is ΔD_p as reported in [1].

$$\begin{aligned} \Delta D_p &= \frac{2n_p(i_1 + i_2)f_s L_s}{V_{dc}} \\ &\cong \Delta D_p = \frac{4n_p I f_s L_s}{V_{dc}} \end{aligned} \quad (8)$$

Effective duty cycle in passive soft switching PSFB converter (D_{effp}) is

$$D_{effp} = D - \Delta D_p$$

Effective output voltage of the converter in passive soft switching PSFB (V_{op}) is given as

$$\begin{aligned} V_{op} &= V_{dc} n_p D_{effp} \\ &= V_{dc} n_p (D - \frac{4n_p I f_s L_s}{V_{dc}}) = V_{dc} n_p D - 4n_p^2 I f_s L_s \end{aligned}$$

where, n_p is number of turns of power transformer in passive soft switched PSFB converter.

B. Proposed Active soft switching

Interval 4 explains the first auxiliary interval in the proposed converter. All the rectifier diodes are in conduction till the auxiliary inductor current reaches reflected load current. This reduces the effective duty of the converter. Loss in the duty corresponds to the period T_1 is ΔD_a .

$$\Delta D_a = \frac{2n_a I L_r f_s}{V_{dc}} \quad (9)$$

Effective duty cycle in proposed active soft switching PSFB converter (D_{effa}) is

$$D_{effa} = D - \Delta D_a$$

Effective output voltage of the converter in proposed circuit (V_{oa}) is given as

$$\begin{aligned} V_{oa} &= V_{dc} n_a D_{effa} \\ &= V_{dc} n_a (D - \frac{2n_a I f_s L_r}{V_{dc}}) = V_{dc} n_a D - 4n_a^2 I f_s L_r \end{aligned}$$

where, n_a is number of turns of power transformer in proposed active soft switched PSFB converter. Loss in duty cycle of the proposed active soft switched PSFB and passive soft switched PSFB for different load conditions is plotted for common specifications given in table I. It can be seen from the fig. 10 that for any given load, output voltage can be realized with minimum duty loss in the proposed active soft switched converter.

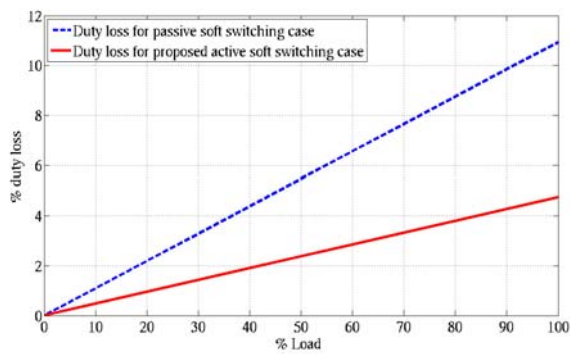


Fig. 10. Loss in duty cycle for passive soft switching PSFB and proposed circuit under different load conditions.

TABLE II
EFFICIENCIES FOR PASSIVE AND ACTIVE SOFT SWITCHED PSFB DC-DC.

% load	Passive Soft Switched $\% \eta$	Proposed Active Soft Switched $\% \eta$
15	79.83	85.10
20	78.19	88.36
30	82.35	92.57
40	81.46	89.75
50	82.5	89.45
60	84.38	89.5
70	84.02	89.56
80	83.99	87.60
90	83.43	87.79
100	83.42	86.95

VII. CONCLUSION

A new active soft switching circuit for bridge converters is proposed in this paper. The novelty of the proposed circuit lies in achieving ZVS during turn-on for main switch and ZCS during turn-on and turn-off for the auxiliary switches. Proposed circuit is compared with conventional passive soft switched PSFB in terms of steady state efficiency and loss in duty cycle. There is an efficiency improvement of about 5% at 70% load condition. Improvement in efficiency is observed from 10% to 100% load conditions.

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