Signal Integrity Analysis of Coupled Thin-Film Microstrip Lines (TFMSLs)

Khitem Lahbacha, Giulia Di Capua, Gianfranco Miele, Antonio Maffucci
Dept. of Electrical and Information Eng., University of Cassino and Southern Lazio, Via G. Di Biasio 43, 03043 Cassino, Italy
{khitem.lahbacha, giulia.dicapua, g.miele, maffucci @unicas.it}

Thi Dao Pham, Djamel Allal
Laboratoire national de métrologie et d'essais, 29 Avenue Roger Hennequin, 78197 Trappes Cedex, France.
{thi-dao.bui, djamel.allal @lne.fr}

Gia Ngoc Phung, Uwe Arz
Physikalisch-Technische Bundesanstalt, Bundesallee 100, 38116 Braunschweig, Germany.
{gia.phung, Uwe.Arz @ ptb.de}

***Abstract*— This paper analyzes the Signal Integrity (SI) performance of thin-film microstrip lines (TFMSL), in view of their use in future communication systems, operating at unprecedented high I/O data rates (over 30 Gb/s) and high frequency (over 60-GHz). Here, various chip-level structures with coupled TFMSL are analyzed, with a special focus on mismatching and coupling associated with different choices of geometry. A frequency domain analysis is carried out using two commercial simulation tools to estimate insertion loss, crosstalk, and mode conversion. A high-speed digital link is then simulated in the time domain to evaluate the SI performance in terms of eye-diagram metrics, over a wide range of data-rate values, from 1 to 100 Gbit/s. The effect of the geometry and coupling is analyzed, and design maps are obtained, suggesting trade-off optimized choices of data-rate values, given the line geometries.**

Keywords*— *crosstalk, data rate, Signal Integrity, insertion loss, jitter, TFMSL.

I. INTRODUCTION

The thin-film microstrip line (TFMSL) is a well-established technology successfully adopted in many high-speed applications like multichip modules (MCMs) [1], monolithic microwave integrated circuits (MMICs) [2], or microstrip samplers [3]. The main advantages of the TFMSLs are related to their scalability of dimensions and metallization. The miniaturized dimensions allow these microstrip lines located on the top layers to be used as interconnects in technology platforms with a high density of integration of components. In addition, the use of their ground plane as a shield results in a reduction of the effects of the substrate. In this way, TFMSLs can be used with low-resistivity substrates at very high frequencies without the known issues of signal degradation (e.g., dispersion) associated with the use of such substrates [4].

In this paper, we analyze the use of TFMSL lines in circuits designed for the 5th generation of mobile communication systems (5G). The work is carried out in the frame of the FutureCom project, "RF measurements for future communication applications" [5]-[6], whose main goal is to assess effective technological solutions to the main challenges related to future communication standards.

Specifically, this paper compares several types of TFMSLs integrated at the chip level in terms of Signal Integrity (SI) performance to study the effects related to the geometry and the data rate. Communication standards like 5G require operating at unprecedented high I/O data rates (over 30 Gb/s) and high frequency (over 60 GHz). Therefore, designing these systems will be only possible based on reliable design guidelines assessed through accurate characterization (e.g., high-frequency characterization, [7]) and modeling activity (e.g., SI analysis, [8]-[9]). More generally, the complexity of the electronic design and the increase in the system performances lead to an increase in design challenges [10], which can only be faced with a thorough understanding of the design rules to be applied.

The reference system analyzed here is a high-speed digital link whose generic layout is shown in Fig. 1: a TFMSL is used to connect a driver to a receiver buffer. The driver transmits signals at high Gbit/s rates, as the above-mentioned communication standards require.

The effects on the link performance due to mismatch associated with the TFMSL geometry are studied by analyzing in detail the behaviour of insertion loss, mode conversion, crosstalk noise, and eye-diagram parameters.

The paper is organized as follows. Section II describes the proposed TFMSL structures. Section III provides a frequency domain analysis of the interconnects, with the estimation of mode conversion and insertion losses, while in Section IV, a time-domain analysis of the overall link is carried out, and the eye-diagram parameters are evaluated. Finally, conclusions are drawn in Section IV.

II. DESCRIPTION OF THE TFMSL STRUCTURES

The TFMSL structures analyzed in this paper are coupled transmission lines printed on the top layer of a chip. The substrate is made by SU-8, which is an epoxy-based photoresist designed for microelectronic applications where chemical and thermal stability is desired [11]. One of the analyzed lines is shown in Fig.2, namely a non-uniform transmission line, in which a tract imposes a geometrical mismatch (change in the characteristic impedance) with a bend of 135°. The reference case (hereafter, the matched line) is the same structure with uniform lines, which is designed to have a nominal characteristic impedance equal to 50 Ω. The design parameters are reported in Table I.

Furthermore, two additional lines have been analyzed, with two different values of the distances between the two coupled traces, as shown in Fig. 3.

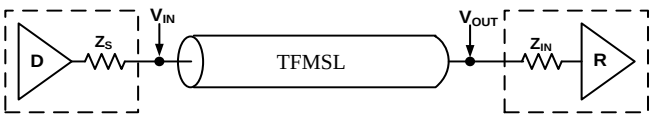

Fig. 1. Schematic layout of the analysed driver-line-receiver link.

Link to publisher version with DOI: 10.1109/SPI57109.2023.10145525

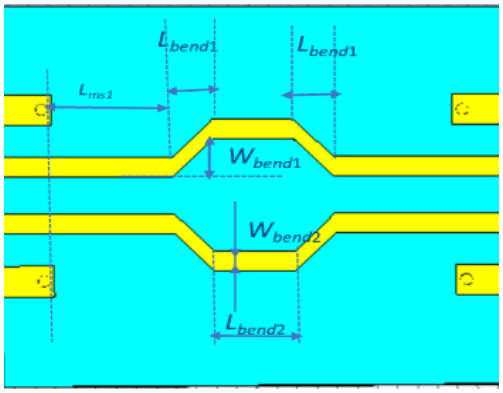

Fig. 2. Parallel coupled TFMSLs, with bent trace 135°.

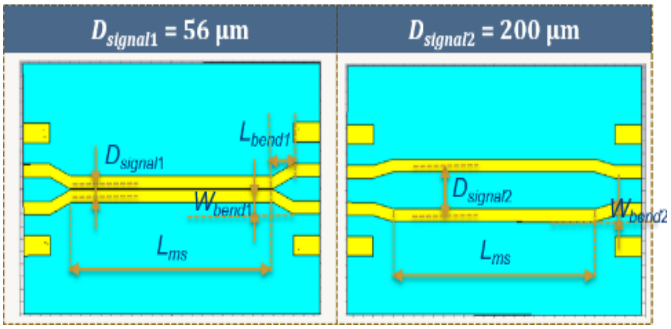

Fig. 3. Additional case studies, with two different values of the distances between the two signal traces: D1 (56µm) and D2 (200µm).

TABLE I. PARAMETERS FOR THE ANALYSED TFMSL STRUCTURES

Parameter	Dimension (µm)
Pad width W_{pad}	80
Line width W_{ms}	52
Step width W_{step}	12
Pitch size S	150
Line length L_{ms}	1000
Pad length L_{pad}	130
Line thickness H_{ms}	0.5
Substrate thickness H_s	20
Ground thickness H_g	0.5
Bend Length L_{bend1}, L_{bend2}	100
Bend Width W_{bend1}	47
Bend Width W_{bend2}	25
Distance $D_{signal1}$	56
Distance $D_{signal2}$	200

III. FREQUENCY-DOMAIN ANALYSIS

The structures have been characterized in the frequency domain by means of the S-parameters extracted by using two different commercial tools, Keysight Advanced Design System (ADS) [12] and CST Microwave Studio [13]. Specifically, the differential and common modes of the coupled lines have been studied, and the results are reported in Fig. 4 (transmission, S_{21}) and Fig. 5 (reflection, S_{11}). Note that the S-parameters refer to the characteristic impedance of differential (25 Ω) and common mode (100 Ω).

In general, the results shown in Fig.s 4 and 5 demonstrate a quite good agreement between the two models in terms of the reflection and transmission coefficients. Some discrepancies are found at higher frequencies. This behaviour is due to the fact, that the ADS model does not include the terminal pads. However, the absolute error is less than 1 dB for the transmission coefficients S_{21}, and less than 3 dB for the reflection coefficients S_{11}, therefore their impacts are negligible.

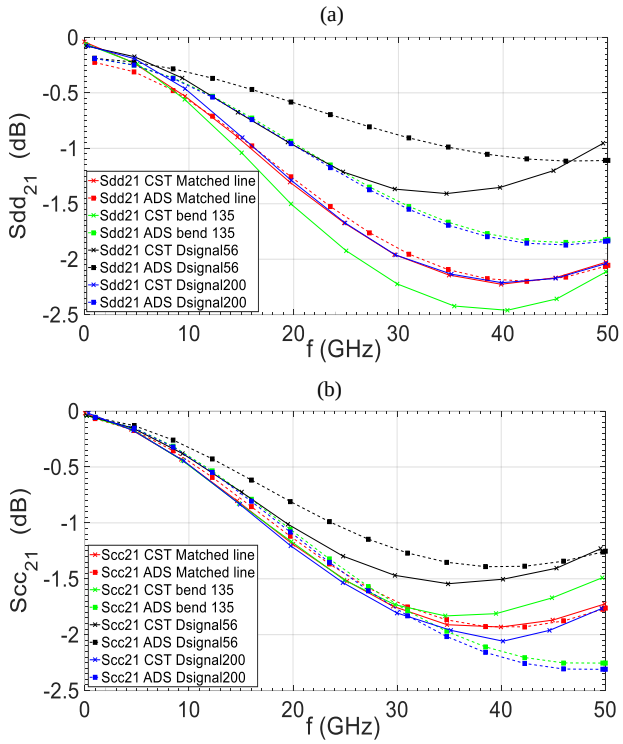

Fig. 4. Transmission coefficients of: (a) differential (Sdd_{21}) and (b) common (Scc_{21}) modes for the matched and bent TFMSL structures.

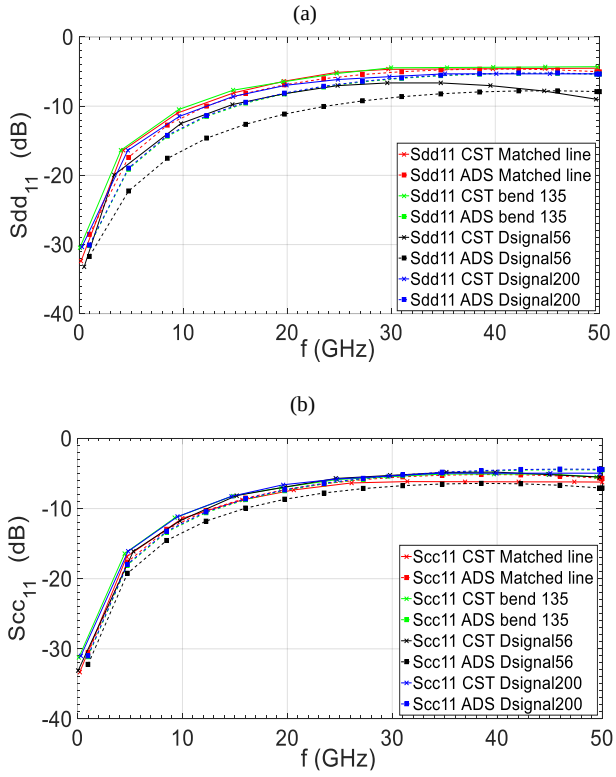

Fig. 5. Reflection coefficients of: (a) differential (Sdd_{11}) and (b) common (Scc_{11}) modes for the matched and bent TFMSL structures.

The analysis of the behavior of the S-parameters, reported in Fig. 6, allows an estimation of the insertion loss and the near-end and far-end crosstalk. Indeed, with the port-label convention of input ports 1 and 2 and output ports 3 and 4, the parameters S_{31} and S_{42} represent the insertion losses, S_{21} represents the near-end noise, and S_{41} is the far-end one. As the distance between two lines decreases from 200 µm to 56 µm (Fig. 3), the insertion loss S_{31} drops, whereas the corresponding far-end noise S_{41} increases. The further apart the signal traces, the smaller the difference between the odd and even-mode impedances and the lower near-end crosstalk (S_{21}).

A mode conversion analysis is carried out in Fig. 7. For instead of the balanced circuits, the impedance discontinuity is one of the features that affect the quality of the signal transmission. In addition, there is another source of distortion of the differential signal due to asymmetries in the coupled lines. Fig. 7 shows the comparison of symmetrical (two bent lines) and asymmetrical (one bent line) coupled TFMSL transmission lines. As expected, the mode conversion losses of the asymmetrical coupled TFMSLs are higher.

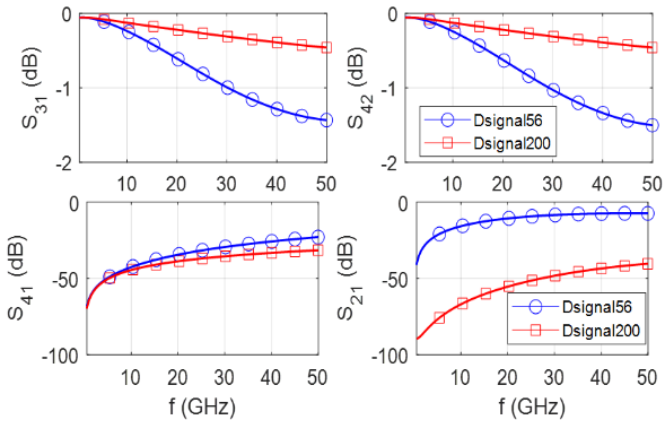

Fig. 6. Top view of lines with different coupling distances (D1 and D2), insertion loss, far-end and near-end crosstalks.

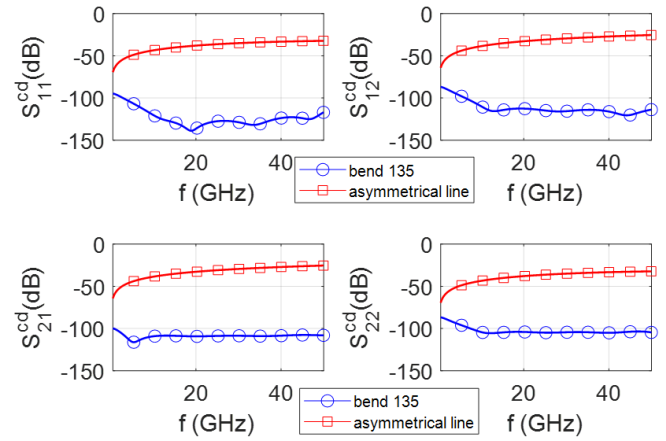

Fig. 7. Simulation comparison of a symmetric (circle) and an asymmetric (square) bent transmission line in terms of mode conversion.

IV. Signal Integrity Analysis

The different TFMSL structures characterized in the previous section were used in the high-speed link in Fig. 1 in a time-domain analysis to assess the SI performance in terms of eye-diagram parameters. To this end, equivalent circuit models based on both single-ended and differential signaling approaches have been implemented in the ADS simulator for all the studied structures. Here, we report the result of a single-ended configuration assuming one channel to be active and the second one to be at rest. The driver is modeled as a matched source of a voltage pulse train, with a bit-rate ranging from 1 to 100 Gbit/s. The receiver is instead modeled as a capacitive buffer of 0.1 pF capacitance. Examples of eye diagrams obtained for the matched line at different data rates (1, 30, and 50 Gbit/s) are reported in Fig.8.

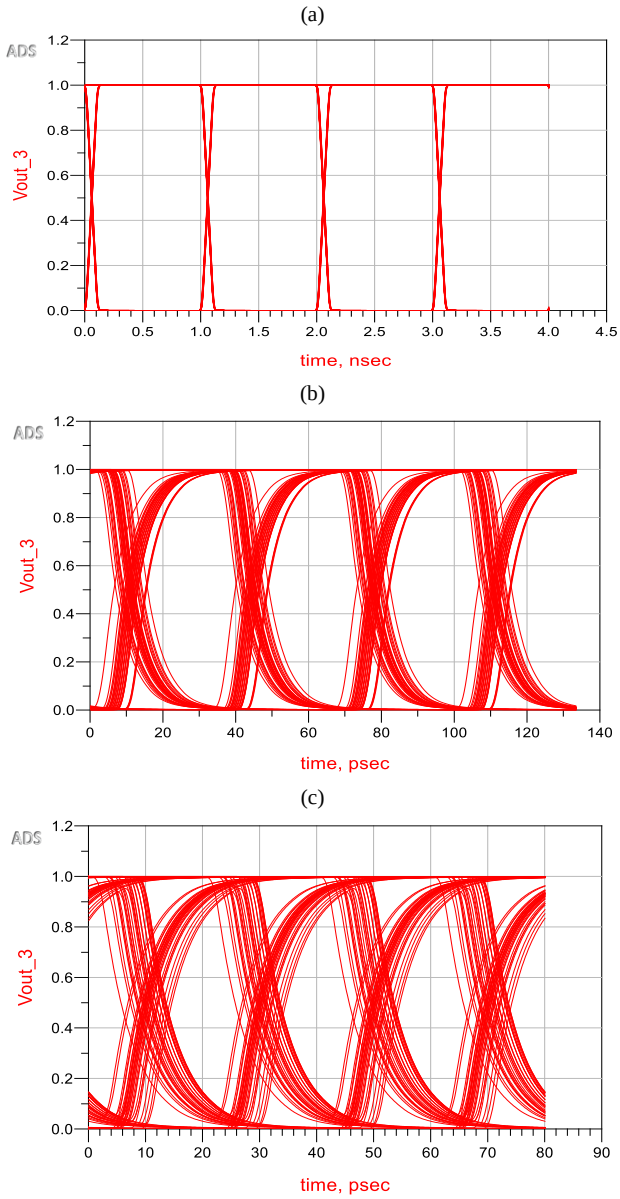

Fig. 8. Eye diagram analysis of parallel coupled TFMSL matched line at different data rates: (a) 1 Gbit/s, (b) 30 Gbit/s, and (c) 50 Gbit/s.

As expected, the quality of the eye diagram degrades as the bit rate increases. In particular, when the data rate is low (1Gbit/s), the performance is optimal, and the eye diagram seems ideal without any effect. However, as soon as the data

rate increases (30 and 50 Gbit/s), the characteristics of the eye diagrams worsen: the margin from noise reduces (eye closing) and the probability of timing errors in the high-speed digital link increases, as a consequence of the rise of jitter.

The metrics reported in Table II have been adopted to quantify the performance: the eye-opening, the ratio eye width/bit period, and the ratio jitter/bit period. The results related to the use of the 135° bent line are also reported in the same table. The eye-diagram metrics are generally worse for the bent line than the matched line. However, this is not always true; for instance, the percentage of the jitter at 50 Gbit/s is about 16% for the matched line and about 9% for the bend 135°.

A systematic eye-diagram analysis has been then carried out by considering all the structures in the data-rate range of interest. The results are the maps shown in Fig. 9, plotting the dependence of the eye-opening and the ratio jitter/ bit period. As expected, increasing the data rate leads to a general decrease in performance. However, these maps can provide helpful guidelines TFMSLs designers since a trade-off can be found between the two performance indexes, given a maximum data rate and a fixed geometry.

TABLE II. IMPACT OF THE DATA RATE ON EYE DIAGRAM MEASUREMENTS.

Metrics	Matched Line			Bend 135°		
	@1Gbit/s	@30Gbit/s	@50Gbit/s	@1Gbit/s	@30Gbit/s	@50Gbit/s
Eye-opening (V)	1	0.97	0.89	1	0.97	0.89
Eye width/Bit period	99%	60%	36.6%	99%	78%	48.8%
Jitter/Bit period	0%	5%	16.6%	0%	6.7%	9%

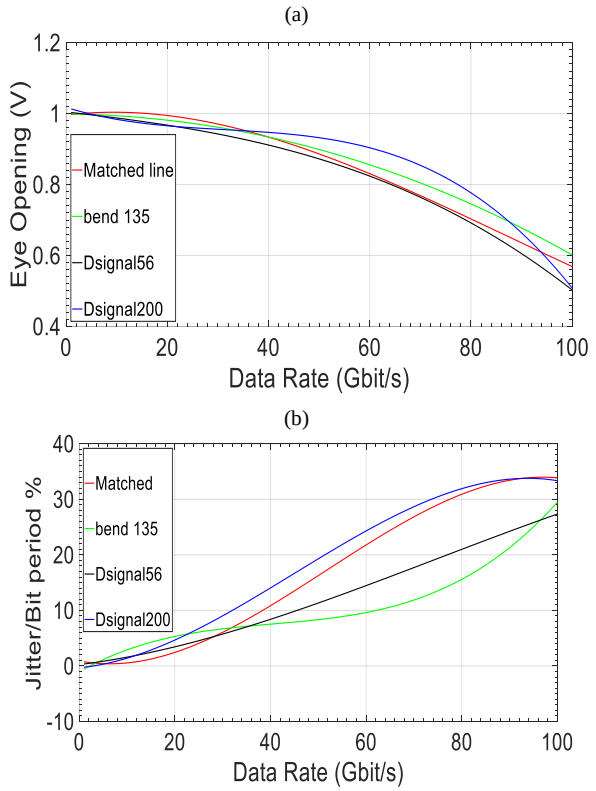

Fig. 9. Maps of the impact of data rate on the eye-opening and the ratio of jitter/bit period of the eye diagram.

V. CONCLUSIONS

This paper has analyzed the performance of a high-speed digital link based on the use of coupled thin-film microstrip lines, which are intended to operate under the conditions imposed by future communication standards (5G and beyond). In particular, the effect of geometric discontinuities, such as line bends, and the effect of varying the coupling distance have been studied. Transmission and reflection coefficients have been evaluated by means of the S-parameters analysis in the frequency domain. The relation between the distance between two lines, the insertion loss, and the crosstalk noise was demonstrated. Mode conversion between differential and common modes has also been studied, related to the asymmetries of the coupled lines. Furthermore, all the geometries considered have been studied in the time domain at the system level, highlighting the possibility of identifying trade-off optimized choices of data-rate values to be used for a given channel configuration. Future work will be devoted to studying the sensitivity of the system-level performance to the buffer capacitance.

ACKNOWLEDGMENT

The authors acknowledge the support by the Project RF Measurements for future communications applications (FutureCom) project (project number 20IND03). This project has received funding from the European Metrology Programme for Innovation and Research (EMPIR programme), co-financed by the Participating States, and from the European Union's Horizon 2020 research and innovation programme.

REFERENCES

[1] N. H. Huynh, W. Heinrich, K. Hirche, W. Scholz, M. Warth, and W. Ehrlinger, "Optimized flip-chip interconnect for 38 GHz thin-film microstrip multichip modules," in *Proc. of IEEE MTT-S International Microwave Symposium Digest*, vol. 1, pp. 69-72, Jun. 2000.

[2] A. Tessmann, *et al.*,"Submillimeter-wave amplifier circuits based on thin film microstrip line front-side technology," in *Proc. of 2015 IEEE Compound Semiconductor Integrated Circuit Symposium* (CSICS), IEEE, 2015, p. 1-4.

[3] C. Xu, *et al.*, "Design of a 40GHz Thin-Film Microstrip Sampler," in *Proc. of the 2018 IEEE International Conference on Microwave and Millimeter Wave Technology* (ICMMT), p. 1-3, 2018.

[4] Y. Zhang, *et al.*, "Loss analysis of thin film microstrip line with low loss at D band," *Journal of Lightwave Techn.*, vol.39, pp. 2421-2430, 2021.

[5] FutureCom Project, https://futurecom.unicas.it

[6] D. Allal *et al.*, "RF Measurements for Future Communication Applications: an Overview," in *2022 IEEE International Symposium on Measurements & Networking* (M&N), Padua, Italy, 2022, pp. 1-6.

[7] H. Kim, J. Kim, Y. Eo, "Broadband thin-film transmission-line characterization for accurate high-frequency measurements of on-wafer components," *IEEE Transactions on Microwave Theory and Techniques*, vol. 64, pp. 931-938, 2016.

[8] Z. Liang, Y. Xie, Q. Chen, "Improving the Signal Integrity, Impedance Control and Attenuation of the Thin Transmission Lines Printed on Flexible Substrates," in *Proc. of the 2020 IEEE 3rd International Conference on Electronics Technology (ICET)*, pp. 34-37, May 2020.

[9] S.C. Thierauf, High-speed circuit board signal integrity. *Artech House*, 2017.

[10] J.N. Tripathi, J. Narayan, R. Kumar Nagpal, and R. Malik. "Signal integrity and power integrity issues at system level." *IETE Technical Review 29.5*, pp. 365-371, 2012.

[11] J. Liu, B. Cai, J. Zhu, et al."Process research of high aspect ratio microstructure using SU-8 resist," *Microsyst. Technol.*, vol.10, pp. 265–268, 2004.

[12] Advanced Design System, www.keysight.com/PathWave Advanced Design System (ADS).

[13] CST Microwave Studio, https://www.cst.com.