A 100 GBd PAM-4 Optical Receiver using a SiGe BiCMOS Traveling-Wave EIC and a Silicon Photonic Ge Photodetector

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Abstract *Upcoming 800G and 1.6T transceivers require 200G/lane opto-electronic front-ends. Using a traveling-wave SiGe BiCMOS transimpedance amplifier (62GHz bandwidth, 6.9kOhm gain) assembled with a Silicon Photonic Ge photodetector, a 2.5pJ/bit optical receiver is demonstrated at a gross rate of 200Gbps PAM-4 using 5 taps of equalization. ©2023 The Authors*

Introduction

In order to process the ever-increasing amounts of datacenter traffic required for eg. artificial intelligence, cloud computing and big data applications, there is a growing need for high-speed data center interconnects. Standards for 400 Gbps links have been completed [1], but 800 Gbps and even 1.6 Tbps links are being envisioned [2]. For 800 Gbps/1.6 Tbps transceivers, 200 Gbps/lane links would allow to avoid doubling/quadrupling the number of links.

In [3], a traditional shunt-feedback transimpedance amplifier (TIA) implemented in SiGe BiCMOS is presented that has a 3 dB bandwidth (BW) of 92 GHz, but (electric-only) data experiments are limited to 120 Gbps NRZ. In [7-9], CMOS shunt-feedback TIAs are demonstrated up to 112 and 128 Gbps PAM-4. To achieve higher speeds, a promising option is to use traveling-wave amplifiers (TWA), as is done in [4] where a 46 GHz bandwidth is reported, but only data transmission experiments up to 40 Gbps NRZ are shown. According to the transimpedance limit [10], doubling the bandwidth of a shunt-feedback TIA within the same technology forces a four times lower transimpedance, increasing input referred noise. Additionally, a shunt-feedback input stage has a 4-pole transfer function (taking bondwire inductance into account), introducing severe intersymbol interference (ISI), whereas a TWA input stage has both a high bandwidth and a more gentle roll-off.

In this paper, we present an optical receiver based on a 55 nm SiGe BiCMOS linear traveling-wave TIA, assembled with short bondwires to a Ge photodetector in the iSiPP50G Silicon Photonic process. Electrical S-parameter measurements of this device show a 3 dB BW of up to 62 GHz, combined with a high transimpedance gain of 76.8 dBΩ (6.9 kΩ). A gross data rate of 200 Gbps PAM-4 is demonstrated with a bit error rate (BER) below the KP4 forward error correction (FEC) limit of 2.4E-4.

Traveling-wave transimpedance amplifier

The linear 4-channel traveling-wave TIA was designed and fabricated in 55 nm BiCMOS with a nominal f_T of 320 GHz. Fig. 1 shows the high-level block diagram of a single channel of this TIA. The photodiode cathode is connected to a

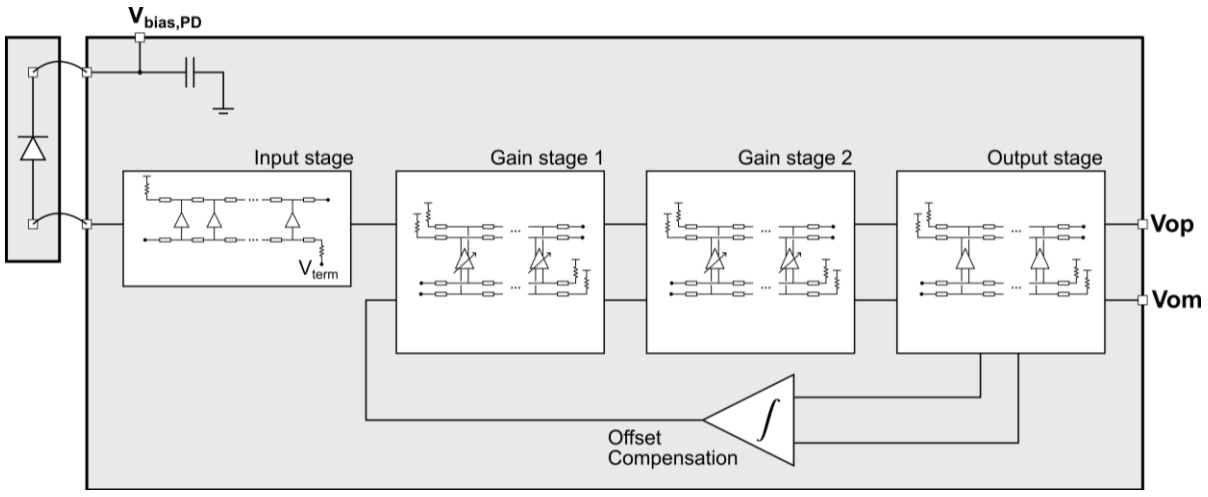

Fig. 1: Block diagram of a single TIA channel

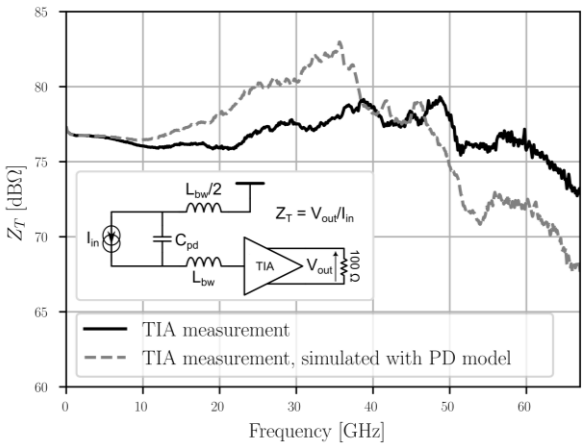

Fig. 2: Measured electrical frequency response of the TIA.

bias voltage that is decoupled on-chip. The single-ended input stage consists of 8 gain cells, after which two differential traveling-wave gain stages provide tunable gain and peaking. Finally, a linear output stage provides additional gain and is designed for a linear output swing of 650 mVpp at sub-5% total harmonic distortion (THD, at 1 GHz). These three final stages consist of 4 gain cells each. An error amplifier senses the DC-offset at the chip output and feeds this back to the first gain stage, canceling this offset.

Gain and peaking settings can be controlled using a low-speed digital serial interface. When only enabling a single channel, the chip draws 200 mA from a single 2.5 V supply (500 mW power). The dimensions of the four-channel chip are 3 mm by 1.5 mm, with each channel measuring 750 µm by 1.5 mm.

Electrical frequency response

To evaluate the electrical response of the chip, a die was assembled on a PCB with wirebond connections for the supply and control lines. The input was contacted with a GSG RF probe and the output with a GSSG RF probe. A PNA-X N5247B vector network analyzer (VNA) was used to measure 3-port S-parameters, and calibration was performed up to the probe tips.

The single-ended to differential transimpedance gain is derived from the S-parameters:

$$Z_T = \frac{S_{21} - S_{31}}{1 - S_{11}} \cdot Z_0 \qquad (1)$$

with port 1 at the input and $Z_0 = 50\ \Omega$.

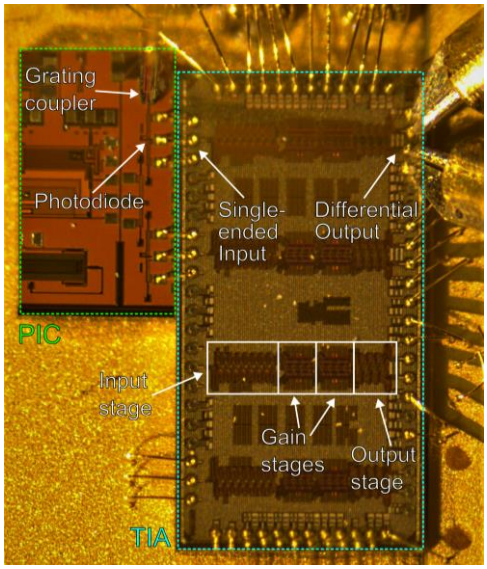

Fig. 3: TIA and PD wirebonded to a test PCB.

This is plotted in Fig. 2 for the maximal gain setting and for all peaking settings at their maximum. The transimpedance gain measured at 1 GHz is 76.8 dBΩ (or 6.9 kΩ) and the 3 dB BW is 62 GHz. Adding an electrical model of the Ge photodiode with bondwires (2 at the cathode, which helps to reduce the total inductance), as depicted in the inset of Fig. 2 (C_{pd} = 50 fF and L_{bw} = 200 pH), lowers the 3 dB BW to 50 GHz.

Opto-electrical time domain measurements

In order to demonstrate the performance of this TIA as a direct-detection receiver, the experimental setup shown in Fig. 4 was used. An arbitrary waveform generator (AWG, M8199A) outputs a PAM-4 signal based on a PRBS13 bitstream. A remote head (M8158A) amplifies this signal to drive a Mach-Zehnder modulator (MZM), which is biased at the quadrature point. A laser generates the optical carrier at 1585 nm (selected for minimal coupling loss to the PIC). An erbium-doped fiber amplifier (EDFA) and a variable optical attenuator (VOA) were used to control the optical power received at the photodiode (PD). When using the PIC with the Ge photodetector, a polarization controller was used to align the polarization to the TE axis of the PIC. By using a 70 GHz photodiode (XPDV3120R) as a reference receiver (directly attached to the remote sampling heads), the high-frequency losses of the transmitter were de-embedded.

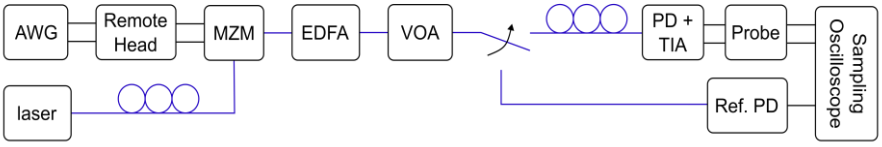

Fig. 4: Experimental setup for opto-electrical time domain measurements

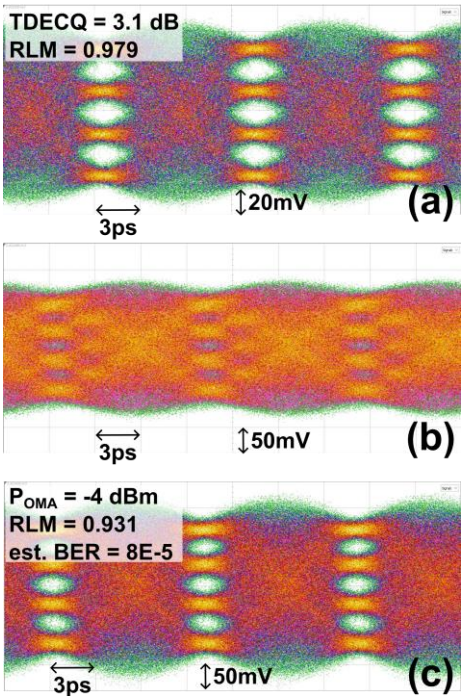

Fig. 5: Measured 100GBd PAM-4 eye diagrams of (a) the reference receiver and (b) the proposed TIA. In (c), a 5-tap equalizer is applied to the TIA output signal.

The TIA chip is wirebonded to a silicon photonic integrated circuit, containing a grating coupler and a Ge PD from imec's iSiPP50G platform (see Fig. 3). The grating coupler incurs a loss of about 3 dB and the photodiode responsivity is 0.8 A/W. The differential output pads of the TIA chip are probed by a GSSG probe to which the remote sampling heads (N1046A) are connected using a short cable.

Fig. 5a shows the eye diagram measured at the output of the reference receiver, when a 100 GBd PAM-4 signal with 8 dBm optical modulation amplitude (OMA) and an extinction ratio (ER) of 3.4 dB is applied. The AWG output pulse is shaped according to a raised cosine with $\alpha = 0.6$. The TDECQ of this signal is 3.1 dB and the RLM is measured at 0.979. The BER is estimated by fitting Gaussian probability distributions to the sampled signal points, and amounts to 2E-8. The eye diagram of Fig. 5b is obtained at the output of the presented receiver when an OMA power of -4 dBm (after the grating coupler) is applied. For this, the gain has been lowered in both gain stages and the output stage to 56.9 dBΩ. The eye is clearly closed, but with an on-scope 5-tap symbol-spaced FFE (Fig. 5c), the BER is improved from 2E-2 to 8E-5, below the limit of 2.4E-4 for KP-4 FEC. The RLM is only degraded to 0.931, demonstrating the linear operation of this TIA.

In Tab. 1, the measured performance of the presented receiver is compared against other state-of-the-art receivers. Our receiver has the highest transimpedance gain. In [3], a much higher BW and baud rate is shown, but only for NRZ modulation. Our 100 GBd PAM-4 experiments showcase a bit rate of 200 Gbps. Besides, the TIA demonstrated in [3] only consists of a single stage. In [6] the BW is also higher than in this work, but the bit rate is limited to 100 Gbps. The closest competitor in terms of bit rate achieves 160 Gbps PAM-4 [5] but requires a 51-tap FFE. For our demonstration, a simple on-scope 5-tap FFE sufficed. Also note that the time-domain measurements in [3,6,7,8] were performed fully electronically, without photodiode. With a power consumption of 500 mW, our chip achieves a power efficiency of 2.5 pJ/bit. This is better than the previously reported BiCMOS traveling-wave TIA [4].

Conclusions

This work presents a SiGe BiCMOS traveling-wave TIA with a bandwidth of up to 62 GHz and a transimpedance gain up to 76.8 dBΩ. After co-integration with a silicon photonic PD, a gross data rate of 200 Gbps PAM-4 is demonstrated, at an efficiency of 2.5 pJ/bit. For this, only a simple 5-tap FFE is required to open up the eye diagram.

Acknowledgements

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Tab. 1: Comparison to the state of the art.

	BW [GHz]	Zt [dBΩ]	Datarate [Gbps]	Efficiency [pJ/bit]	Integrated with PD?	TIA topology	Technology
This	62	76.8	200 (PAM-4)[c]	2.5	Yes	Traveling-wave	55nm BiCMOS
[3]	92	47[a]	120 (NRZ)	0.4	No	Shunt feedback	55nm BiCMOS
[4]	46	47	40 (NRZ)	7.5	Yes	Traveling-wave	180nm BiCMOS
[5]	38[e]	N/A	160 (PAM-4)[d]	1.2	Yes	N/A	N/A
[6]	65[e]	71	100 (PAM-4)	3.45	No	Shunt feedback	130nm BiCMOS
[7]	60[e]	65	112 (PAM-4)[b]	0.96	No	Shunt feedback	28nm CMOS
[8]	45.5	59.3	128 (PAM-4)[c]	0.0875	No	Shunt feedback	22nm FinFET
[9]	32	63	112 (PAM-4)	0.6875	Yes	Shunt feedback	16nm FinFET
[a]Calculated from S21; [b]Using 3-tap FFE; [c]Using 5-tap FFE; [d]Using 51-tap FFE; [e]Including PD (model)							

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