A SiGe High Gain and Highly Linear F-Band Single-Balanced Subharmonic Mixer

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***Abstract*—A compact, broadband, high gain, second-order active down-converter subharmonic mixer is demonstrated using a 130-nm SiGe BiCMOS technology. The mixer adopts a bottom-LO Gilbert topology, on-chip RF and LO baluns and two emitter-follower buffers to realize a high gain wideband operation in both RF and IF frequencies. The measured performance exhibits a flat conversion gain (CG) of about 11 dB from 90 to 130 GHz with an average LO power of +3 dBm and high 2LO-RF isolation better than 60 dB. The mixer shows an input 1-dB compression point of -16 dBm consuming a dc power of only 40 mW. The chip dimension is 0.4 mm^2, including probing pads. It demonstrates also up to 12 GHz 3-dB IF bandwidth, which to the authors' knowledge, is the highest obtained among active mixers operating above 100 GHz**

***Index Terms*—SiGe MMICs, millimeter-wave, subharmonic mixer (SHM), conversion gain.**

I. Introduction

SUBHARMONIC mixer (SHM) is an attractive candidate for frequency conversion in micro-wave and millimeter-wave transceivers. It requires only a fraction of the local oscillator (LO) frequency compared to a fundamental mixer and increases the LO-to-RF isolation significantly. Unfortunately, most of the high frequency SHMs above 100 GHz have conversion loss which imposes rigorous noise figure and gain requirements on low noise amplifier and following building blocks of receiver chain [1, 2, 4]. On the other hand, to realize a high gain amplifier at the RF or IF side, usually three to five stages are utilized, where it burdens the power budget of a low power system. Therefore, implementing a millimeter-wave down-converter SHM is challenging with respect to conversion gain, bandwidth, noise figure and linearity requirements.

Recently, several efforts have been done in literature to design high gain SHMs. In [3], a transformer-based gm-boosting Top-LO Gilbert SHM is presented operating at 79 GHz, where a conversion gain of 1.6 dB with a LO power of -5 dBm is achieved. This technique boosts the RF transconductance without additional power consumption. However, it is difficult to achieve a large gain for input frequencies higher than 90 GHz due to the additional loss of transformer network. In [4, 5], a two-stage subharmonically pumped transconducance mixer is introduced that reaches to maximum 6 dB and -1 dB conversion gain at V-band and D-band using a 5 dBm and -1 dBm LO power, respectively. This type of mixer features broadband operation. Nonetheless, it suffers from conversion loss and requires an optimal base bias along with a large driving LO power. Therefore, both mixers employ a power hungry IF buffer which correspondingly leads to 120 mW and 262 mW total power consumption. Another SHM topology is a modified Gilbert cell based on two stacked switching quads, which is used in [6] for 122 GHz. This topology shows better conversion gain compared to a Gilbert cell configuration with parallel transistor stacks. However, as the frequency goes up, the maximum conversion gain of the mixer occurs by non-quadrature LO signals. Hence, a novel hybrid with an arbitrary phase shift is needed in order to provide an optimum LO phase distribution. Furthermore, due to the several stacked transistors, a larger supply voltage is required to avoid the compression of the output voltage amplitude, which inevitably influences the power consumption of whole circuit.

This letter reports a high gain wideband bottom-LO Gilbert SHM that is designed to operate at F-band frequency. The mixer is implemented in a single balanced arrangement, driven by a differential LO- and RF- scheme. It also generate anti-phase IF signals which are broadly matched at the output to 50 Ω through the emitter followers.

II. Circuit Analysis and Design

The subhramonically pumped bottom-LO Gilbert mixer was first demonstrated at 930 MHz [7] and is well described in [8]. Unlike a conventional topology which implements the mixer function by a transconductor followed by current commutating switching; this scheme achieves the same functionality by the switched transconductors. One of the main advantages of bottom-LO topology is the high LO-to-RF and high LO-to-IF isolation. This is because the LO signal appears in common-mode at both RF and IF ports. Furthermore, any LO leakage to the RF port is mixed with the second harmonic of LO frequency due to subharmonic operation, which is back to the same LO frequency and is well filtered out at the next stage. Therefore, this topology is utilized here to design a full F-Band SHM for the first time.

Fig. 1 depicts the simplified schematic of the proposed wideband single-balanced SHM along with a fabricated chip photo. The circuit consists of a push-push frequency doubler LO-stage (Q1s/Q2s), a differential RF transconductance stage (Q1/Q2), two emitter-follower buffer-stage (Q1b/Q2b), and two on-chip Marchand baluns at RF and LO ports. The LO-stage acts as a frequency doubler to convert input differential

LO voltage into current. It generates the second harmonic of LO and controls transconductances of the RF-stage efficiently at twice the LO frequency. Consequently, two out-of-phase subharmonic IF components (f_{IF}=f_{RF}-2f_{LO}). are produced and conveyed to the buffer-stage through resistive loads. The output buffer provides a 50 Ω matching over a broad bandwidth and also forms as a low-pass filter to enhance the RF-to-IF isolation at the output ports.

Both mixer and buffer stage are biased with current sources, regulated by a reference current. Subsequently, a high current or a low current can be injected to the circuit, which accordingly offers a highly linear or a low noise operation. Regarding transistor modeling, two series resistors (R1/R2) are also placed at the collector of output current sources to prevent transistor damages under high current levels.

In order to achieve a wideband operation, a transmission-line-based Marchand structure with broadside coupled lines is realized at both RF and LO ports. This design was introduced in [9]. A further improvement is done by removing the ground layer (M4) under the signal lines resulting to more compact layout and lower insertion loss. Fig. 2 exhibits the simulated performance of baluns in terms of phase and amplitude imbalance, while the minimum loss is -1.3 dB and -2 dB, for RF and LO signals, respectively.

The high frequency RF signal is applied through a shunt spiral inductor (L1/L2) accompanied by a series line (TL_1/TL_2) to transform the low input impedance of transistor base to a higher value [2]. To do this, custom inductors are designed with one-turn symmetric structure on M6, where the simulated value of each inductor is about 20 pH with the maximum quality factor of 12.9 at 173 GHz, and the self-resonance frequency of 355 GHz.

To increase LO swing across the emitter terminal of RF transistors, a tuning-out series line (TL_3) is adopted between RF and LO stages, implementing a π-network [10]. This network provides a higher conversion gain at lower LO powers and slightly enhances the RF bandwidth of the mixer. Finally, the IF loads incorporate 150 Ω resistors together with emitter-followers, to provide broadband IF response.

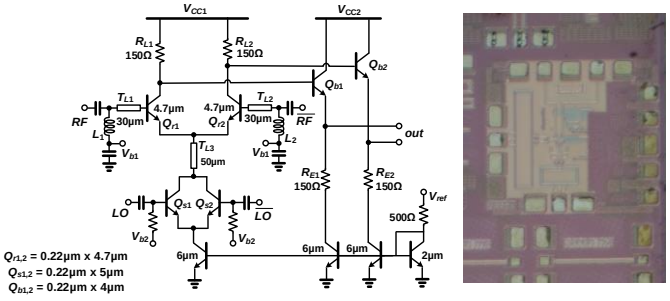

Fig. 1. (a) Circuit schematic of the single-balanced (SB) Bottom-LO SHM (b) chip photo (size: 600 μm × 670 μm including pads). write components

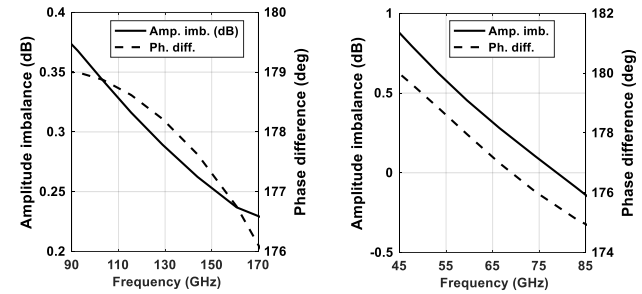

Fig. 2. Simulated amplitude imbalance and phase difference of (a) RF (b) LO Marchand baluns

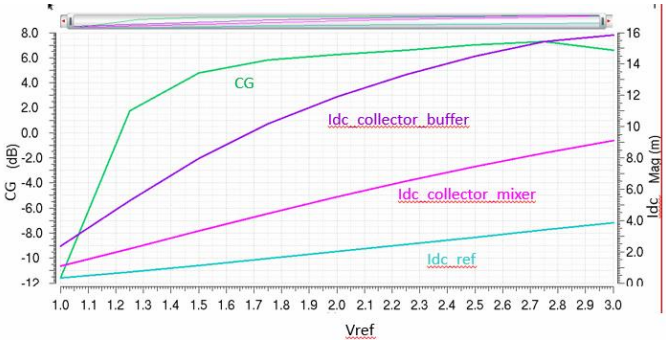

Fig. 3. Measured conversion gain, output P1dB and simulated NF ?? versus collector current of mixing stage (f_{LO}=65 GHz, f_{RF}=131 GHz). (I will replace with meaurement)

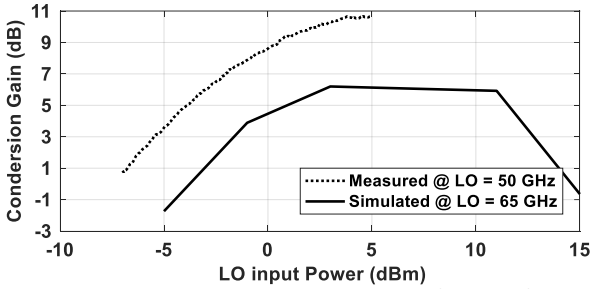

Fig. 4. Measured and simulated conversion gain as a function of LO-power with a fixed LO and IF frequency of 50 GHz and 3 GHz, respectively.

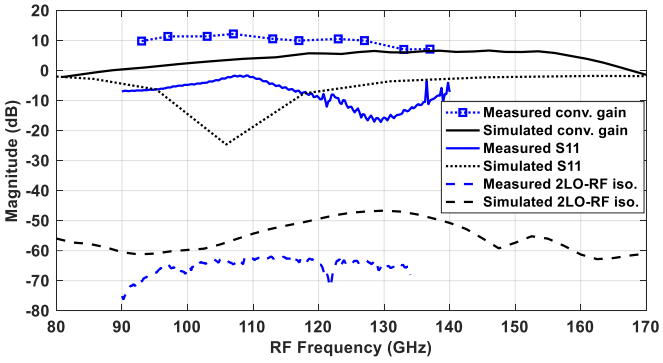

Fig. 5. Measured and simulated conversion gain and 2LO-to-RF isolation versus RF frequency.

III. Mixer Measurement

The presented F-Band SHM is fabricated in 0.13 μm SiGe BiCMOS process featuring high speed npn HBTs with maximum f_t/f_{max} of 250 GHz/370 GHz and BV_{CEO}= 1.5 V The chip size is 600×670 μm^2, including all probing pads. To characterize the mixer performance, on-wafer measurements

TABLE I. PERFORMANCE SUMMARY OF SHMS

Ref.	Process	RF (GHz)	×N	CG (dB)	IF BW (GHz)	IP_{1dB} (dBm)	OP_{1dB} (dBm)	2LO-RF Iso. (dB)	P_{LO} (dBm)	P_{DC} (mW)	Chip size (mm^2)	Topology
[1]	90nm CMOS	30-100	2	-1.5		-10.4	-12	38	10	58	0.35	level
[2]	32 nm SOI CMOS++	158-182	2	+8$	6	NA	NA		4	74	0.75	Passive resistive
[3]	65 nm CMOS	75-81	2	1.6		-16.2	-15.6		-5	12	0.31	gilbert
[4]	250 nm InP DHBT	110-170	2	-1	5	NA	NA		-1	262	0.825	trans
[5]	250 nm InP DHBT	55-67	2	6	NA	-2	+4		5	120	0.63	trans
[6]	130nm SiGe:C	125-129	2	4	NA	NA	NA		9	89.1	NA	Stack Gilbert
This Work	**130nm SiGe**	**90-140**	**2**	**12**	**12**	**-16**	**-4**	**60**	**<6**	**40**	**0.4**	**Bottom with buffer**

++ I/O ...

are carried out using an Agilent N5247A PNA-X microwave network analyzer from 10 MHz to 67 GHz and N5262BW08 WR8 based frequency converter to extend the RF frequency range from 90-140-GHz. The whole chip consumes about 40 mW dc power, where only 12 mW is drawn by the mixer stage and 28 mW and 3 mW is dissipated by the buffers and reference current source, respectively. Fig. 3 shows the measured conversion gain and output 1-dB compression point (OP_1dB) as a function of collector current in the mixing stage, while the LO-power is fixed at +3 dBm.

The variation of mixer conversion gain versus LO power is shown in Fig. 4. It demonstrates a positive gain up to an LO input power of -6 dBm. The LO is swept from 44 to 67 GHz while its input power is slightly changed from 6 to 3 dBm. The SHM can cover a RF frequency of full F-Band with a conversion gain of +8.4 to +12 dB due to the LO power drop at higher frequencies. The 2LO-to-RF isolation is also shown in Fig. 5, which is greater than 60 dB. The 3-dB bandwidth extends over 40 GHz from 90 to 135 GHz. The measured IF response is shown in Fig. 6. The results indicate a flat IF bandwidth from 0.1 to 12 GHz using OFF-chip DC-blocking capacitors at the output IF port, which helps to cover the lower frequencies up to 100 MHz. This is the widest 3-dB IF bandwidth among active mixers operating above 100 GHz. Fig. 6 describes the output power at 3 GHz versus input power at 100 GHz. As is seen, the circuit can provide up to -16 dBm input power at a 1-dB compression point, while the total power consumption is only 40 mW. Table I compares the performance summary of the presented SHM and some other published results in a similar frequency range. It can be seen that our SHM achieves state-of-the-art conversion gain, and relatively high output power, as well as a broadband operation.

The simulated noise figure of the mixer is below 16 dB over the entire IF bandwidth which is good enough to be preceded by an LNA with a moderate noise figure.

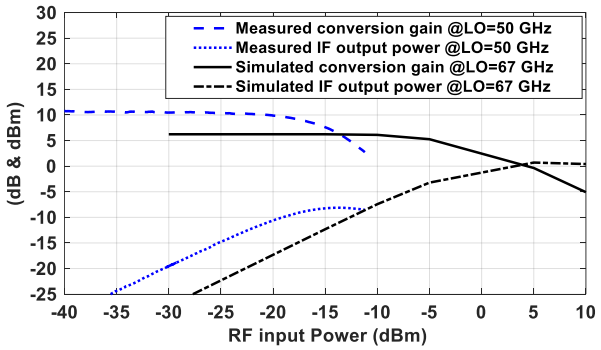

Fig. 6. Measured IF output power as a function of the RF input power at a fixed RF and IF frequency of 103 GHz and 3 GHz, respectively. several vm??

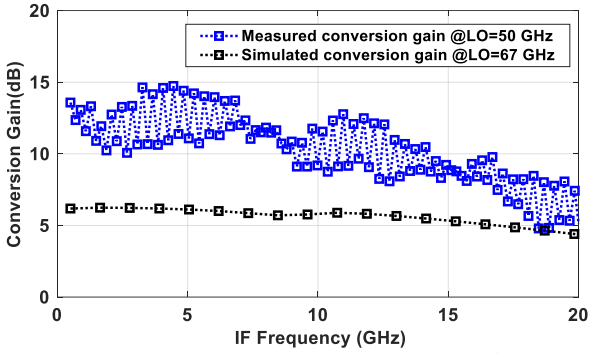

Fig. 7. Measured and simulated conversion gain versus IF frequency. The LO is fixed at 50 GHz and RF is swept from 100 to 120 GHz.

IV. CONCLUSION

In this letter, design and characterization of a SiGe F-band subharmonic down-converter mixer is presented. This mixer utilizes a SB bottom-LO Gilbert topology and demonstrates a record conversion gain of above 10 dB from 90 to 130 GHz. The presented results in Table I shows a state-of-art IF bandwidth. In addition, the SHM has a good linearity, port to port isolation and a relatively small chip size.

V. ACKNOWLEDGMENT

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