A Direct Carrier I/Q Modulator for High-Speed Communication at D-Band Using 130 nm SiGe BiCMOS Technology

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***Abstract*— This paper presents a 110-170 GHz direct conversion I/Q modulator realized in 130 nm SiGe BiCMOS technology with f_t/f_{max} values of 250 GHz/ 370 GHz. The design is based on double-balanced Gilbert mixer cells with on-chip quadrature LO phase shifter and RF balun. In single-sideband operation, the modulator exhibits up to 9.5 dB conversion gain and has measured 3 dB IF bandwidth of 12 GHz. The measured image rejection ratio and LO to RF isolation are as high as 20 dB and 31 dB respectively. Measured input P_{1dB} is -17 dBm at 127 GHz output. The DC power consumption is 53 mW. The active chip area is 620 µm× 480 µm including the RF and LO baluns. The circuit is capable of transmitting more than 12 Gbit/s QPSK signal.**

***Index Terms*— Gilbert cell mixer, millimeter wave, 5G, I/Q modulator, SiGe BiCMOS, D-band.**

I. Introduction

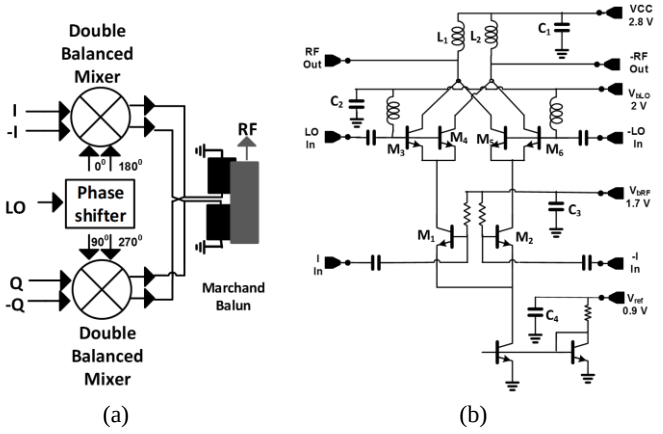
After 60 GHz ISM-band and the E-band (71-76 and 81-86 GHz), the unoccupied frequency band at 110-170 GHz (D-band) is attractive for compact, lightweight point-to-point application such as backhaul links for 5G mobile networks [1], [2]. This increased available bandwidth and relatively low atmospheric path attenuation below 1 dB/km from 120 GHz to 160 GHz can be used for multiple gigabit communication with km range [3]-[6]. The 141–148.5 GHz frequency band is allocated by the Federal Communication Commission (FCC) for fixed and mobile communication [7]. An ISM bandwidth of 1 GHz around 122.5 GHz will be mainly used for industrial, medical and security sensors in Europe and US [8].

At millimeter wave (mm-wave), there is great potential for improved performance and higher integration levels in both III-V and silicon technologies [9], [10]. Due to its low cost at volume, high reliability and high integration with dense CMOS based digital processor, SiGe BiCMOS technologies is more in favor of the commercial application such as high-speed communication, automotive radars, sensing and imaging [11], [12]. This technology has previously been used to design transmitter and receiver chips in D-band [3]-[5], [6]. However, the main challenges for the designs beyond 100 GHz are the increased parasitic effect, device model inaccuracy, and limited transistor performance.

For increased capacity and spectrum efficiency, the front end systems need to able to support complex modulations. The I/Q modulator and demodulator are key components in modern wireless transmitter and receiver systems. The modulation/demodulation directly at the carrier frequency can reduce complexity of these systems. This paper presents a direct conversion I/Q up-converting mixer/modulator at the D-band which can be used both in homodyne and heterodyne architectures. This design requires modest LO driven power which can be generated by frequency multiplier circuits in the same technology. The paper starts with a brief description of the technology and topology of the design in Sec. II, followed by presentation of the measurement results in Sec. III. The performance is summarized and compared with previous published results in Sec. IV.

II. Technology And Circuit Design

The I/Q modulator is designed in an 130 nm SiGe BiCMOS process from Infineon (B11HFC). The process features high speed npn HBTs with maximum f_t/f_{max} of 250 GHz/370 GHz and BV_{CEO}= 1.5 V [13]. The block diagram of the I/Q modulator is shown in Fig. 1(a). It consists of a LO phase shifter, broadside RF Marchand balun and two direct up-conversion mixers. Both mixers structured as double balanced Gilbert cells . The double balanced topology is used to improve port isolation and to increase the frequency conversion efficiency [14]. These mixers are fed with orthogonal carriers generated by an on-chip differential quadrature coupler. The LO phase shifter consists of two 90^0 broadside couplers and one Marchand balun. This 90^0 coupler is a differential implementation of the well-known quarter-wavelength backward coupler [15], [16]. Fig. 1(b) shows the schematic of the one double balanced mixer cell including the current mirrors, IF transconductance stage, LO switch stage, and RF output balun. The input baseband signals are converted to current signals by the transconductance stage (M_1-M_2) and



(a) (b)

Fig. 1. (a) Block diagrams of the I/Q modulator. (b) Schematic of the one double balanced up-conversion mixer.

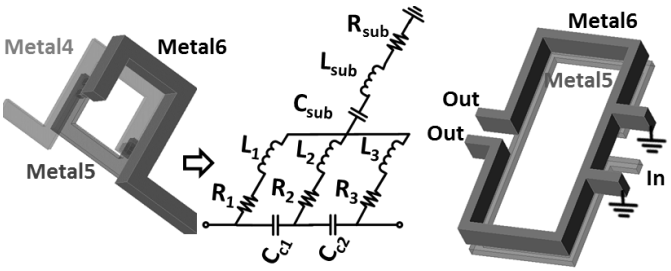


Fig. 2. (a) 3-D layout of a multilayer on-chip inductor. (b) Lumped-element model of inductor. (b) 3-D layout of the RF and LO balun.

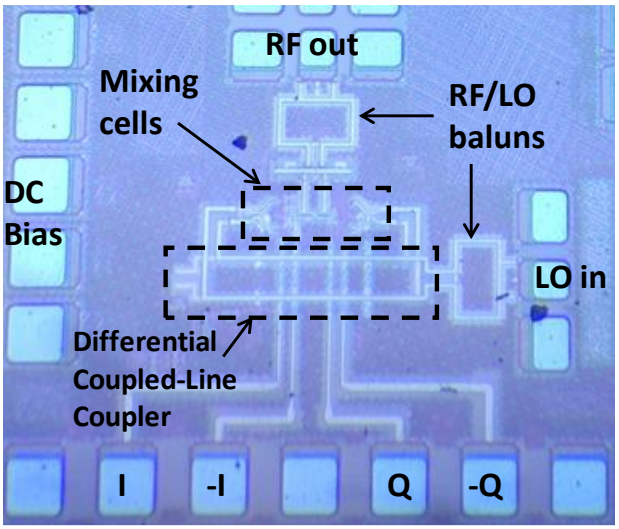


Fig. 3. Chip photograph of the I/Q modulator with active chip size of 620 µm× 480 µm including the RF/LO baluns and the LO hybrid.

are fed to the differential pair (M_3-M_6) which are also called switching quads. The up-converted RF differential output currents are added and passed through a common inductive load (L_1-L_2). These two outputs are then connected to a balun for differential to single-ended output conversion. For optimal performance, the switching mixer transistors are chosen to be 2 µm long and the transconductance transistors are accordingly scaled to be 4 µm long. The operating condition is set by the reference current which is mirrored to the two mixer cells. Baseband ports are DC coupled as blocking capacitors for such frequencies may occupy very large chip area. The collector and the base voltages of the switches are applied to the virtual RF grounds of the load and the LO matching network respectively. Decoupling capacitors (C_1, C_2, C_3, C_4) are incorporated to avoid potential odd-mode instability of the circuit. Metal2 is used as a ground layers and M3-M6 copper layers are used for interconnections as well as design of passive structures. Most of the passive components are EM-

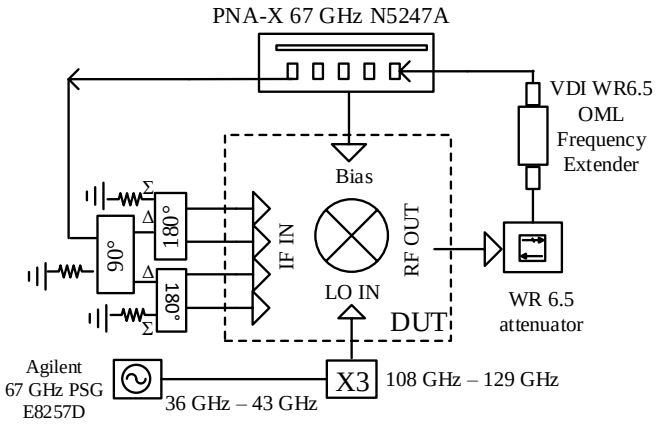


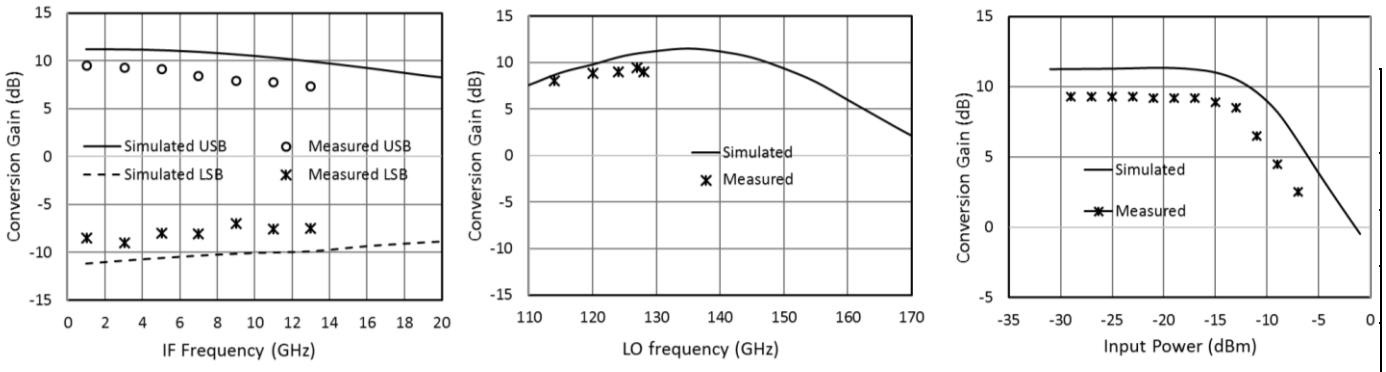
Fig. 4. Illustration of the CW measurement setup of I/Q modulator.

simulated in HFSS and then imported into the circuit design environment for co-simulation. Fig. 2(a) shows the geometry of a two-turn on-chip inductor and its extracted equivalent model in Fig. 2(b). L_1, R_1, L_2, R_2 and L_3, R_3 are the effective inductance and resistance of each turn in the M4, M5 and M6 layers, respectively, and C_{c1} and C_{c2} are used to model the capacitive coupling between the turns. C_{sub}, L_{sub} and R_{sub} represent the lumped capacitance, inductance, and resistance between metal segments and the M2 ground plane, respectively. A 3-D view of balun is shown in Fig. 2(c). The balun has simulated 0.6 dB amplitude and 5^0 phase imbalance between the two output ports in D-band. The reflection coefficients on input and output ports are simulated to be lower than 18 dB. The chip photograph is shown in Fig. 3. In order to minimize any unwanted parasitic effects and to maintain the amplitude and phase balance of the modulator, the signal paths of the RF, LO, and IF were laid as symmetric as possible. The LO coupler and matching networks are compact and symmetrically laid out around the mixer cells. Any imbalance is critical to the LO isolation and image suppression of the modulator.

III. Measurement Setup And Circuit Characterization

On-wafer probe measurements have been performed to characterize the I/Q modulator as a side band up-converting mixer using WR6.5 waveguide GSG-probes for the LO and RF ports and GSSGSSG for the balanced IF ports. The mixer collector bias is +2.8 V and takes 16 mA current. The LO and IF base voltages are +2 V and +1.7 V as shown in Fig. 1. For demonstration of single side-band operation, a CW signal with balanced four phases is applied to the differential I and Q ports. The LO signal is provided from an Agilent 8257D synthesizer together with an in-house developed x3 frequency multiplier module. The LO signal power going into the chip (measured with an Erikson power meter) after considering probe loss is between 5 dBm and 7 dBm.

Details of the measurement setup are shown in Fig. 4. A Keysight PNA-X N5247A network analyzer with VDI WR6.5



(a) (b) (c)

Fig. 5. (a) Conversion gain versus IF frequency at 126 GHz LO. (b) Conversion gain versus LO frequency at 1 GHz IF. (c) Conversion gain versus input power at 1 GHz IF and 126 GHz LO.

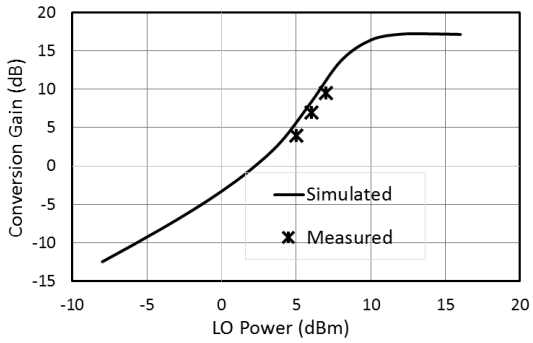


Fig. 6. Measured and simulated conversion gain versus LO power at 126 GHz and an input IF of 1 GHz.

(110-170 GHz) frequency extension module at RF port is used in the measurement. The loss accounted for the measurement setup was calibrated and de-embedded in the presented data.

The measured upper (USB) and lower (LSB) sideband conversion gains versus IF frequency at 126 GHz LO are shown in Fig. 5(a). The input signal power to both the I and Q ports are -26 dBm. The image rejection is approximately 20 dB and exhibits up to 9.5 dB conversion gain. The 3 dB IF bandwidth of the chip is measured to be 12 GHz which is in good agreement to the simulation results. Limited by the available intrument, the driven LO power from the source at the frequencies higher than 130 GHz were below 1 dBm, which was insufficient to drive the modulator. Fig. 5(b) shows the simulated and measured USB conversion gain versus LO frequency with an IF frequency of 1 GHz. The simulation and measurement are performed at 7 dBm LO power to modulator. As can be seen the 3 dB RF bandwidth is 30 GHz from 120 GHz to 150 GHz. Fig. 5(c) shows the linearity of the mixer at 127 GHz RF output and input at 1 GHz. The input P_{1dB} is measured to be -17 dB. The 126 GHz LO power at the output port of mixer is measured to be -24 dBm which provides an LO to RF port isolation of 31 dB. Fig. 6 shows the simulated and measured conversion gain versus LO power to mixer for input 1 GHz and LO at 126 GHz.

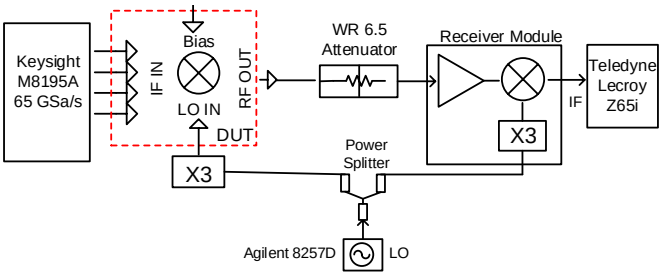
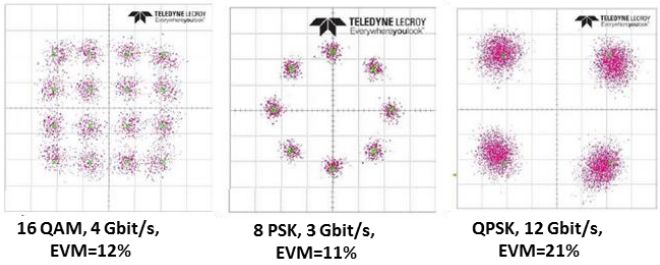


Fig. 7. Experimental setup for data transmission test.



(a) (b) (c)

Fig. 8. Received signal constellation diagram of (a) 4 Gbit/s 16QAM, (b) 3 Gbit/s 8PSK, (c) 12 Gbit/s QPSK.

It can be seen that mixer conversion gain increases with LO power and saturates at 16 dB in simulation.

Data transmission is verified with the experimental setup as shown in Fig. 7. The modulator MMIC is probed on-wafer and an in-house developed D-band receiver is used at the receiver side [6]. The LO sources of the modulator and receiver are synchronized. An arbitrary Waveform Generator (Keysight M8195A 65 GSa/s) is used to generate high order QAM signals centered at 5 GHz IF. The generated signal is fed to the modulator which up-converts the IF input signal to RF at 131 GHz. A variable attenuator is inserted between the modulator and receiver in order to attenuate the RF signal to the receiver preventing the receiver to saturate. The receiver down-converts the

incoming RF signal to IF before sampling by a real-time oscilloscope (Lecroy) with a fixed 80-GSamples/s sampling rate. Lecroy VSA software is used for demodulation and constellation analysis.

Fig. 8(a-c) shows constellation diagram for 16-QAM, 8-PSK and QPSK modulation, respectively. A 12 Gbit/s QPSK signal was transmitted with total EVM of 21 % from the modulator to the receiver. The maximum rate is limited by the low available LO power to the modulator and receiver module. It is possible that the modulator itself can operate with even higher bit rates as well.

IV. Performance Summary And Conclusion

A D-band direct I/Q modulator is reported in this paper. The design is fabricated using a commercial 130 nm SiGe BiCMOS process and verified experimentally for wideband communication. The active area of the chip including the RF/LO baluns and the LO hybrid is 620 µm× 480 µm. The chip consumes 53 mW DC power. Table I shows a brief performance summary of the presented modulator with some published results in similar frequency range. It can nevertheless be seen that the presented design demonstrates outstanding performance in terms of conversion gain, dc power and RF/IF bandwidth for the given technology.

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TABLE I

Performance Comparison Of Transmitters

Ref.	Frequency (GHz)	Data rate - Modulation	Integration	Psat. (dBm)	DC power (mW)	Gain (dB)	Technology
[3]	120	9 Gbit/s -ASK	Oscillator+ ASK Modulator	-19.2	80.9	-	65 nm CMOS
[4]	120	10 Gbit/s -ASK	Frequency doubler +ASK Modulator+ Power amplifier	0	500	-	0.1 µm InP-HEMT
[12]	140	4 Gbit/s -ASK	Amplitude Modulator+LO Amplifier+VCO	-8	-	-	SiGe BiCMOS
[5]	142	14 Gbit/s -OOK	Oscillator+Mixer+PA	8.7	66	7 dB (diff.)	0.13 µm BiCMOS
[6]	110-170	48 Gbit/s -QPSK	I/Q Modulator+PA+LO tripler	9	165	25	0.25 µm InP DHBT
This work	120-150	12 Gbit/s QPSK	Modulator	-4.5	52	9.5 dB	0.13 µm SiGe BiCMOS