FPGA-Based Implementation and Experimental Demonstration of a Vehicular VLC System

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***Abstract*—Amidst the widespread deployment of LED lighting in vehicles, visible light communications (VLC) has emerged as a promising solution for reliable vehicle-to-vehicle (V2V) connectivity. This paper presents an FPGA-based design and implementation of a vehicular visible light communication (VLC) system employing On-Off Keying (OOK) modulation. The system uses a low-beam vehicular headlight as the wireless transmitter while the encoding, modulation, and demodulation modules are implemented on the Zynq-7000 series FPGA. At the receiver side, a 25.4 mm biconvex lens is utilized in front of the photodetector for received power improvement at longer distances. SNR, data rate, packet loss ratio, and BER results are shared from an extensive measurement campaign carried out in broad daylight conditions for up to 20 m distance. The experimental results demonstrate promising data rates and signal-to-noise ratios at distances of up to 14 m, highlighting the potential of VLC-based solutions for short-range vehicular communication.**

***Index Terms*—Vehicular Visible Light Communication, FPGA, Outdoor VLC, OOK, Signal-to-Noise Ratio, Optical Receivers**

I. Introduction

In recent years, vehicular automation has emerged as a pivotal research area within the automotive industry with the primary goal of improving driving efficiency and road safety. One of the applications of achieving vehicular autonomy is vehicular platooning, where autonomous vehicles move cohesively in closely-knit groups. This mechanism promises to not only enhance road throughput but also significantly reduce traffic congestion, ultimately paving the way for safer and more efficient roadways. To realize this scenario, robust Vehicle-to-Vehicle (V2V) communication is essential for facilitating the real-time exchange of critical vehicular state parameters including speed, acceleration, and potential fault alerts [1].

Historically, the IEEE 802.11p standard, utilizing Radio Frequency (RF) communication, has been favored for vehicular communication, given its capability for long-range and high-data-rate transmissions. Yet, its efficacy in high-density traffic environments is increasingly being brought into question. Specifically, RF communication faces challenges like channel congestion, making it a less-than-ideal candidate for the dynamic and safety-critical requirements of platooning systems [2]. To address these RF limitations, this study explores the potential of Visible Light Communication (VLC) as an alternative medium. The availability of LED-based exterior lighting solutions in vehicles has positioned visible light communication (VLC) as a natural candidate for vehicle-to-vehicle (V2V) connectivity [3], presenting a myriad of benefits: it operates on a license-free spectrum, is cost-effective, and uniquely doubles as both a lighting and communication entity. Such attributes render VLC a promising candidate for outdoor vehicular applications, especially when considering Intelligent Transportation Systems (ITS) [4].

Our research, detailed in the following sections, presents an FPGA-based design of a vehicular VLC system, employing the On-Off Keying (OOK) modulation scheme. By leveraging the standard Ford F-Max truck's vehicular headlights and the advanced capabilities of the Zynq-7000 series FPGA, we introduce a VLC system optimized for vehicular environments. The rest of the paper is organized as follows: in section II, we discuss the related works and highlight the novelty of our work. In section III, we present the system design and implementation details. In section IV, we describe our experimental setup and share results from our measurement campaign performed in outdoor broad daylight conditions. Finally, we conclude the paper and discuss future directions in section V.

II. Related Works

The implementation of a vehicular VLC system involves modulating the optical intensity of a vehicular headlight with binary information superimposed over the DC bias. The modulation frequency is selected high enough to avoid any flickering while remaining within the bandwidth limit of the LED. At the receiver end, a photodetector is utilized for collecting the received optical signal.

Several vehicular VLC system implementations, employing microprocessor or PC-based solutions, have been reported in the literature. For example, a vehicular VLC prototype system was developed using Raspberry Pi microprocessor in [5], and a communication link span of up to 12 m was achieved at a data rate of 9.6 kbps. In [6, 7], National Instruments Universal Software Radio Peripherals (USRPs) were utilized, and the baseband signal processing blocks were implemented in LabVIEW software on PC. In [8], a similar USRP-based set-up was demonstrated using the open-source software

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GNU Radio. Although such PC-based baseband processing solutions offer flexibility, broad functionality, and relatively easier implementation of advanced modulation schemes, they have certain limitations, particularly in terms of real-time processing capabilities and power consumption. FPGA-based system-on-chip (SoC) devices present an attractive alternate solution due to their inherent parallelism, high processing speed, and low latency, which are crucial for the implementation of high-performance real-time communication systems.

Some works on FPGA-based VLC system implementations were reported in [9–17]. Studies [9–11] focus solely on detailing the FPGA implementation of various modulation schemes for VLC systems and evaluating FPGA resources and power utilization, without reporting any actual results from VLC experiments. Other works [12–15] provide some experimental results but are limited to indoor VLC systems. As wireless transmitters, they use indoor LEDs which typically follow a Lambertian pattern. On the other hand, vehicular headlights have an asymmetrical intensity distribution. Furthermore, these are high-power LEDs that require a custom-design driver. In [16], a 6 W LED module certified for automotive applications is utilized, but the experiments are still performed indoors at a 6 m distance and a data rate of only 100 kbps is reported.

In this study, we present an FPGA-based vehicular VLC system utilizing the Zynq-7000 series SoC development board and a custom-design front-end featuring a 26 W vehicular low-beam headlight LED module. At the receiver side, we explore the usage of a 25.4 mm biconvex lens in front of the photodetector to observe the improvement in overall system performance. Our implemented system shows promising results in broad daylight conditions indicating its potential applicability not only in platooning but in a range of other vehicular scenarios. To the best of the authors' knowledge, no prior works have provided a comprehensive investigation of real-time FPGA-based VLC system implementation and experimental evaluation for vehicular connectivity.

III. System Design and Implementation

A. Transmitter Design

Fig. 1 shows the block diagram of the implemented system. Data from the transmitter PC is transmitted as UDP packets via ethernet to the Eclypse Z7 SoC development board that features the Zynq-7000 series FPGA [18]. This board is split into two primary blocks: the processing system (PS) block, and the programmable logic (PL) block. The UDP packets that arrive at the SoC board are initially processed by the PS block. This operation is executed in the Xilinx Software Development Kit (SDK) using C language. The processed packets are then stored in system memory in the form of a frame structure to be later accessed by the PL block for transmission.

The frame structure for transmission is illustrated in Fig. 2. Each frame begins with an 8-bit header assigned the binary value '11011011', succeeded by a 16-bit field that indicates the payload length, representing the number of data bytes within the frame. Following this field are the actual data bytes. In adherence to standard networking practices, the maximum

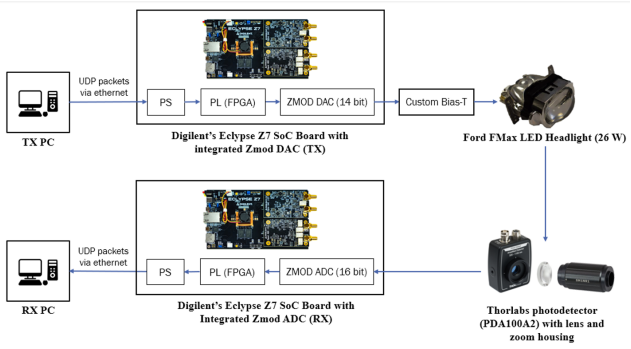


Fig. 1. System block diagram

allowable data bytes in each frame is limited to 1450 bytes. This conservative threshold ensures that the total size of the packet does not exceed the typical Maximum Transmission Unit (MTU) of 1500 bytes for Ethernet, thus preventing fragmentation and potential transmission inefficiencies. The frame concludes with an 8-bit footer, assigned the value '10100101'. Both the header and footer bytes are utilized at the receiver end for frame detection.

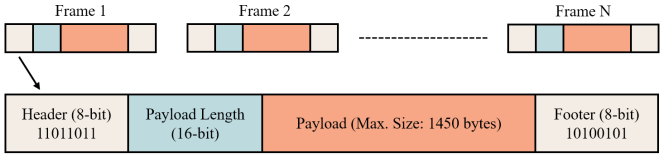


Fig. 2. Frame structure

We employ on-off keying (OOK) modulation in our system, which is implemented in the PL block using VHDL and associated Intellectual Property (IP) cores from the Xilinx Vivado Design Suite. The PL block retrieves the frame structure from system memory byte-by-byte. Each byte is then transmitted to the integrated 14-bit Zmod DAC module bit-by-bit. Notably, each bit read from the BRAM (Block RAM) is assigned multiple samples before being sent to the DAC. The number of samples assigned to each bit (both 1s and 0s) plays a key role in determining the achievable data rate. Given that both the FPGA and the DAC operate at 100 MHz and 100 Msps respectively, a lower number of samples per bit can yield a higher data rate. For instance, 10 samples per bit can achieve up to 10 Mbps, while 5 samples per bit can reach up to 20 Mbps. However, the inherent bandwidth of our vehicular LED which is around 2.3 MHz as depicted in Fig. 3 (b) puts a constraint on the number of samples per bit to be chosen. To ensure reliable communication and account for other system constraints, we've opted for 25 samples per bit for our current study, targeting a data rate of 4 Mbps.

The generated samples for each bit are then directed to the Zmod DAC's associated IP core within Vivado for transmission. The DAC IP is configured to provide an output signal in the range of ±5 V. Given the DAC's 14-bit resolution, it can represent values from -8192 to 8191 (decimal), corresponding

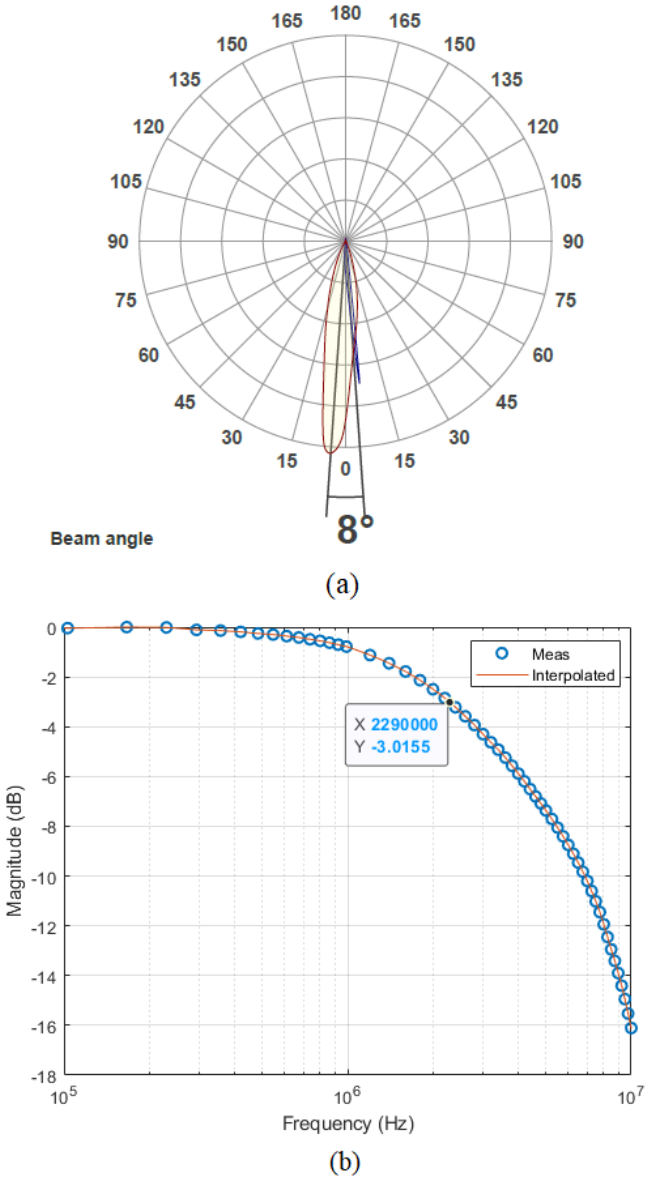


Fig. 3. (a) 26-W Ford F-Max LED radiation pattern (b) LED's 3-dB bandwidth

to voltages from -5 V to +5 V. In our configuration, samples corresponding to '1's are assigned DAC values between 820 and 4100 (decimal), translating to approximately +0.5 V to +2.5 V. Conversely, samples representing '0's are given values between -820 and -4100 (decimal), corresponding to roughly -0.5 V to -2.5 V. The exact values are chosen according to the linear region of operation of the LED.

The output of the DAC module is directed into the AC input port of a custom-design bias-T. This high-current bias-T is designed and built in-house specifically for driving high-power vehicular LEDs and is capable to support DC currents of up to 12-A with a 3-dB bandwidth of approximately 11 MHz. The output of the Bias-T is connected to the 26-W Ford F-Max low-beam headlight LED module that will be used as VLC transmitter. Fig. 3 (a) illustrates the radiation pattern of the LED, showing a narrow beam angle with a Full Width at Half Maximum (FWHM) of only 8 degrees. This focused or 'directional' light distribution is attributed to the specific design of the LED, tailored to cater to road illumination applications where precise directional lighting is paramount. This characteristic significantly diverges from indoor LEDs, which typically conform more closely to a Lambertian emission pattern, thereby delivering a broader light dispersion suitable for general indoor lighting. Fig. 3 (b) shows the frequency response of the LED module. The analysis shows a 3-dB bandwidth of approximately 2.3 MHz.

TABLE I
SYSTEM PARAMETERS SUMMARY

Parameter	Value
Maximum Payload Length	1450 bytes
Modulation Scheme	On-Off Keying
Number of Samples per Bit	25
FPGA Operating Frequency	100 MHz
Zmod DAC and ADC Sampling Rate	100 Msps

TABLE II
HARDWARE COMPONENTS SPECIFICATIONS

Component	Model	Features
FPGA-based SoC Board	Eclypse Z7	Integrated DAC & ADC
Bias-T	Built In-House	11 MHz BW
Headlight LED	Ford F-Max	26 W, 2.3 MHz BW
Photodetector	PDA100A2	11 MHz BW
Bi-Convex Lens	LB1027-A	Ø: 25.4 mm, f: 40 mm

B. Receiver Design

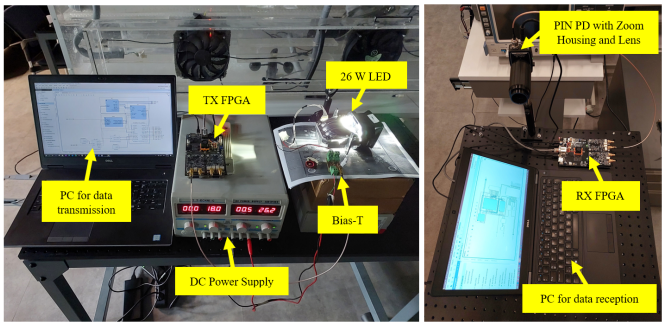
On the receiver side, the optical intensity is captured using Thorlabs' PDA100A2 PIN adjustable-gain photodetector module (active area: $75.4\,\text{mm}^2$, field of view (FOV): $53°$). This module, equipped with a built-in transimpedance amplifier, converts the photodetector output (photocurrent) to a corresponding voltage signal. At a gain setting of 0 dB, its bandwidth is 11 MHz. However, this drops to 1.4 MHz at a 10 dB setting. Given that the inherent bandwidth of our LED stands at 2.3 MHz, the 10 dB gain setting of the photodetector cannot be utilized. A 25.4 mm diameter bi-convex lens with a focal length of 40 mm is therefore positioned in front of the photodetector using a zoom housing (as shown in Fig. 5) to enhance the received optical power and achieve a longer communication distance.

The output of the photodetector module is transferred to the 16-bit Zmod ADC module integrated with the Eclypse Z7 SoC development board. The received signal, now in 16-bit format, is processed by the PL block of the SoC development board. Here, an envelope detection and thresholding mechanism classifies incoming samples against a fixed threshold: samples below are deemed '0', and those above are '1'. The state machine continuously searches for the header byte pattern '11011011'. Upon identifying this header, it begins receiving

the entire frame bit-by-bit and keeps writing each received byte to BRAM to be later accessed by PS. The reception process also keeps checking for the footer byte '10100101'. If the footer byte is not received, or if the received data byte count mismatches the received payload length or surpasses 1450 bytes, the system flags it as a false detection and re-initiates the search for a new header. Once the footer byte is received, the entire frame saved in BRAM in byte format is accessed by the PS block. The PS block then converts this frame back into UDP format and finally dispatches the converted data to the receiver PC via Ethernet. A summary of the system parameters and hardware components specifications is provided in Table I and Table II respectively.

IV. Experimental Setup and Measurement Results

Fig. 4 (a) and (b) show the transmitter and receiver setup respectively. For the measurement campaign, two vehicles were customized using an aluminum profile structure to hold the LED and photodetector units. The low-beam headlight LED module was mounted in front of the transmitter vehicle while the Thorlabs' PDA100A2 photodetector along with zoom housing and lens were mounted at the rear of the receiver vehicle (see Fig. 5). The rest of the transmitter and receiver equipment were placed inside their respective vehicles. Fig. 5 shows the experimental vehicles positioned 6 meters apart in an outdoor sunny environment. All experiments were performed in broad daylight during similar times of the day in the late afternoon, with similar ambient lighting and clear weather conditions.



(a) (b)

Fig. 4. (a) Transmitter setup, (b) Receiver setup

Fig. 6 shows the measured SNR (in dB), data rate (in Mbps), Bit Error Rate (BER), and packet loss ratio (%) plotted against transmission distance (in m). The data rate, BER, and packet loss ratio are determined based on the transmission of 10,000 packets, each being 1450 bytes in size (116 million bits). All four graphs shown in Fig. 6 (a-d) depict measurements made under three different scenarios at the receiver side as follows: 1) photodetector without zoom housing or lens (represented by blue curves), 2) photodetector with an attached zoom housing (red curves), and 3) photodetector with a 25.4 mm lens positioned inside the attached zoom housing (indicated by yellow curves).

For scenario 1, up to distances of 8 m, the measurements highlight an SNR consistently above 10 dB, a data rate exceeding 3.5 Mbps, a BER at or below 1×10^{-1}, and a packet loss ratio under 10%. However, as the inter-vehicle distance is further increased, the system performance starts to degrade. Next, in scenario 2, it's evident that the introduction of the zoom housing in front of the photodetector (without the lens) negatively influences the receiver's performance by reducing the effective field of view. Specifically, introducing the zoom housing results in an average SNR reduction of 10.9%, a 7.6% decrease in data rate, a 2.5% rise in the BER, and a 19.6% increase in packet loss ratio over the entire measurement span from 2 m to 20 m.

Lastly, in scenario 3, the inclusion of the 25.4 mm lens within the affixed zoom housing evidently enhances the overall system performance. Specifically, employing the lens with zoom housing results in an average SNR improvement exceeding 9 dB over the entire measured distance of 2 to 20 m when compared to results without using zoom housing and lens (Fig. 6 (a)). Additionally, the SNR remains above 10 dB for as long as 18 m distance which is a marked improvement over scenarios 1 and 2. This improvement in SNR subsequently translates to enhancements in other system performance metrics as well, including data rate, BER, and packet loss ratio. For example, as shown in Fig. 6 (b), the inclusion of the lens causes the data rate to remain above 4 Mbps for up to 10 m distance and 2 Mbps for up to 18 m, a marked improvement over the results when the lens was not utilized. Regarding BER, there's a notable average improvement of over 65% for distances up to 10 m when compared to scenarios 1 and 2 (Fig. 6 (c)). Also, the BER remains at or below 1×10^{-1} for up to 10 m distance, after which, the BER rates become similar to those observed in scenarios 1 and 2. Lastly, packet loss ratio stays below 20% for distances up to 14 m in scenario 3 (Fig. 6 (d)), a significant improvement when compared to scenarios 1 and 2, where the packet loss ratio was observed to be 50% and 66% respectively at 14 m distance.

V. Conclusion and Future Directions

In this study, the implementation and experimental evaluation of an FPGA-based vehicle-to-vehicle VLC system in outdoor conditions using OOK modulation is presented. The FPGA implementation allowed for the efficient utilization of the inherent bandwidth of the vehicular LED, achieving data rates of up to 4 Mbps. At the receiver side, the utilization of a 25.4 mm biconvex lens in front of the photodetector is also investigated. The experimental results in the broad daylight scenario show significant improvements in SNR, data rate, BER, and packet loss ratio by utilizing the lens, demonstrating the potential of using VLC for vehicular communication in line-of-sight situations. It is however noted that while the utilization of lens enhances system performance, the accompanying zoom housing diminishes it and introduces pronounced directionality by limiting the receiver's effective field of view.

Future works will aim to design a system that integrates the lens directly in front of the photodetector, bypassing the use of the zoom housing. Additionally, future research will aim to improve the BER performance of the system

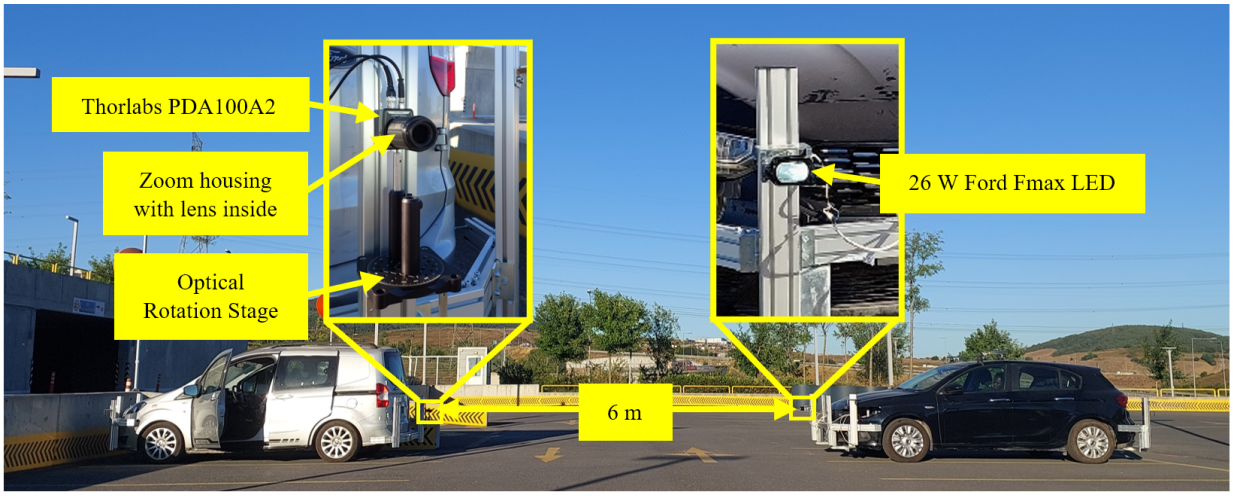


Fig. 5. Transmitter and receiver vehicles placed at a 6 m distance for measurements in outdoor daylight conditions

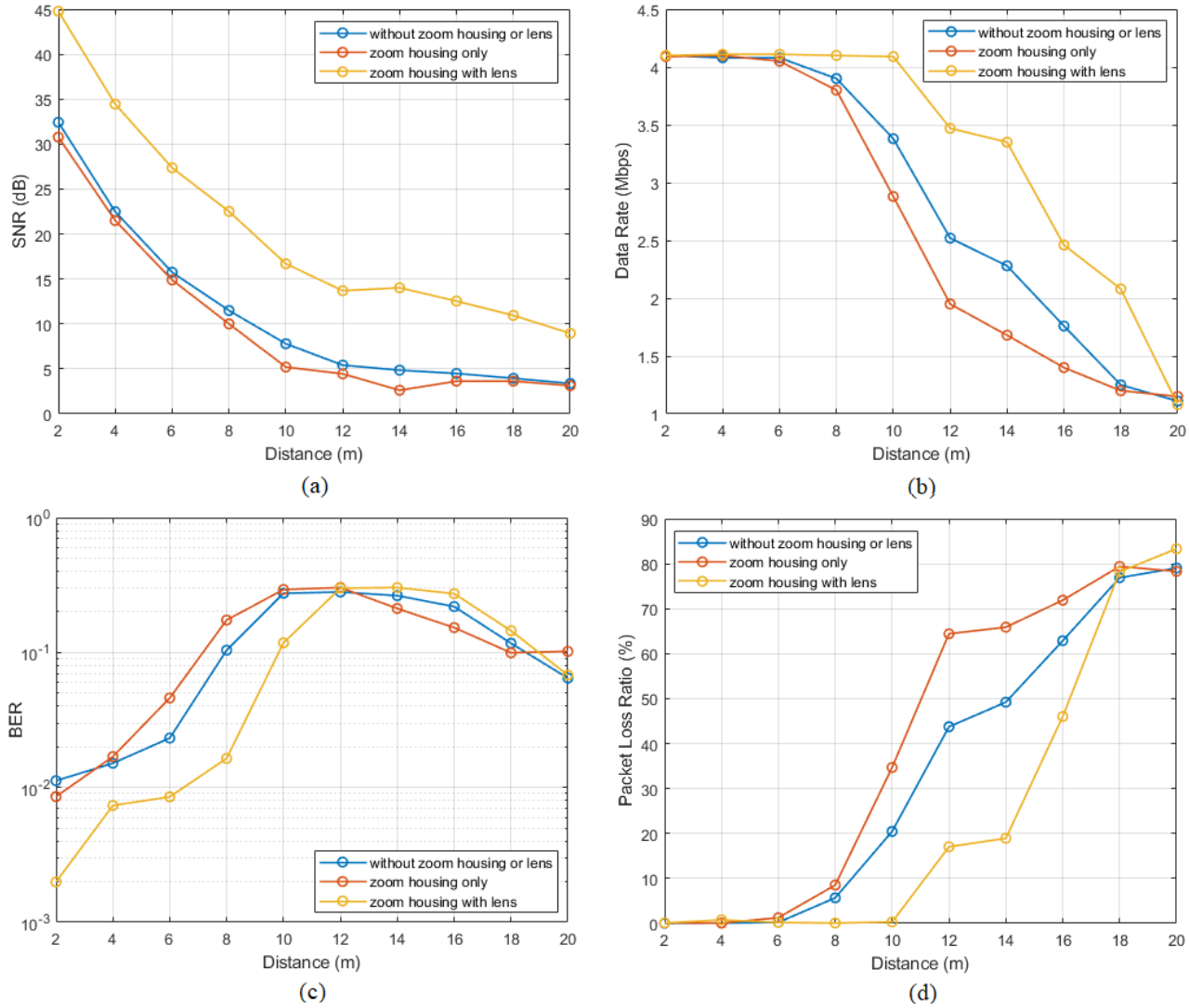


Fig. 6. (a) SNR vs. distance, (b) data rate vs. distance, (c) BER vs. distance, (d) packet loss ratio vs. distance

and also explore the use of multiple vehicular LEDs and photodetectors to address mobility-related challenges. The vehicular LED's bandwidth is also planned to be improved by utilizing pre-equalization and/or blue filtering techniques to support vehicular applications demanding higher data rates.

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REFERENCES

[1] B. Soner and S. Coleri, "Visible light communication based vehicle localization for collision avoidance and platooning," *IEEE Transactions on Vehicular Technology*, vol. 70, no. 3, pp. 2167–2180, 2021.

[2] M. Y. Abualhoul, M. Marouf, O. Shagdar, and F. Nashashibi, "Platooning control using visible light communications: A feasibility study," in *16th International IEEE Conference on Intelligent Transportation Systems (ITSC 2013)*, 2013, pp. 1535–1540.

[3] A. Memedi and F. Dressler, "Vehicular visible light communications: A survey," *IEEE Communications Surveys Tutorials*, vol. 23, no. 1, pp. 161–181, 2021.

[4] M. Y. Abualhoul, O. Shagdar, and F. Nashashibi, "Visible light inter-vehicle communication for platooning of autonomous vehicles," in *2016 IEEE Intelligent Vehicles Symposium (IV)*, 2016, pp. 508–513.

[5] K. Lega, S. Naga Haneesh Sammeta, D. Bollepally, G. Kalyan Mallavarapu, E. Eso, Z. Ghassemlooy, and S. Zvanovec, "A real-time vehicular visible light communications for smart transportation," in *2020 12th International Symposium on Communication Systems, Networks and Digital Signal Processing (CSNDSP)*, 2020, pp. 1–5.

[6] B. Aly, M. Elamassie, and M. Uysal, "Vehicular vlc system with selection combining," *IEEE Transactions on Vehicular Technology*, vol. 71, no. 11, pp. 12 350–12 355, 2022.

[7] B. Turan, O. Narmanlioglu, S. C. Ergen, and M. Uysal, "Physical layer implementation of standard compliant vehicular vlc," in *2016 IEEE 84th Vehicular Technology Conference (VTC-Fall)*, 2016, pp. 1–5.

[8] M. S. Amjad, C. Tebruegge, A. Memedi, S. Kruse, C. Kress, J. C. Scheytt, and F. Dressler, "Towards an ieee 802.11 compliant system for outdoor vehicular visible light communications," *IEEE Transactions on Vehicular Technology*, vol. 70, no. 6, pp. 5749–5761, 2021.

[9] R. Alindra, P. S. Priambodo, and K. Ramli, "Fpga implementation of ofdm-based visible light communication system," in *2022 International Conference on Informatics Electrical and Electronics (ICIEE)*, 2022, pp. 1–6.

[10] O. N. Samijayani, D. I. Savitri, D. Astharini, K. Azrina, S. Rahmatia, and R. Alindra, "Implementation of visible light communication using pam on xilinx artix 7 35t fpga," in *2018 IEEE 5th International Conference on Engineering Technologies and Applied Sciences (ICETAS)*, 2018, pp. 1–5.

[11] V. E. Levent, G. Saglam, H. F. Ugurdag, N. Fajar Rizqi Annafianto, F. Aydin, S. W. Tesfay, B. Aly, M. Elamassie, B. Kebapci, and M. Uysal, "Fpga based dco-ofdm phy transceiver for vlc systems," in *2019 11th International Conference on Electrical and Electronics Engineering (ELECO)*, 2019, pp. 418–421.

[12] E. Setiawan, S. Fuada, and T. Adiono, "Experimental demonstration of ofdm visible light communications based on system-on-chip," in *2018 International Symposium on Electronics and Smart Devices (ISESD)*, 2018, pp. 1–5.

[13] Q. Chen, M. Zhang, Z. Ghassemlooy, P. Luo, D. Han, and B. Zhang, "Implementation and experimental demonstration of a real-time 7-dsss vlc system based on fpga," in *2016 15th International Conference on Optical Communications and Networks (ICOCN)*, 2016, pp. 1–3.

[14] Q. Huo, M. Zhang, W. Xu, D. Han, M. Wu, and Q. Li, "Fpga-based 120mbps online visible light communication system with rgb leds," in *2016 15th International Conference on Optical Communications and Networks (ICOCN)*, 2016, pp. 1–3.

[15] Y. Zhang, M. Zhang, H. Zhou, Y. Sun, C. Wei, and W. He, "A long distance real-time dpsk visible light communication system based on fpga," in *2019 18th International Conference on Optical Communications and Networks (ICOCN)*, 2019, pp. 1–3.

[16] S. Ricci, S. Caputo, and L. Mucchi, "Fpga-based visible light communications instrument for implementation and testing of ultralow latency applications," *IEEE Transactions on Instrumentation and Measurement*, vol. 72, pp. 1–11, 2023.

[17] I. Bağlıca, B. N. Ashfaq, S. Ergin, B. Kebapçı, T. Baykas, and M. Uysal, "Experimental demonstration of an fpga-based outdoor vlc broadcasting system," in *2023 31st Signal Processing and Communications Applications Conference (SIU)*, 2023, pp. 1–4.

[18] Digilent. Eclypse z7. Accessed: 2023-09-15. [Online]. Available: https://digilent.com/reference/programmable-logic/eclypse-z7/start