Optimizing Wireless Power Transfer Efficiency in Cascaded H-Bridge Converter through an Auxiliary Resonant Circuit Pole

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***Abstract*—The usage of an Auxiliary Resonant Commutated Pole (ARCP) circuit with an 11-level Cascaded H-Bridge (CHB) converter as an option for feeding high-power Wireless Power Transfer (WPT) track-pads in traction applications is proposed in this research. By utilizing a mathematical model to obtain the switching pulses of the ARCP circuit, a reduction in the conduction losses of the involved inductance can be achieved. Moreover, an optimization routine is developed to reduce the MOSFETs' root mean square current by finding each module's phase shift angles. The study uses the SAE J2954 standard to restrict the Electromagnetic Interference (EMI) in the frequency band between $400\,kHz$ and $30\,MHz$. The success of the suggested technique is displayed by simulation results showing that it is possible to operate the CHB with Zero Voltage Switching in all modules of the power converter. Inductive Power Transfer applications applied in railways can benefit from this contribution due to the use of multilevel converters.**

***Index Terms*—Auxiliary Resonant Commutated Pole, Wireless Power Transfer, Cascaded H-Bridge, Railways.**

I. Introduction

Wireless Power Transfer (WPT) technology can increase the efficiency and convenience of charging batteries, especially in situations where wired connections are not possible or desirable. Several studies have explored the use of different designs in transmitter and receiver pads, compensation networks and modulation techniques to improve the efficiency and performance of WPT systems and these are well-reported in [1]–[4].

Many researchers are working to improve the electrification process or the current network with the purpose of improving efficiency and reducing cost. Unfortunately, there are areas which currently utilise diesel traction where the electrification is not possible since the train may run under a bridge or through an area of natural beauty where the addition of overhead lines may be restricted. Further research has also taken place into the use of energy storage both on the train itself and at local substations in an effort to support the electrification and ensure that energy is not wasted, for example, when braking [5]. A possible solution to ensure that energy storage systems and their use in onboard electrical traction applications can be achieved, even in areas where overhead lines may be prohibited or where the construction and maintenance costs of overhead lines can be high [6], is with the use of Wireless Power Transfer.

Recently, attention has been drawn to Dynamic Wireless Power Transfer, which enables the charging of the battery onboard while the vehicle is in motion [2], [3], and has garnered interest due to the possibility of reducing the mass of batteries in heavy-duty vehicles like railways [7]–[9]. In this sense, new designs in coil tracks and receivers have been developed [10], [11]. Figure 1a presents an example of how to implement Dynamic WPT on railways, which uses a single-phase transmitter coil on the train track, like the single-phase meander topology with the power converter next to the railway track, as shown in Fig. 1b. This topology is investigated to cover a wide area for high power WPT [3], [6], [10] applications.

An essential element to enable the use of high-power WPT is the incorporation of power electronics. In this sense, multilevel power converters appear as solutions, but they face the challenge of drawing power from medium voltages (MV) grids while ensuring Electromagnetic Compatibility (EMC) and high efficiency. In this sense, Zero Voltage Switching (ZVS) operation is essential to achieve these objectives. For

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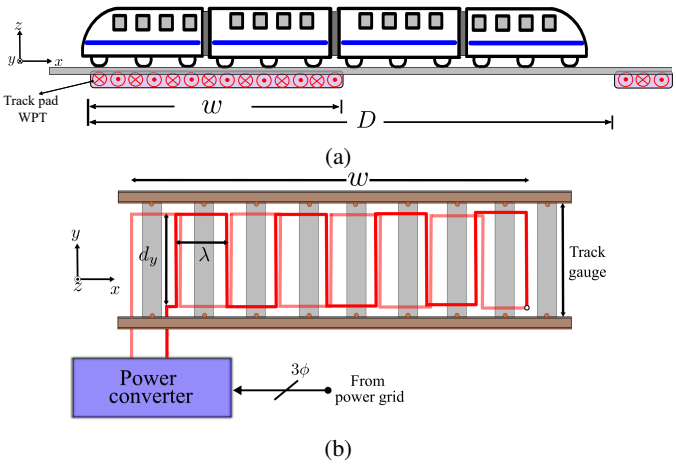


Fig. 1: Example application of Dynamic Wireless Power Transfer (WPT) in railways: (a) Single-phase transmitter coils positioned on the track (covering w meters) and spaced apart D meters. (b) A close-up view of the trackpad with coils having a height d_y and width λ, demonstrating the single-phase meander design.

instance, in [12], a Modular Multilevel Converter (MMC) with integrated magnetics and a complex strategy scheme was proposed to ensure ZVS for all switches over a wide range of operations.

A recent study [13] proposed a Cascaded H-bridge (CHB) converter that reduces the count of High-Frequency Transformers (HFTs) while enabling Zero-Voltage Switching over a wide range of operations changing the modulation strategy. However, HFTs incorporation in two out of three modules compromises the modularity feature and results in a complex modulation strategy. Another study in [14] introduced an asymmetric CHB converter that implements a phase shift strategy in only one module, while the rest operate with zero or π phase shift angles, depending on the voltage input conditions concerning the system, to reduce switch losses. Unfortunately, this approach fails to ensure ZVS in the CHB modules, resulting in an unequal power distribution among modules and asymmetric stress on the semiconductors.

Numerous research papers have studied how to reduce switching losses in power converters by incorporating resonant stages with LC components, as mentioned in sources such as [15], [16]. One notable topology is the Auxiliary Resonant Commutated Pole (ARCP) circuit, which can decrease Electromagnetic Interference (EMI) issues with fewer components and minimal loss in efficiency [17]. An ARCP circuit is a power converter that uses an auxiliary resonance circuit to achieve zero voltage turn-on in the primary circuit and maintain zero current turn-offs in the auxiliary one. The ARCP topology was first introduced in [18] and has been applied in various soft-switching Pulse Width Modulation micro-inverters [19], DC-DC converters [20], and even resonant converters [21]. In [22], the authors conducted experiments and concluded that Silicon and Silicon Carbide devices perform similarly in ARCP circuits.

The present work aims to integrate the Auxiliary Resonant Commutated Pole circuit into each Cascaded H-Bridge module. This configuration guarantees Zero Voltage Switching with phase shift operation and incorporates a swapping strategy that balances the power supplied in each module. To determine the optimal angle selection for the CHB, an optimization routine is employed to reduce the Root Mean Square (RMS) current value in the semiconductor, considering the harmonics constraints specified by the SAE J2954 standard, particularly in the range from $400\,kHz$ to $30\,MHz$. Furthermore, this article considers the impact of phase shift and converter output current on the ARCP's inductor current during the resonant stage.

II. Auxiliary Resonant Commutated Pole

Commonly in Wireless Power Transfer technology, the resonant converter operates at a frequency above the resonance, in the inductive region, system to maintain a lag current in relation to the voltage and to ensure ZVS turn on. However, a phase shift strategy can make it impossible to conserve this feature for broad phase shift angles without an increase in the lag angle, as shown in [13]. To address this issue, an alternative for operating an H-Bridge module with a phase shift strategy is the introduction of an auxiliary circuit.

Based on the above, the following analysis is based on the H-bridge configuration depicted in Fig. 2, which operates in resonance for WPT applications. It is assumed that the operation occurs with a well-tuned resonant tank and at a frequency equal to $\omega_{WPT} = 2\pi/T = 2\pi f_{WPT}$, with a sinusoidal current output having an amplitude of $\hat{I}$ and a quasi-square wave voltage output with a phase shift angle of φ.

For clarity, a one-half cycle will be described in the subsequent subsections because the MOSFET pulses remain constant during the fundamental period. For the analysis, it is assumed that the ARCP circuit and semiconductors have negligible losses.

A. ARCP operation

The ARCP topology is shown in Fig.2, connected to a standard H-bridge module at O_1. The auxiliary circuit is compounded by the MOSFETs Q_{z1} and Q_{z2}, the inductance L_z as the energy storage device, and the clamping diodes D_{z1} and D_{z2}. These last components have the task of circuit protection in case of over-voltages. The C_{oss} capacitance corresponds to the non-linear parasitic output MOSFET capacitance, which must be discharged to ensure a ZVS operation. In this particular topology, only $C_{oss,1}$ and $C_{oss,2}$ interact with the auxiliary circuit (considering unipolar modulation), so the following analysis will focus on the left leg of the H-bridge module.

The operation of the ARCP is based on three stages; charging, resonance, and discharging. The voltages and currents details are shown in Fig. 3a, where the initial voltages in $C_{oss,1}$ and $C_{oss,2}$ are V_{dc} and $0\,V$, respectively. At the same time, the

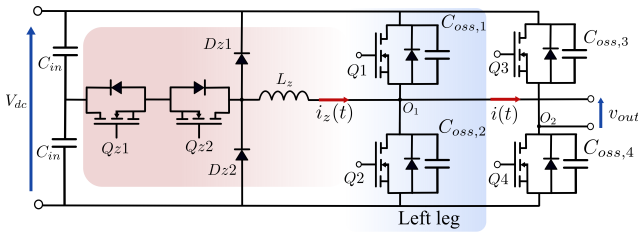


Fig. 2: H-bridge module with the Auxiliary Resonant Commuted Pole circuit.

current $i(t)$ is assumed to circulate through the Q_2 MOSFET channel.

The charge instance (Fig. 3b) starts with Q_{z1} turning on, increasing the current $i_z(t)$ and the L_z energy storage. The voltages across the Mosfets do not change due to capacitors not interacting with the circuit. When $t = t_z$, the charging process ends, Q_2 goes to zero, i_{Q2} goes to zero, and $i_z(t)$ reaches the value I_{z0}, generating a difference with respect to $i(t)$ equal to ΔI_z. The current in the inductor is modelled as in:

$$i_z(t) = \frac{V_{dc}}{2L_z} \cdot t; \qquad -t_z \leq t < 0 \tag{1}$$

While the voltages $v_{c1}(t)$ and $v_{c2}(t)$ will keep on V_{dc} and $0\,V$, respectively.

In the case of the resonance stage, shown in Fig. 3c, L_z interacts with $C_{oss,1}$ to discharge it and charge $C_{oss,2}$. The second-order equivalent circuit operates in resonance at a frequency ω_0, normally higher than the fundamental frequency ω_{WPT} at the output H-bridge module. When the process starts, the inductor current i_z and $v_{c2}(t)$ increase in a sinusoidal way. When $t = t_{ri}$, the current i_z equals I_{z0} and voltage v_{c1} is not zero, thus the process continues until t_{rv}, when $v_{c2} = V_{dc}$ and $v_c1 = 0$. It should be noticed from Fig. 3a that the time t_{ri} is lower than t_{rv}, being equals only when $i(t_L) = i(0)$. The dynamic behaviour of $i_z(t)$, $v_{c1}(t)$, $v_{c2}(t)$ is described by (2)-(4), taking $\omega_0 \gg \omega_{WPT}$ into account.

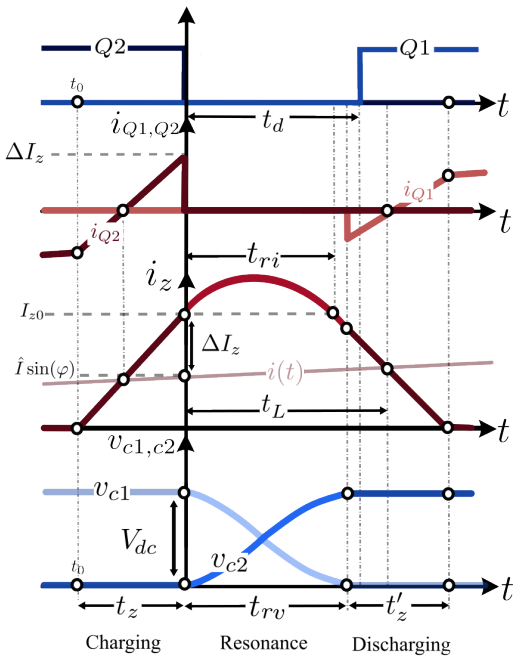
$$\begin{aligned} i_z(t) = \hat{I}\sin(\omega_{WPT}t + \varphi) + \Delta I_z \cos(\omega_0 t) \\ + \left(\frac{V_{dc}}{2Z_0} - \frac{\omega_{WPT}}{\omega_0}\hat{I}\cos\varphi\right)\sin(\omega_0 t) \end{aligned} \tag{2}$$

$$\begin{aligned} v_{c1}(t) = \frac{V_{dc}}{2} + \frac{Z_0\hat{I}\omega_{WPT}}{\omega_0}\cos(\omega_{WPT}t+\varphi) - Z_0\Delta I_z \sin(\omega_0 t) \\ - \left(\frac{V_{dc}}{2} - \frac{Z_0\omega_{WPT}\hat{I}\cos\varphi}{\omega_0}\right)\cos(\omega_0 t) \end{aligned} \tag{3}$$

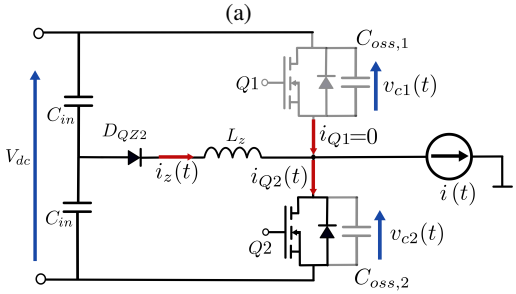
$$v_{c2}(t) = V_{dc} - v_{c1}(t) \tag{4}$$

where

$$\omega_0 = \frac{1}{\sqrt{L_z(C_{oss,1}+C_{oss,2})}}\ ;\ Z_0 = \sqrt{\frac{L_z}{C_{oss,1}+C_{oss,2}}} \tag{5}$$



(a)



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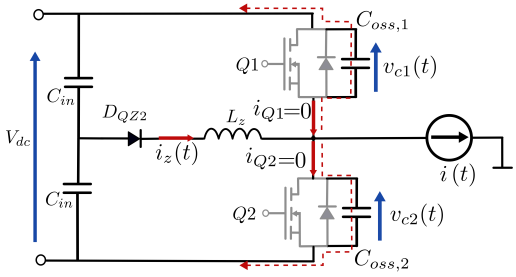

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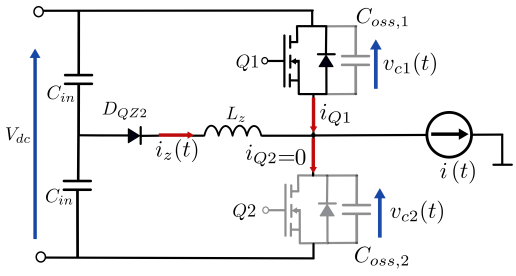

(d)

Fig. 3: Behaviour of ARCP. (a) i_{Q1}, i_{Q2}, i_z, v_{c1} and v_{c2} plot, and its equivalent circuit during (b) charging, (c) resonance and (d) discharging process.

When the resonance stage ends, the diode in Q_1 starts to conduct, and immediately the current i_{Q1} changes to a negative value lower than ΔI_z. When $Q1$ is high, the voltage in the body diode is zero, and a soft turn-on switching is reached. However, the discharging process continues, and L_z keeps transferring energy to the source until $t = t_L$, where it flows toward the load. Once the discharging process ends, i_{Q1} equals the load current. This process has a time-lapse of t'_z, described by (6).

$$i_z(t) = i_z(t_{rv}) - \frac{V_{dc}}{2L_z}(t - t_{rv}); \qquad t_{rv} < t \leq t_{rv} + t'_z \quad (6)$$

This study considers $t_{rv} < t_d < t_L$ to ensure Zero Voltage Switching during the turning on of Q_1 and Q_2 MOSFET devices, otherwise the v_{c1} could be greater than zero at the switching lapse (i.e. $t_{rv} > t_d$), or producing an undesired resonant stage (i.e. $t_d > t_L$). Based in Fig 3a, t_L can be approximated by (7), assuming $t'_z \approx t_z$, which increases with an increment in ΔI_z or t_{rv}, and decreases with smaller shift angles φ. It is noticed that the t_L is always greater than t_{rv}, so the dead time should be selected based on those calculations.

$$t_L \approx \frac{\Delta I_z + \frac{V_{dc}}{2L_z} t_{rv}}{\hat{I}\omega_0 \cos(\varphi) + \frac{V_{dc}}{2L_z}} \quad (7)$$

In Fig. 4 one and a half fundamental cycle is shown jointly with voltage on the parasitic capacitance, i_{Q1}, switching pulses Q_{z1} and Q_{z2}, and the current $i_z(t)$. The dynamic in the currents i_z, voltages v_{c1} and v_{c2}, have an impact on the output voltage v_{out}, which creates a trapezoidal waveform with a time rise equal to t_{rv}. At the same time, the dynamic behaviour of the voltage across the Q_3 and $Q4$ body diode introduces a decay time t_e.

Furthermore, the ARCP impacts the switching current i_{Q1}, incorporating an additional slope depending on the L_z, the current at the inverter output and the phase shift angle, creating additional conduction losses compared with the hard-switching scenario. Due to this reason, the phase shift angle could be selected to reduce these conduction losses.

B. ARCP design

According to Fig. 3a and (3), a larger inductance will increase t_z and t_{rv} time, soaring the RMS i_z value and in consequence, the conduction losses in the ARCP. On the other hand, a larger inductance value offers more difference time between t_{rv} and t_L, which is good to ensure a soft switching during the turning-on, considering the delays and rise time. Therefore, the inductance L_z will be selected as small as the dI/dt semiconductor limitation is accomplished and have a reasonable time difference between t_{rv} and t_L.

An increase in the parasitic capacitance or L_z would raise the resonant time stage, the i_z peak current, and the current capability of the Q_{z1} and Q_{z2} MOSFETs. Since the parasitic capacitance is dependent on the SiC packaging design, the authors of [22] suggest the incorporation of an additional snubber in parallel to increase the total capacitance up to tens of nF. To increase the resonant time stage, reduce conduction losses, and ensure a safe and smooth switching on, a trade-off between an increase in L_z and additional capacitances must be analyzed.

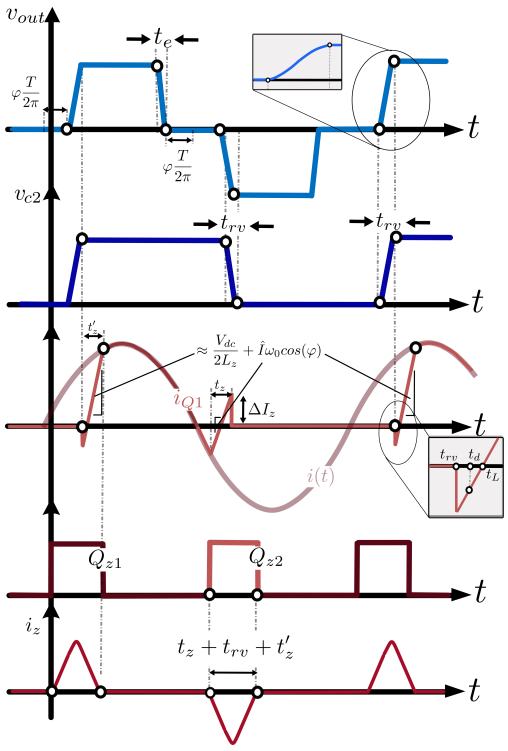

Fig. 4: H-Bridge output voltage, voltage across v_{c2}, switching current i_{Q1}, switching pulses ARCP and current inductor i_z during one and half fundamental cycle.

The values of t_{ri} and t_{rv} are selected to minimize the magnitude of ΔI_z, Assuming that the voltage input, C_{oss} values, current amplitude, frequency and phase shift angle are known. The analytical expression for ΔI_z as a function of t_{ri} and t_{rv} is described by (8) and (9) which are obtained from (2) and (3) respectively. In Fig. 5, the dependency of the resonance times and ΔI_z are shown for different phase shift angles, considering an application example. It is noticed that the t_{ri} values are smaller than t_{rv} times for the same current level and φ angle, and tend to be equal for greater ΔI_z values. Considering the above, just the selection of t_{rv} will be considered in the further steps.

$$\Delta I_z(t_{ri}) = \left(\frac{V_{dc}}{2Z_0} - \frac{\omega_{WPT}\hat{I}\cos(\varphi)}{\omega_0}\right)\cot\left(\frac{\omega_0 t_{ri}}{2}\right) \quad (8)$$

$$+ \frac{\hat{I}\cos(\varphi)\omega_{WPT} t_{ri}}{1 - cos(\omega_0 t_{ri})}$$

$$\Delta I_z(t_{rv}) = \frac{V_{dc}}{2Z_0}\cot\left(\frac{\omega_0 t_{rv}}{2}\right) - \frac{\omega_{WPT}\hat{I}\cos(\varphi)}{\omega_0}\cot(\omega_0 t_{rv}) + \frac{\hat{I}\omega_{WPT}\cos(\omega_{WPT}t_{rv}+\varphi)}{\omega_0\sin(\omega_0 t_{rv})} \tag{9}$$

In order to reduce the conduction losses, ΔI_z should be as small as possible, which means that t_{rv} and t_L will be greater. However, based on (7), a large t_{rv} does not ensure soft turning on in the MOSFETs, and the difference between t_L and t_{rv} should be higher enough to deal with delays and rise times.

The parasitic capacitance's charge and discharge of Q_3 and Q_4 occur during the dead time and depend on the current magnitude, capacitance and voltage input. To ensure ZVS capability on Q_3 and Q_4 during the turning on, t_e in Fig. 3a must satisfy (10). At the same time, t_d must satisfy $t_{rv} < t_d < t_L$, as is shown in Fig. 3a. Therefore, to guarantee ZVS, this study considers t_L at least 1.5 times greater than t_{rv}.

$$t_e \approx \frac{(C_{oss,3}+C_{oss,4})V_{dc}}{\hat{I}\sin(\varphi)} < t_d \tag{10}$$

The third step considers the t_z and t_z' calculation. The first one is obtained based on the ΔI_z current and (1). The computation is described on (11). A similar procedure should be applied to obtain t_z' but using (12), based on (3d).

$$t_z = 2L_z\left(\frac{\Delta I_z + \hat{I}\sin(\varphi)}{V_{dc}}\right) \tag{11}$$

$$t_z' = 2L_z\left(\frac{i_z(t_{rv})}{V_{dc}}\right) \approx t_z \tag{12}$$

Finally, the pulse width for Q_{z1} and Q_{z2} is made, as shown in Fig. 3a, based on the sum of t_z, t_{rv} and t_z'.

III. Angle Search for Cascaded H-Bridge Converter

The final application of this auxiliary circuit analyzed above is to ensure the ZVS feature in the H-Bridge converter, whose terminal will be connected with other modules to create a CHB converter able to supply high power to track coils in the railway WPT. To keep the modularity feature of the CHB, the ARCP components and input voltages for each module must be the same.

The output voltage in each module could have distinct values for the phase shift angle to reduce the harmonic content, EMI and losses, guaranteeing a fundamental component able to satisfy the load requirements. However, this strategy will require swapping the pulses in each module to balance the power delivered by each one [23]. This paper will consider a swapping frequency f_{WPT}/n, with n equal to the number of H-bridge modules in the CHB converter.

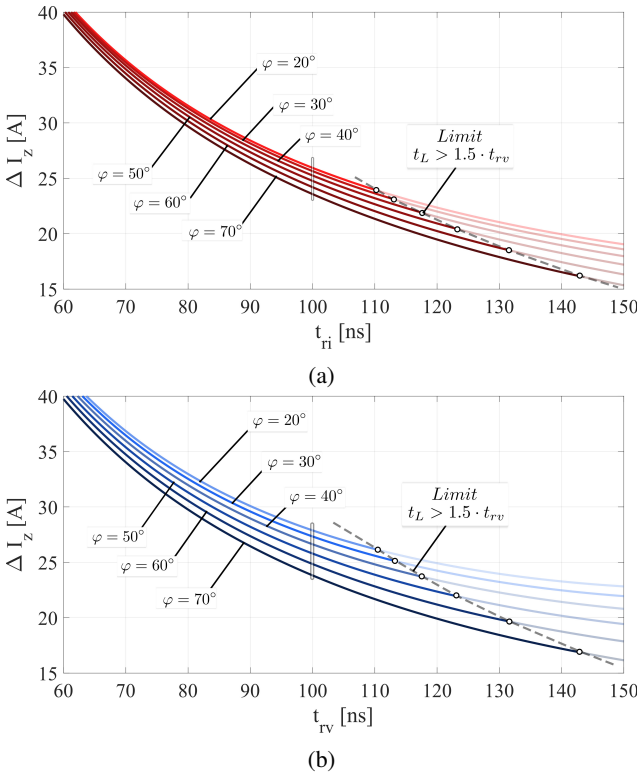

Fig. 5: Difference between i_z current and $i(t)$ at the beginning of the resonance stage, considering $V_{dc} = 650\,V$, $C_{oss,1} = C_{oss,2} = 1.85nF$ (CAS325M12HM2), $L_z = 3\mu H$, $\hat{I} = 306\,A$, and $f_{WPT} = 60\,kHz$. (a) $\Delta I_z(t_{ri})$ (b) $\Delta I_z(t_{rv})$.

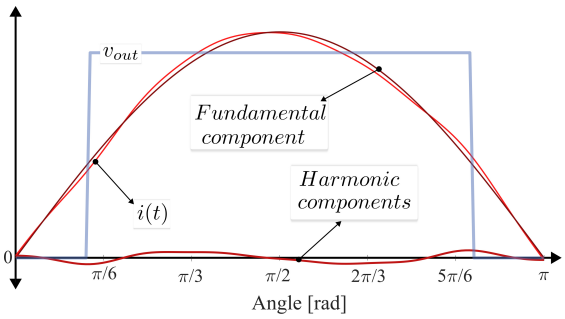

Fig. 6: Output voltage v_{out} and current waveform ($i(t)$). The fundamental current component and the sum of harmonics are also shown.

A. Restriction for the angle selection

Considering the degree of freedom introduced by the number of modules, the angle selection could have multiple solutions depending on the approach. In the case of Inductive Power Transfer, additional restrictions regarding the limits on the magnetic intensity produced by the WPT coils are mentioned in international standards such as SAE J2954 and ICNIRP Guideline 2010 [24]. The first one establishes recommendations limits on a frequency band which decays from $400\,kHz$ to $12\,MHz$ where a minimum value is reached and it should be kept from $12\,MHz$ to $30\,MHZ$.

One solution to finding the angles is to work with Selective Harmonic Elimination (SHE) modulation. Nevertheless, the standard approach of harmonic minimization is not practical due to the difference between the number of harmonics to eliminate and freedom degrees, which means that this technique does not always ensure a feasible solution for the studied application [25]. On the other hand, the harmonic mitigation technique is more flexible because it uses limits on individual harmonic content.

In this study, the limits for the $k-th$ harmonics are given by the square wave signal and expressed by (13), considering the frequency band defined on the SAE J2954 standard. The above means that the odd harmonics between $400\,kHz$ to $30\,MHz$ will be mitigated.

$$v_k = \sum_{i=1}^{n} \cos(k\varphi_n) \leq n \tag{13}$$

One of the challenges is the magnitude of the low-order harmonic signal, ranging from the fundamental component up to $400\,kHz$. The removal of those harmonic elements could not guarantee a feasible solution, given the need to mitigate a wide high-frequency band. In this sense, this article proposes an upper and lower limit for these harmonic bands to improve the chances of reaching a solution in the optimization routine. It is important to note that using this approach may produce an output current that is not completely sinusoidal. However, this distorted output can be an advantage in achieving zero voltage switching on MOSFETs. It can lead to lower current values compared to a purely sinusoidal output, particularly at smaller phase shift angles. An illustration of this can be seen in Figure 6. In essence, adopting this strategy ensures that the resonance stage can be accomplished in less time than the designated time, reducing t_{rv} to below the predetermined threshold while ensuring that the time to charge/discharge $C_{oss,3}$ and $C_{oss,4}$ remains below the limit stated in (10).

B. Optimization

Once the boundaries on the harmonic content have been established, an optimization routine can be programmed to obtain the angles. In this study, the objective function will be the minimization of RMS current value of i_{Q1} to reduce the conduction losses, where the angle selection impacts on the ΔI_z value and the slopes during the inductor L_z charging and discharging process, as is shown in Fig. 3a.

Considering that the power converter involves n modules operating with staircase modulation with swapping the φ_i-th angle to balance the power output in each H-Bridge, the optimization routine must consider the sum of i_Q currents in each module during one fundamental period. In summary, the objective function is declared as

$$min\ J(\vec{\varphi}, \Delta I_z, t_{rv}) = \sum_{i=1}^{n} \sqrt{\frac{1}{T}\int_{a_i}^{b_i} i_{Q_i}^2(t, \Delta I_z, \varphi_i)dt} \tag{14}$$

Where $a_i = t_{rv} + \varphi_i T/2\pi$, $b_i = T/2 + \varphi_i T/2\pi$ and $\vec{\varphi} = [\varphi_1, \varphi_2, ..., \varphi_n]$.

IV. Simulation results

A simulation model was developed and analyzed to assess the performance of the ARCP design. The model was based on the parameters presented in [26] but used an 11-level CHB ($n = 5$) converter with ARCP integrated, as illustrated in Fig.7. The inductance of L_z was set to $3\mu H$, and the capacitance values of $C_{oss,1} = C_{oss,2} = 1.85\,nF$ were obtained using the datasheet information (CAS325M12HM2) and the recommendations mentioned in [27]. The simulation was designed to operate at $V_{dc} = 650\,V$, $\omega_{WPT} = 60\,kHz$, and $\hat{I} = 306\,A$. The simulation was performed using the circuit simulator Plecs.

TABLE I: Optimization result.

	$t_z[\mu s]$	$I_{z0}[A]$
$\varphi = 32.09°$	17.4	188
$\varphi = 29.22°$	16.2	175
$\varphi = 26.20°$	14.9	161
$\varphi = 23.30°$	13.6	147
$\varphi = 20.42°$	12.3	133

To determine the optimal phase shift angles, taking into account the restrictions imposed by high-order harmonics (SAE J2954) and third harmonic ($0.15 \leq v_3 \leq 5$), the optimization routine in (14) was solved using a genetic algorithm [28] in the Matlab Optimization Live Editor. The study uses $t_{rv} = 100\,ns$ and $t_d = 120\,ns$, which were chosen based on the limits presented in Fig. 5a and 5b. A minimum phase shift angle of $20°$ was required to satisfy (10). The optimization results, along with the values of t_z and I_z, are shown in Table I.

Figure 8a depicts one cycle of the voltage output at the CHB terminal. The waveform has a trapezoidal shape due to the harmonic content restrictions. By zooming in on the waveform, the dynamic behaviour during the turning-on process in $Q3$ becomes visible. Precisely, when the time t_e' is less than t_{rv}, it indicates that the ZVS feature is achieved.

Figure 8b depicts the soft switching transition of $Q1$ at a phase shift angle of $\varphi = 32.08°$. The module's output voltage rises from $0\,V$ to $650\,V$ within a time interval equivalent to t_{rv_1}, which is less than t_d. At the start of MOSFET $Q1$ conduction, the voltage across the parasitic capacitor is zero, and the current i_{Q1} is negative during the time interval of $t_L - t_d$. It is noteworthy that t_{rv1} is less than $100\,ns$ due to a decrease in ΔI_z triggered by the low order harmonics present in the current, as illustrated in Fig. 6.

The achievement of the zero-voltage switching characteristic for all phase shift angles was established through an analysis of the current behaviour in the inductor L_z. To demonstrate the operational effectiveness of the ARCP in conjunction with the swapping strategy, Fig. 10 exhibits five fundamental cycles of the inductor current in one module. The objective is to showcase that power is balanced in each CHB module can be achieved by the implementation of ARCP and the swapping strategy.

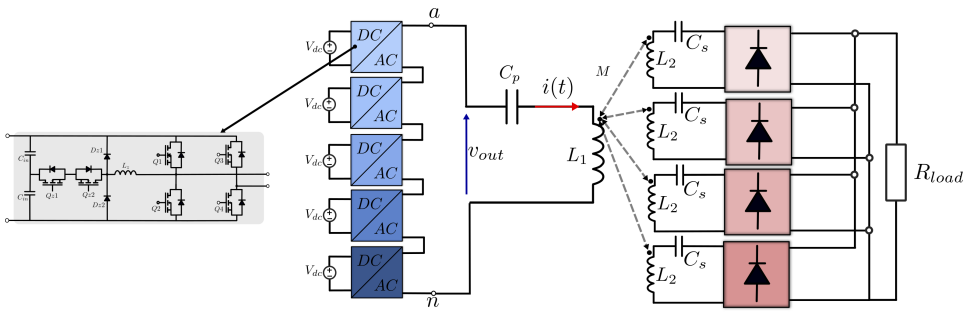

Fig. 7: Power converter topology and equivalent circuit for both transmitter coil and pickup coils of WPT system to be used in dynamic charging of railways.

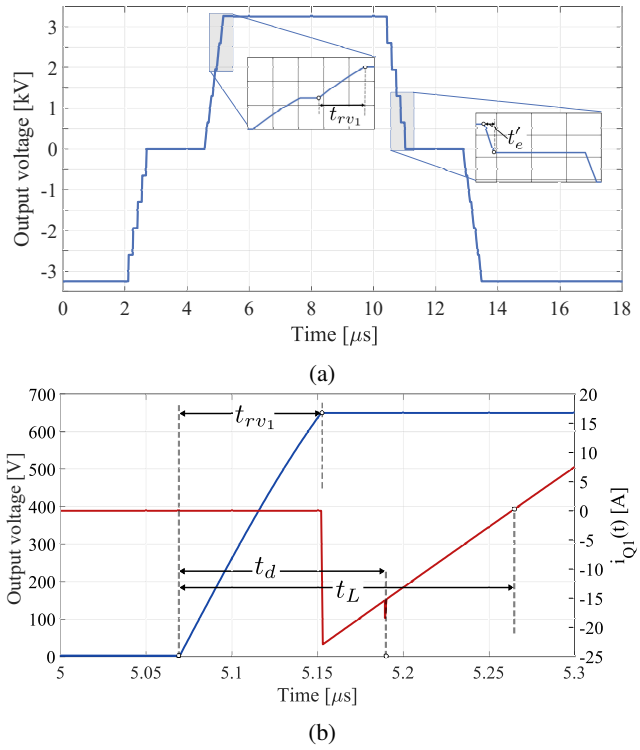

Fig. 8: Voltages output (a) at the CHB output terminal, (b) at module 1 with i_{Q1} current (red) to show the ZVS behaviour when $\varphi = 32.08°$.

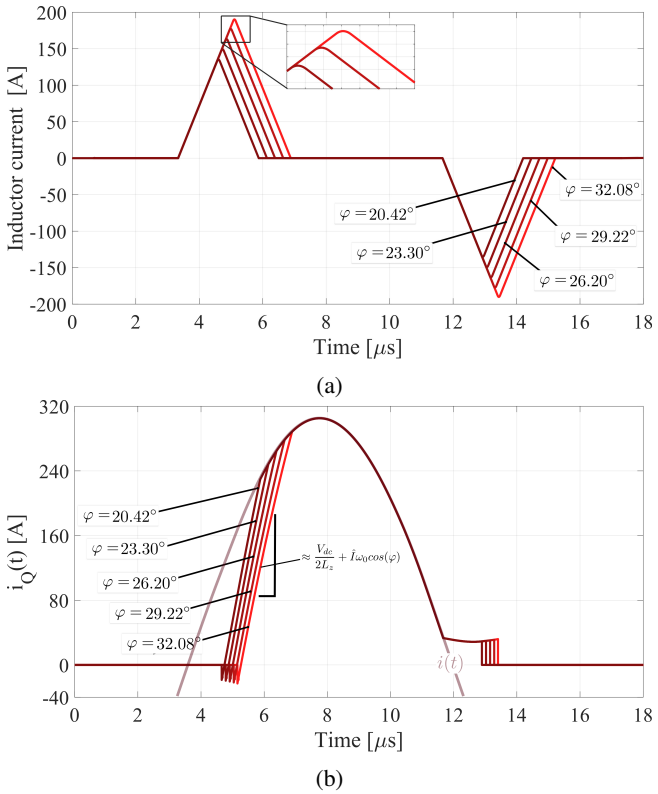

Fig. 9: Dynamic of i_{Q1} and i_z during one cycle in each module. (a)$i_z(t)$, (b) $i_{Q1}(t)$.

V. Conclusions

The multilevel power converter with an Auxiliary Resonant Commutated Pole circuit described in this study can be used as a resonant converter for Wireless Power Transfer in electric railway traction. In regions of the railway network where installing overhead lines may be forbidden or challenging, this Inductive Power Transfer technology can be employed.

The purpose of this work is to achieve zero-voltage switching at high-frequency operation by incorporating ARCP into CHB converter for a high power Inductive Power Transfer system. An optimization routine, which includes restrictions according to the SAE J2954 standard, was designed to reduce conduction losses by finding the firing angles. The development of analytical models for the ARCP behaviour and the proposed guidelines to calculate the operation times have shown the potential for integration of the auxiliary circuit into the CHB converter.

To validate the theoretical framework, simulations have been carried out. The simulation results have demonstrated the feasibility of the proposed approach for achieving soft switching in CHB systems. The proposed approach might be experimentally validated while taking into account power losses, and EMI issues to verify the SAE J2954 standard.

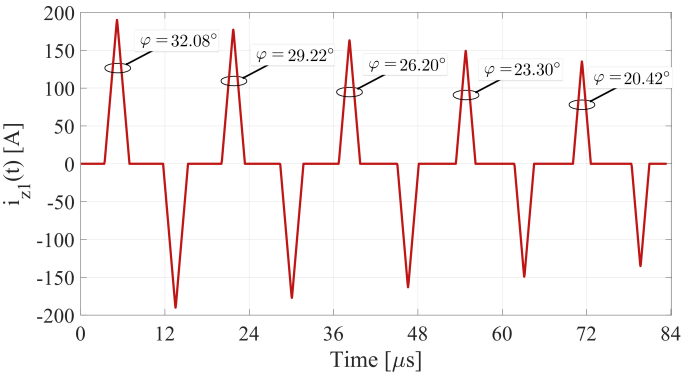

Fig. 10: Current in L_z inductor from one module during five fundamental cycles.

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