

Correlated Non-Ideal Effects of Dark and Light I-V Characteristics in a-Si/c-Si Heterojunction Solar Cells

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Abstract—a-Si/c-Si heterojunction solar cells exhibit several distinctive dark and light I-V non-ideal features. The dark I-V of these cells exhibits unusually high ideality factors at low forward bias and the occurrence of a ‘knee’ at medium forward bias. Non-idealities under illumination, such as the failure of superposition and the occurrence of an ‘S-type’ curve, are also reported in these cells. However, the origin of these non-idealities and how the dark I-V non-idealities manifest themselves under illumination, as well as vice versa, have not been clearly and consistently explained in the current literature. In this study, a numerical framework is used to interpret the origin of the dark I-V non-idealities and a novel simulation technique is developed to separate the photo-current and the contact injection current components of the light I-V. Using this technique, the voltage dependence of photo-current is studied to explain the failure of the superposition principle and the origin of the S-type light I-V characteristics. The analysis provides a number of insights into the correlations between the dark I-V and the light I-V. Finally, using the experimental results from this study and from the current literature, it is shown that these non-ideal effects indeed affect the dark I-V and the light I-V in a predictable manner.

Index Terms— amorphous semiconductors, current-voltage characteristics, heterojunctions, process control, silicon, modeling and simulation

I. INTRODUCTION

FINDING a cost effective alternative to traditional c-Si solar cells has been a major driving force in the development of the a-Si/c-Si heterojunction solar cell technology [1], [2]. These so called ‘HITTM’ cells have demonstrated efficiencies exceeding 24% [3], comparable to those of the champion c-Si solar cells [4]. However, its complex heterojunction structure makes optimization of the cells challenging.

An important step towards designing high quality solar cells is to understand the non-idealities in carrier transport that can degrade the solar cell performance. Analysis of the dark I-V and the light I-V provides insights into the non-idealities of carrier transport that affect a-Si/c-Si solar cell efficiency. In the literature, the low bias transport (in the dark) is generally

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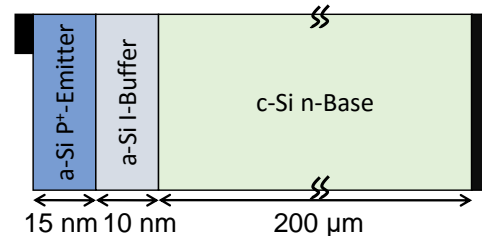


Fig. 1. Diagram of P+/I/n a-Si/c-Si heterojunction solar cell.

attributed to one of two mechanisms – namely, multi-tunneling capture emission across a-Si region [5] or diffusion flux across the barrier [6]. The two mechanisms are distinguished by the temperature dependence of the slope of the dark I-V characteristics plotted in a semi-log plot. Under high forward bias, carrier transport appears to be dominated by diffusion [7], [8]. However, it is frequently observed that there are a number of the non-ideal features in the dark I-V, such as unusually high ideality factors ($\gg 2$), occurrence of a “knee” in the medium bias range, etc. [5], [6], [8]–[12], irrespective of the low bias transport mechanism. The physical origin of these features are not fully understood. A consistent explanation of these features in the dark I-V may provide a renewed perspective in analyzing and optimizing these cells.

Likewise, several studies in the literature discuss the distinctive features of the light I-V characteristics of a-Si/c-Si heterojunction solar cells. In these solar cells, it is known that superposition may or may not hold until the V_{OC} point. This failure of superposition appears to be correlated to the process details in fabricating the cell [13]–[15]. Indeed, several experimental reports (e.g., [16]–[19]) have suggested a link between the properties of a-Si and the occurrence of a non-ideal S-type curve under certain circumstances. Further, numerical modeling was used to understand the transport mechanism under light using tunneling across the a-Si/c-Si interface and drift diffusion based transport [20], as well as hot carrier based transport [21]. These studies were mainly confined to understanding the light I-V properties, without any specific effort to correlate the features to the dark I-V.

Das et al. [17] reported a comprehensive set of both experimental dark I-V and light I-V characteristics obtained by varying the a-Si process conditions [22]. Based on the shape of the light I-V characteristics, the authors summarize their dark and light I-V observations into three categories, namely, Type-1, Type-2 and Type-3 responses as shown in Fig. 2. Using the $Suns-V_{OC}$ measurement under white, blue, and infrared light, they postulated that the presence of a barrier to minority carrier (hole) conduction may cause the S-type curve in some the

samples. However, this study was mainly focused on understanding the light I-V behavior and the authors did not correlate the dark and the light I-V characteristics from a device physics perspective. In this paper, we will use the same dark and light I-V data set (along with our own measurements) to establish the physical origin of the correlation between the dark and light I-V characteristics.

In section II, we explore the origin of the non-ideal features in the dark I-V characteristics. In section III, we use a novel simulation technique to isolate the photo-current and the contact injection current components of the light I-V characteristics. In section IV, the non-ideal effects of the dark I-V and light I-V characteristics are correlated and the experimental data are interpreted based on the theory developed in sections II and III. Finally, in section V, we discuss the effects of interface defects on the analysis of the dark I-V characteristics.

II. PHYSICS OF CARRIER TRANSPORT IN THE DARK

A. Experimental Observations

Industrial-grade P+/I/n solar cell samples were used in this study. The P+ a-Si emitter and an intrinsic a-Si buffer layer were deposited on the front side of a c-Si wafer, while the back side was coated with Aluminum to act as the back surface field and the back contact. The diagram of the solar cell is provided in Fig. 1. The dark and the light I-V for five samples were measured using a Keithley 4200SCS measurement setup.

The dark I-V characteristics are first analyzed for parasitic shunt conduction, as follows. From the reverse bias characteristics (not shown in figure), it is easy to obtain the nonlinear shunt resistance of the solar cell, i.e.,

$$J_{Sh} = G_{Sh}V + J_{0Sh}V^\gamma. \quad (1)$$

The range of γ was found to be, $1 < \gamma < 2$, reflecting the space charge limited transport [23], [24]. The excellent uniformity of the pre-factors (G_{Sh} , J_{0Sh}) for the measured samples, as summarized in Table I, indicates the process uniformity. The slight difference in the parameters reflect inevitable variations in the fabrication process.

Next, the forward biased dark I-V is ‘cleaned’ by subtracting the effects of the parasitic shunt current by using the ‘reflection’ method suggested in [24], [25]; this allows consideration of the intrinsic I-V features uncontaminated by shunt conduction. A typical shunt-corrected forward bias dark I-V characteristics (of

TABLE I
SUMMARY OF MEASURED DARK I-V RESULTS

Sample No.	Shunt Parameters			Forward Bias Parameters			
	G_{Sh} S cm ⁻² x10 ⁻⁵	J_{0Sh} x10 ⁻⁸	γ	n_{MFB}	V_2^{Dark} V	J_0 A cm ⁻² x10 ⁻¹⁰	n_{HFB}
A	1.7	1.8	1.0	3.7	0.48	0.4	1.2
B	1.6	1.7	2.0	4.1	0.49	8.0	1.5
C	1.9	1.8	1.0	3.9	0.47	2.1	1.3
D	3.9	1.6	0.9	3.7	0.47	93	1.7
E	1.6	0.6	2.0	3.0	0.42	11	1.4

The shunt parameters are extracted from the measured dark I-V data using the method developed in [24]. The n_{MFB} indicate abnormally high ideality factors ($n_{MFB} \gg 2$).

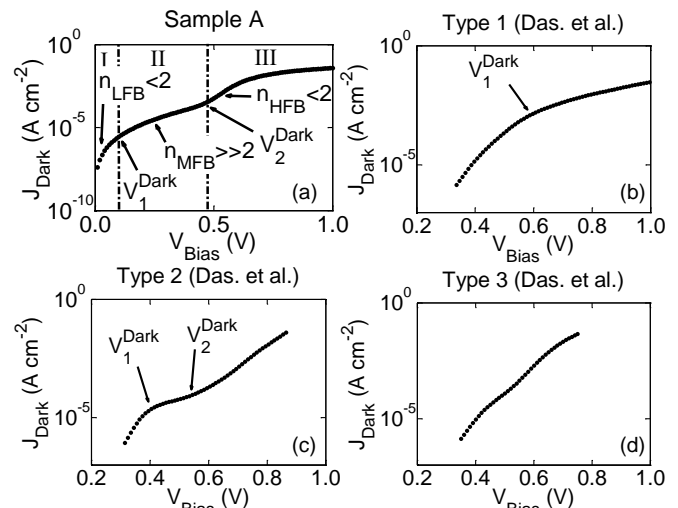


Fig. 2. (a) The shunt corrected dark I-V of sample no. 1 used in this study is plotted. The bias where the ideality factor crosses 2 ($V_{Bias} = V_1^{Dark}$) and bias where the ideality factor drops below 2 ($V_{Bias} = V_2^{Dark}$) are marked. The vertical lines separate the different bias regions. (b) The measured dark I-V of a type-1 sample reported in [17] is plotted. The V_1^{Dark} is also indicated for this sample. (c) The measured dark I-V of a type-2 sample reported in [17] is plotted. The V_1^{Dark} and V_2^{Dark} are also indicated. (d) The measured dark I-V of a type-3 sample reported in [17] is plotted. There is no unusually high ideality region observed for this sample in the plotted bias range.

sample A) is shown in Fig. 2(a). The shunt corrected experimental dark I-V was fitted with a phenomenological single diode model,

$$J_{Dark}^{Fit} = J_0 e^{\frac{q(V_{Bias} - IR_{Series})}{n\kappa_B T}}, \quad (2)$$

where, J_0 is reverse saturation current, R_{Series} is the series resistance and n is the ideality factor. We will define n_{LFB} , n_{MFB} , n_{HFB} as being the ideality factors at low ($V_{Bias} < V_1^{Dark} \approx 0.1V$ to $0.3V$, Region I), medium ($V_{Bias} \approx 0.4 V$), and high forward bias ($V_{Bias} \approx 0.6 V$), respectively. The parameters obtained from these fits are summarized in Table I. Note that ideality factors are obtained from the local derivative of the $\log(J_{Dark})-V_{Bias}$ curve. However, these ideality factors do not imply an exponential $\log(J_{Dark})-V_{Bias}$ relationship, rather they indicate the degree of complexity of $J_{Dark}-V_{Bias}$ characteristics in these solar cells.

Under low forward bias (at $V_{Bias} < V_1^{Dark} \approx 0.1V$ to $0.3V$), marked as region I in Fig. 2(a), n_{LFB} is below 2 for all of the samples. On increasing the bias ($V_1^{Dark} < V_{Bias} < V_2^{Dark} \approx 0.5 V$; region II), n_{MFB} exceeded 3 for all of the samples; this result is consistent with other studies, as reported in section I. It is difficult to interpret such a high n_{MFB} in terms of classical transport mechanisms associated with p-n or p-i-n junctions where the ideality factors generally do not exceed the value 2. Moreover, at the intermediate voltage ($V_{Bias} = V_2^{Dark} \approx 0.5 V$), a ‘knee’ appears in the dark I-V characteristics, see Fig. 2(a). Finally, at high forward bias, the dark current increases exponentially (with $n_{HFB} < 2$), until it is saturated by the R_{Series} , see region III of Fig. 2(a).

The non-idealities in the dark I-V characteristics, such as, the high ideality factors ($n_{MFB} > 2$) above $V_{Bias} = V_1^{Dark}$ and the occurrence of ‘knee’ were also observed by Das et al. [17]. As mentioned in the Introduction, these authors classified their

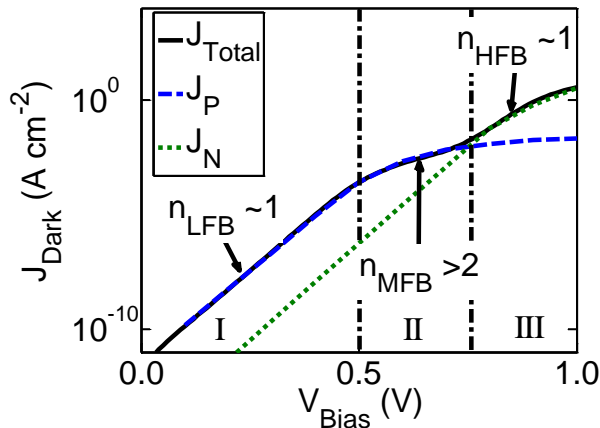


Fig. 3. Numerical dark I-V, J_{Dark} , along with the J_N and J_P at the front contact is plotted for an ideal a-Si/c-Si interface device. The vertical lines separate the different bias regions.

cells into 3 categories (i.e., type-1, type-2 and type-3), depending on the shape of the light I-V characteristics. The corresponding dark I-V characteristics for each of these types are plotted in Fig. 2(b), (c) and (d). It can be observed that the type-1 and type-2 samples also show regions of unusually high ideality factors ($n_{MFB} > 2$) in certain bias ranges. Different from type-1 (but similar to sample A), the type-2 sample features a ‘knee’ above which the ideality factor falls below 2. However, these non-idealities are not observed in the type-3 sample, see Fig. 2(d). In the following subsection, we will use detailed numerical simulations to explore the physical origin of these non-ideal effects and explain why they occur in some cells, but not in others.

B. Numerical Simulation of the Dark Current

In order to understand the carrier transport and to explain the observed dark I-V behavior, numerical simulations using ADEPT 2.0 [26] are used in this section. The simulations are based on the standard material parameters for c-Si and a-Si layer obtained from [20], [27]. The minority carrier surface recombination velocities at the front (s_f) and the back (s_b) are

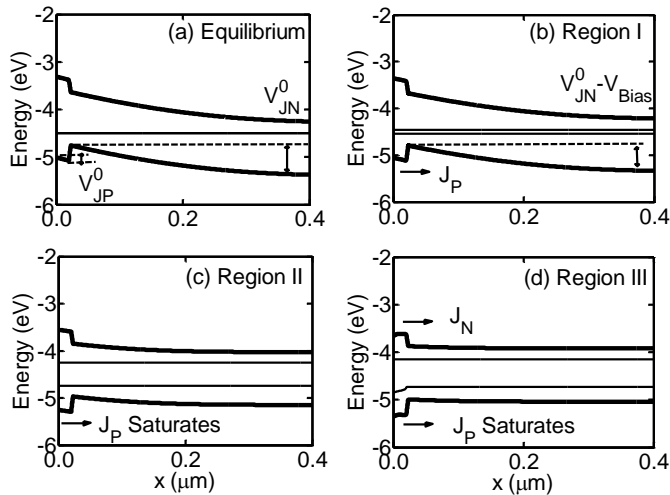


Fig. 4. Schematic of energy band diagram in (a) equilibrium, indicating the band bending in a-Si side (V_{JP}^0) and c-Si side (V_{JN}^0) of the interface, (b) region I ($0 < V_{Bias} < V_1^{Dark}$) where J_P is the dominant current component, (c) region II ($V_1^{Dark} < V_{Bias} < V_2^{Dark}$) where J_P saturates, and (d) region III ($V_{Bias} > V_2^{Dark}$) J_N becomes dominant.

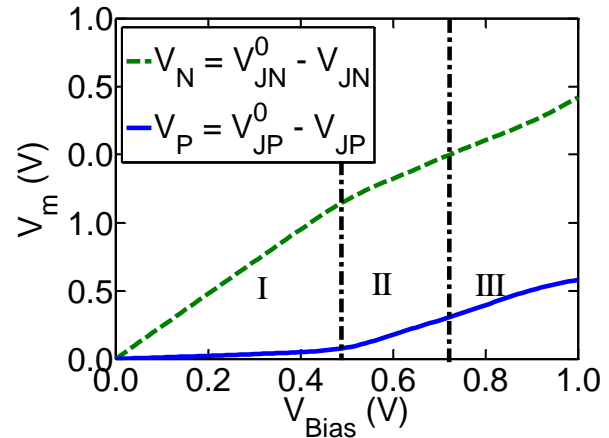


Fig. 5. The change in the band bending, V_m , across the a-Si and c-Si layers as a function of applied bias. The vertical lines separate the different bias regions.

set to 100 cm/s. The effect of the a-Si back surface field (BSF) that may exist in other solar cell designs is thus lumped into the s_b .

In Fig. 3, the dark current (J_{Dark}) along with the hole diffusion current (J_P) and electron diffusion current (J_N) at the front contact of the simulated P+/I/n heterojunction solar cell are plotted. The characteristic voltage features of a typical measured dark I-V curve in Fig. 2(a), (b) and (c) are captured by the simulated dark I-V characteristics in Fig. 3. In order to understand the different features, energy band diagrams at different applied biases (regions) are plotted in Fig. 4. The V_{JN} and V_{JP} represent the band bending in the c-Si and the a-Si regions, respectively. The change in the band bending from the equilibrium value between the a-Si and c-Si layer is given by

$$V_m = (V_{Jm}^0 - V_{Jm}), \quad (3)$$

where, $m = P$ for p-type (and intrinsic) a-Si, $m = N$ for n-type c-Si and V_{Jm}^0 is the equilibrium band bending. The band bending (V_m) across the a-Si and c-Si layers as a function of applied bias is plotted in Fig. 5.

It can be observed from Fig. 5 that nearly the entire voltage drop occurs across the n-type c-Si layer (V_N) for low voltage bias (region I). This occurs due to the screening effect of an inversion hole charge at the a-Si/c-Si interface. As a result, the energy band in a-Si region remains pinned with respect to the hole quasi-Fermi level, (see Fig. 4(b)). Hence, the hole concentration at the top of the valence band barrier is essentially voltage independent. Under these conditions, the dominant current transport mechanism is the J_P in the c-Si layer, as observed in Fig. 3.

As the bias voltage increases (region II), the voltage drop continues to increase across the c-Si, until the valence band on the c-Si neutral region aligns with the top of the hole barrier at the interface, as shown in Fig. 4(c). At this bias voltage ($V_{Bias} = V_1^{Dark}$), the J_P saturates as it is limited by the hole concentration at the top of the hole barrier at the interface: this saturation is reflected by n_{MFB} exceeding 2 [28]. At even higher bias voltages (region III), the inversion charge which was present at the interface at lower bias voltages begins to disappear, causing an almost equal partitioning of the applied voltage across the n-type c-Si and the p-type a-Si layers, as shown in Fig. 5. Under

these conditions, the dominant current component is dictated by the relative barrier heights for the electrons and holes. In this particular simulation it is observed that, the dominant transport mechanism is J_N into the a-Si (see Fig. 3) and n_{HFB} falls below 2. The ‘knee’ in the dark I-V at $V_{Bias} = V_2^{Dark}$ is a consequence of the change from hole dominated current to electron dominated current¹. Increasing the bias further introduces bulk series resistance effects.

The change in ideality factor – from $n_{LFB} < 2$ to $n_{MFB} > 2$ and back to $n_{HFB} < 2$ – with increasing applied bias is observed even in an ideal interface heterojunction and is a key signature for carrier transport in these devices. After introducing interface defects, these features are either enhanced or diminished due to changes in the electrostatics and carrier recombination rates dictated by the type of defect states. However, the essential features discussed in this section are still observed. The effects of defect states on the dark I-V will be analyzed later in section V.

III. PHYSICS OF CARRIER TRANSPORT UNDER ILLUMINATION

Using the dark I-V analysis, one might expect that the light I-V features can be explained by applying the classical superposition principle. However, using a novel simulation approach, we will show that the light I-V components (the contact injection current and the photo-current) have strong generation and voltage dependencies. Since, the superposition principle fails under these circumstances, a systematic understanding of individual light I-V features is essential.

A. Experimental Observations

The measured light I-V characteristics of sample A, studied in this paper are plotted along with the dark I-V characteristics in Fig. 6(a). It can be observed that the light I-V does not follow the principle of superposition due to rollover of the light I-V close to the maximum power point. Further, in Fig. 6(b), (c) and (d), the dark I-V and the light I-V characteristics obtained from [17] are plotted. In Fig. 6(b) and (c), the light I-V exhibits a strong voltage dependence which were referred to as ‘type-1’ and ‘type-2’ ‘S-type’ curves in [17] respectively. The light I-V in Fig. 6(b) and (c) also do not obey the superposition principle due to rollover of the light I-V close to the maximum power point.

However, in Fig. 6(d), the light I-V of ‘type-3’ sample (obtained from [17]) do exhibit adherence to superposition, at least up to V_{OC} and was referred to as a ‘good fill-factor’ sample in [17]. Further, there are several other studies in the literature that also do not report the occurrence of the ‘S-type’ curve in the light I-V [15].

Using a novel modeling approach, important insights into carrier transport under light I-V can be realized. This approach allows the injection current to be directly computed for a given illumination condition and is described in the following section.

¹Note that it is possible to have hole dominant current in high bias region as well. This depends on the exact a-Si process parameters, such as electron affinity. Suppression of electron current into a-Si region is possible by higher conduction band barrier. Under this scenario hole current from a-Si region is dominant and can exhibit exponential bias dependence.

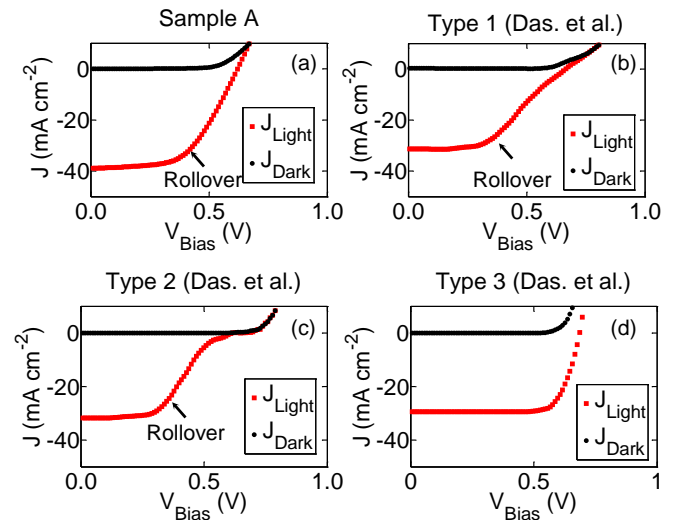


Fig. 6. The light I-V characteristics of sample A and those reported in [17] are plotted. Superposition principle does not hold for I-V plotted in (a), (b) and (c). Light I-V of type-1 and -2 indicate rollover in light I-V referred to as the S-type curve.

B. Numerical Simulation of the Light Current

Analyzing the light I-V inherently involves isolating two bias dependent and generation dependent current components of total current under light (J_{Light}), as follows:

$$J_{Light}(V, G) = J_{Inj}(V, G) + J_{Photo}(V, G), \quad (4)$$

where, J_{Inj} is the contact injection current, and J_{Photo} is the photo-current due to photon generation. A fundamental problem of analyzing the light I-V of measured devices is that these two components cannot be evaluated accurately using closed form expressions.

In order to overcome this challenge, we have developed a novel numerical method to de-convolve J_{Light} into its components, J_{Inj} and J_{Photo} . The implementation procedure for the numerical method is as follows.

A modification to the ADEPT 2.0 [26] simulation tool was used in this study to separate the J_{Light} into the J_{Inj} and the J_{Photo} . This modified drift-diffusion solver uses the following algorithm to determine the J_{Light} and J_{Inj} under illumination for a given generation rate profile ($G(x)$) and applied bias (V_{Bias}).

- 1) The solver calculates the hole density ($p_{Light}(x)$), the electron density ($n_{Light}(x)$) and the potential profile ($\phi(x)$) under illumination using the full drift-diffusion formalism. The J_{Light} can be calculated from the obtained $p_{Light}(x)$ and $n_{Light}(x)$.
- 2) The simulated $\phi(x)$ under illumination was frozen and the $G(x)$ is set to zero. The solver once again solves the continuity equations using the frozen $\phi(x)$ obtained from step 1 to calculate a new set of hole density ($p_{Inj}(x)$) and electron density ($n_{Inj}(x)$) profiles. The J_{Inj} was then calculated using the $p_{Inj}(x)$ and $n_{Inj}(x)$.
- 3) The J_{Photo} can be obtained from the J_{Light} and J_{Inj} using (4).

Note that steps 2 and 3 essentially fix the energy band and resolve the carrier density profiles for the contact-injected-carrier components of the total carrier density profiles.

Next, the analysis of these individual components is carried out using test structures to provide insights into the carrier

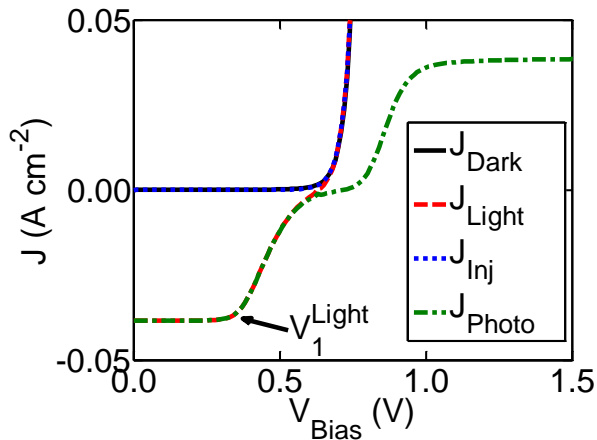


Fig. 7. The J_{Dark} , J_{Light} , J_{Inj} and J_{Photo} are plotted for a moderately doped emitter device ($N_A = 5 \times 10^{17} \text{ cm}^{-3}$). ‘S-type’ curve in J_{Light} due to voltage dependence of J_{Photo} . Note that the J_{Dark} , J_{Inj} overlap in the plotted region and J_{Light} , J_{Photo} overlap up to V_{OC} . The rollover in J_{Photo} starts to occur at $V_{Bias} = V_1^{Light}$.

transport under illumination. In order to analyze the J_{Light} , in terms of its individual components J_{Photo} and J_{Inj} , two a-Si/c-Si heterojunction test structures with different emitter doping ($N_A = 5 \times 10^{17} \text{ cm}^{-3}$ and $N_A = 5 \times 10^{18} \text{ cm}^{-3}$) were simulated. It should be noted that the dark and the light I-V features are also affected by other emitter properties such as valence band offset, a-Si band gap, etc., as discussed in [12] and [16], respectively. However, the essential features of individual components remain the same, hence only the emitter doping is used as a variable in this analysis. The simulations under illumination are carried out using AM 1.5G solar spectrum.

First, the behavior of J_{Photo} is analyzed to study the origin of non-ideal features, such as the S-type curve. J_{Photo} , along with J_{Dark} , J_{Inj} and J_{Light} , are plotted in Fig. 7 and Fig. 8 for the low and heavily doped emitter devices, respectively. It is clear from Fig. 7 that the J_{Photo} for the moderately doped emitter device has a strong bias dependence even below V_{OC} , and thus the superposition principle does not hold. This significant rollover in J_{photo} at $V_{Bias} = V_1^{Light} \sim 0.4 \text{ V}$, as shown in Fig. 7, can be explained by considering the corresponding energy band diagram at $V_{Bias} = 0.4 \text{ V}$ shown in Fig. 9. It is observed that the

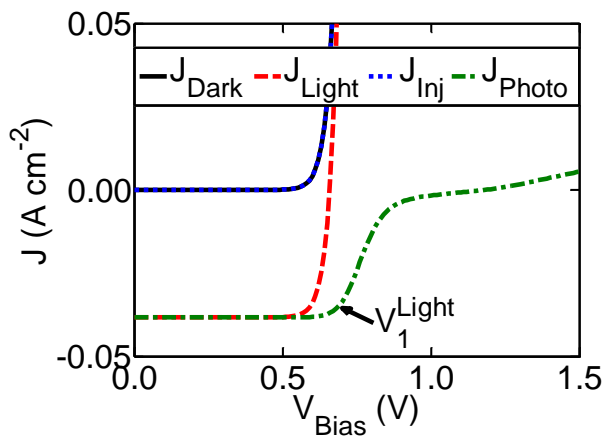


Fig. 8. The J_{Dark} , J_{Light} , J_{Inj} and J_{Photo} are plotted for a heavily doped emitter device ($N_A = 5 \times 10^{18} \text{ cm}^{-3}$). The J_{Photo} is bias independent at least up to V_{OC} . Note that the J_{Dark} , J_{Inj} overlap in the plotted region. The rollover in J_{Photo} starts to occur at $V_{Bias} = V_1^{Light}$.

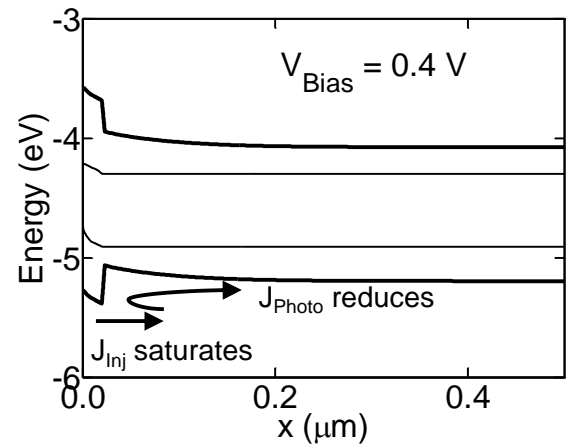


Fig. 9. Energy Band Diagram for moderately doped emitter device under illumination at $V_{Bias} = 0.4 \text{ V} \sim V_1^{Light}$. At this bias, the valence band offset acts as barrier for collection of photo generated carriers. Also, at this bias, loss of c-Si barrier causes saturation of J_{Inj} , which is hole current dominant.

valence band offset at the a-Si/c-Si interface acts as a barrier to the collection of photo generated carriers at the front contact. This observation can be quantified by plotting the position-resolved collection efficiency at different biases as in Fig. 10. This simulation involves counting the number of carriers that are collected at the front contact in response to an impulse of photo generated carriers at each position along the length of the device. Fig. 10 indicates close to 40% reduction in the collection efficiency from the c-Si absorber region at $V_{Bias} = 0.4 \text{ V}$ when compared to short circuit condition. For high forward bias ($V_{Bias} > 0.9 \text{ V}$, Fig. 7), the reversal of the J_{Photo} polarity is due to change in the direction of photo-generated carriers above the built-in voltage.

For a heavily doped emitter device, however, Fig. 8 indicates the J_{Photo} starts to rollover well above V_{OC} , at $V_{Bias} = V_1^{Light} \sim 0.7 \text{ V}$, indicating that superposition can be safely assumed for this device. Here, the magnitude of J_{Inj} which is equal to J_{Dark} dictates the shape of the I-V characteristic up to V_{OC} . The suppressed J_{Photo} at very high forward bias indicates a very high built-in voltage for this device.

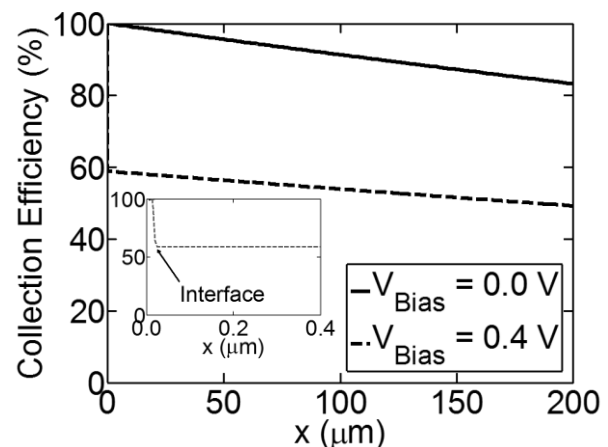


Fig. 10. The position dependent collection efficiency plot for a moderately doped emitter device under short circuit condition and at $V_{Bias} = 0.4 \text{ V}$. This shows a 40% reduction in collection efficiency for carriers generated in Si. The inset shows the reduction of the collection efficiency at the interface due to the a-Si/c-Si valence band offset which acts as a barrier for hole collection.

IV. CORRELATION OF DARK AND LIGHT I-V

A. Analysis of Simulation Results

The preceding discussion suggests a possible correlation between the dark I-V and the light I-V because both are controlled by the a-Si/c-Si potential barrier. In order to establish this correlation quantitatively, the behavior of J_{Inj} must be analyzed. J_{Inj} , which is essentially the “effective dark current under illumination,” will have the same features as those of the J_{Dark} . Thus, the insights developed in section II on the features of the dark I-V characteristics will be useful in analyzing the features of J_{Inj} . Next, it will be shown that J_{Inj} , which is obtained from light I-V simulations, can be correlated to the J_{Photo} discussed in section III. This correlation provides insights into the operation of these solar cells.

We will use the same test structures discussed in section III to analyze the essential features of J_{Dark} and J_{Inj} . J_{Inj} and J_{Dark} , for both moderately and heavily doped emitter structures, are plotted on a semi-log plot in Fig. 11 and Fig. 12, respectively. Observe that both J_{Dark} and J_{Inj} have the same essential features discussed in section II; indeed, V_1^{Light} and V_2^{Light} of J_{Inj} can be viewed as counterparts of V_1^{Dark} and V_2^{Dark} observed in J_{Dark} . Also, note that the V_1^{Light} , which represented the rollover of J_{Photo} (see Fig. 7 and Fig. 8), is the same as the one used here in Fig. 11 and Fig. 12. The justification for this will be provided once J_{Dark} and J_{Inj} are correlated.

For the moderately doped emitter device, the V_1^{Light} occurs at a lower bias voltage compared to that of V_1^{Dark} . As discussed in section II (for J_{Dark}), the saturation in J_{Inj} occurs when the valence band in the c-Si neutral region aligns with the top of the a-Si hole barrier as pointed out in Fig. 9. There is a considerable change in electrostatic potential profile under the illumination when compared to the dark, due to the presence of photo-generated carriers. This causes the early saturation of J_{Inj} when compared to J_{Dark} . However, this shift in V_1^{Dark} and V_1^{Light} is not observed in the heavily doped emitter device, indicating a negligible change in the potential profile under illumination when compared to the dark conditions. It is important to note that the photo-generated carriers in the device with lower V_1^{Dark} have a larger impact on the electrostatics of this device, thus causing a greater shift in V_1^{Light} to lower voltage biases.

The correlation between J_{Photo} and J_{Inj} is based on an important observation that the valence band at the top of the a-Si barrier aligns with that of the neutral c-Si region at $V_{Bias} = V_1^{Light}$. At this bias, both the saturation of J_{Inj} and the rollover of J_{Photo} occur (see Fig. 9 for a low emitter case). It can be observed for the moderately doped emitter device in Fig. 7 and Fig. 11 that the rollover of J_{Photo} and saturation of J_{Inj} occur at the same voltage bias. Further, this is also true for the heavily doped emitter device, as shown in Fig. 8 and Fig. 12.

B. Analysis of Experimental Results

Several distinctive features of the dark I-V and the light I-V such as the occurrence of high n_{MFB} above V_1^{Dark} , the occurrence of knee under dark conditions, the failure of superposition and the occurrence of S-type light I-V curve are explained using the numerical simulation framework in section II and III. Here, the dark I-V and the light I-V data measured during this study as well as those obtained from [17] are analyzed based on the

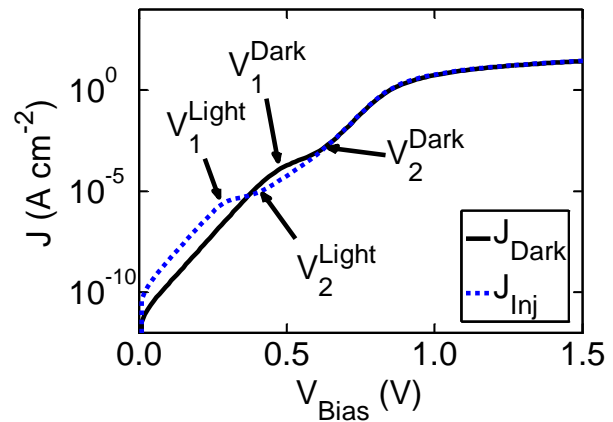


Fig. 11. The J_{Dark} and J_{Inj} are plotted for a low doped emitter device. The shift in V_1^{Light} from V_1^{Dark} indicate significant change in the c-Si band bending due to photo-generated carriers that results in the early saturation of low bias dominant hole current from the front contact.

theory developed in the preceding sections. It should be noted that, there may be significant processing differences among the samples considered. Despite these differences, it is possible to understand the general features of the experimental results based on the theoretical model discussed in the previous section.

From the sample A dark I-V measurement in Fig. 2(a), it can be observed that the low forward bias dark I-V has an ideality factor that changes continuously over the bias voltage, which could be due to the presence of interface defect states (discussed in section V). Hence, it is not possible to accurately estimate the V_1^{Dark} . However, the V_2^{Dark} can be estimated from the local maxima in the $d^2 \log(J)/dV^2$ versus V_{Bias} plot and was found to be around $V_2^{Dark} \sim 0.48$ V.

From the sample A light I-V measurement in Fig. 6(a), it can be observed that the light I-V has a weak bias dependence at very low biases ($V_{Bias} \sim 0.1$ V). However, a strong rollover starts to occur above $V_{Bias} \sim 0.3$ V, which suggests that the V_1^{Light} may be around the same voltage range based on the discussion in the earlier subsection which correlated the J_{Photo} and J_{Inj} .

From the dark I-V reported in [17], it can be observed that type-1 (see Fig. 2(b)) and type-2 (see Fig. 2(c)) samples exhibit

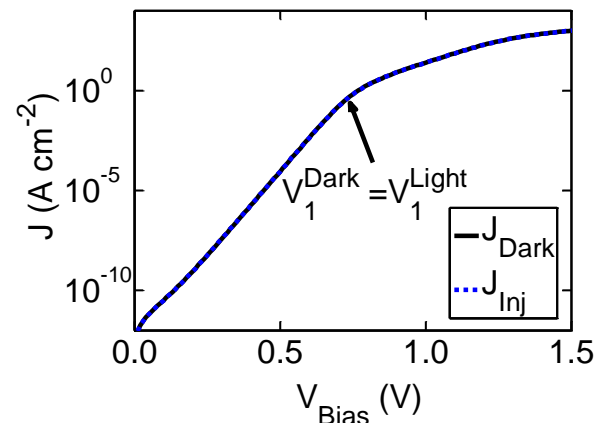


Fig. 12. The J_{Dark} and J_{Inj} are plotted for a high doped emitter device (overlap throughout the plotted bias range). No shift of V_1^{Light} from V_1^{Dark} indicate negligible impact of c-Si band bending due to photo-generated carriers.

a distinctive V_I^{Dark} , followed by a region with a very high ideality factor ($n_{MFB} > 2$) that can be attributed to J_P saturation. Further, the type-2 sample also exhibits a knee above which the ideality factor eventually returns to a value less than 2. This can be attributed to the change in the type of dominant minority carrier current (J_P to J_N), as expected from the analysis of dark I-V characteristics in section III. This knee is not observed in type-1 and type-3 (see Fig. 2(d)), presumably because of the high quality emitter and front contact properties that suppress J_N .

The light I-V characteristic of the type-1 sample (Fig. 6(b)) exhibits a rollover at relatively low bias and a strong S-type behavior which is correlated to the low V_I^{Dark} observed in the dark I-V (Fig. 2(b)) for this sample. The type 2 sample, which has V_I^{Dark} in the medium bias range in the dark I-V (Fig. 2(c)), also has a light I-V rollover (Fig. 6(c)) at around the same voltage range (V_I^{Light}). Finally, the type-3 sample, which has a near ideal dark I-V (Fig. 2(d)) with no V_I^{Dark} within the plotted range, exhibits no rollover (no V_I^{Light} observed) of light I-V (Fig. 6(d)) as well. Observably, the fill factor, FF , is very high for this case.

Now, it is also possible to correlate some of the other sets of measurements present in literature, such as, those reported in [15]. These samples do not indicate any sign of non-ideal features in the dark I-V and the light I-V most likely due to excellent process control, closely resembling the device with higher emitter doping discussed in section III.

V. DISCUSSION

At very low forward bias, apart from the multi tunneling capture emission phenomena [5] the dark I-V can be effected by the presence of interface defects. The effect of interface defects is discussed in this section for the sake of completeness. When defects are present in the a-Si/c-Si interface, there are two reasons for deviation of the dark I-V, namely, carrier recombination at the interface and change in electrostatics due to trapped charges. These two components can be studied separately using numerical simulation by considering, first, neutral traps ($D_{IT} = 10^{12} \text{ cm}^{-2}$) to see the effect of recombination current (J_{Rec}) and then using donor/acceptor like traps ($D_{IT} =$

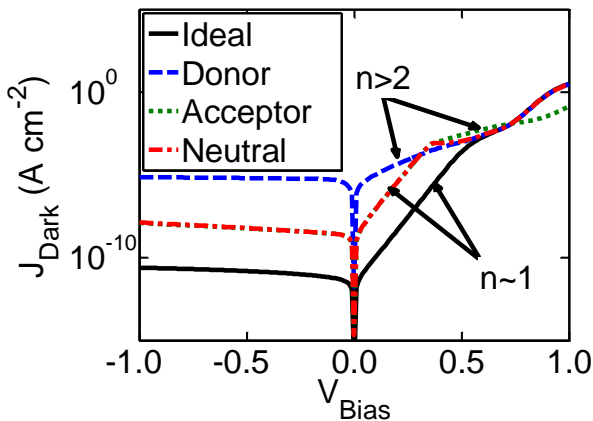


Fig. 13. Numerical dark I-V for an ideal structure along with non-ideal structure with defective a-Si/c-Si interface containing donor, acceptor and neutral traps with $D_{IT} = 10^{12} \text{ cm}^{-2}$ (Gaussian energy distribution around the mid-gap with $\sigma = 0.3 \text{ eV}$).

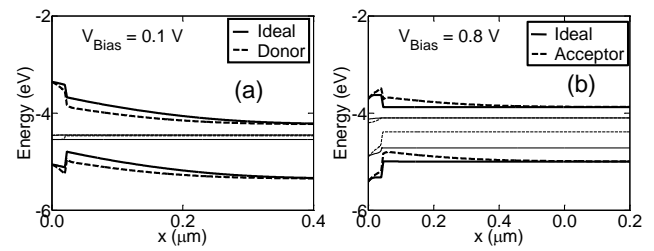


Fig. 14. Energy band diagram near the junction of an ideal structure along with a non-ideal structure with (a) donor-like traps at a-Si/c-Si interface at $V_{Bias} = 0.1 \text{ V}$, (b) acceptor-like traps at a-Si/c-Si interface at $V_{Bias} = 0.8 \text{ V}$.

10^{12} cm^{-2}) to capture the effects of change in electrostatics. The traps considered in this work have a Gaussian energy distribution around the mid-gap with $\sigma = 0.3 \text{ eV}$.

Upon introducing neutral defects, the reverse bias and low forward bias currents increase due to additional J_{Rec} (see Fig. 13). The ideality factor, however, remains below 2 for the low forward bias region and the high forward bias region. In the medium bias range, the saturation of J_P causes the ideality factor to increase beyond 2, as observed in an idealized defect-free device discussed in section II.

Donor traps at the a-Si/c-Si interface cause high currents in the reverse and low forward bias regions due to high J_{Rec} . It should be noted that the ideality factors in low forward bias in this case are *now considerably higher than 2*. This high ideality factor can be understood from the energy band diagram in Fig. 14(a). At low forward bias ($V_{Bias} \sim 0.1 \text{ V}$), on capturing the holes from the ‘inversion region’ at the interface, the positively charged donor states push the band downward. However, the hole carrier concentration at the top of the barrier on the a-Si side remains the same (notice the hole quasi Fermi level shifts along with the a-Si bands). This causes the early saturation of J_P as explained in section II. Hence, the twofold effect of charged defects, namely, increased low-bias dark current and high ideality factor, is due to high J_{Rec} and the change in c-Si barrier height in the presence of positively charged donor traps. Under high forward bias ($V_{Bias} > V_2^{Dark}$), the de-trapping of donor traps causes them to behave like neutral traps and the dominant diffusion current (J_N) makes the impact of J_{Rec} negligible.

On the other hand, acceptor-like traps are neutral in the reverse and low forward bias region ($V_{Bias} < V_I^{Dark}$), as there are few electrons to capture at the interface. The low bias ideality factor is less than 2 before it increases due to saturation of J_P . However, at high forward bias ($V_{Bias} > V_2^{Dark}$), the ideality factor is above 2 and the current deviates significantly from the ideal case. This can be understood from the energy band diagram at high forward bias, shown in Fig. 14(b). At high forward bias, the filled acceptor traps (which are negatively charged) push the bands upward. This causes an additional barrier to electrons from the c-Si to reach the a-Si layer, and thus the diffusion current J_N into the a-Si side is suppressed. Hence, at high forward bias the J_{Rec} and the saturated J_P continue to dominate over the J_N .

VI. CONCLUSIONS

The non-ideal effects of the dark I-V and the light I-V characteristics of (P+/I/n) a-Si/c-Si heterojunction solar cell are discussed. In the dark I-V, the unusually high ideality factors in

the medium bias regions, even in an otherwise ideal interface heterostructure, is attributed to J_P saturation. The V_2^{Dark} is observed when the dominant current transport shifts from J_P to J_N . High densities of defects at the a-Si/c-Si interface can introduce additional current due to interface recombination and shift the position of V_1^{Dark} and V_2^{Dark} by affecting the electrostatics.

A novel simulation method using a detailed numerical model to separate J_{Light} into its component parts, J_{Inj} and J_{Photo} , has been developed. The rollover in J_{Photo} in moderately doped emitter devices is due to the presence of a hole barrier at the a-Si/Si interface. It is shown that J_{Dark} , J_{Inj} and J_{Photo} are correlated in a fundamental way. The consequence of this correlation is that a device with a higher V_1^{Dark} has no shift in V_1^{Light} and has a voltage independent J_{Photo} up to V_1^{Light} . This avoids the rollover of the light I-V before V_{OC} and yields in a better FF.

Finally, based on the interpretation of the experimental results, it is shown that the dark I-V and the light I-V non-idealities indeed follow the theory presented in this paper. This correlation offers a fundamental insight regarding the importance of the heterojunction interface in designing highly efficient HITTM cells.

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REFERENCES

- [1] M. Tanaka, M. Taguchi, T. Matsuyama, T. Sawada, S. Tsuda, S. Nakano, H. Hanafusa, and Y. Kuwano, "Development of New a-Si/c-Si Heterojunction Solar Cells: ACJ-HIT (Artificially Constructed Junction-Heterojunction with Intrinsic Thin-Layer)," *Jpn. J. Appl. Phys.*, vol. 31, no. Part 1, No. 11, pp. 3518–3522, Nov. 1992.
- [2] K. Maki, D. Fujishima, H. Inoue, Y. Tsunomura, T. Asaumi, S. Taira, T. Kinoshita, M. Taguchi, H. Sakata, H. Kanno, and E. Maruyama, "High-efficiency HIT solar cells with a very thin structure enabling a high Voc," *Photovoltaic Specialists Conference (PVSC), 2011 37th IEEE*, pp. 57–61, 2011.
- [3] M. Taguchi, A. Yano, S. Tohoda, K. Matsuyama, Y. Nakamura, T. Nishiwaki, K. Fujita, and E. Maruyama, "24.7% Record Efficiency HIT Solar Cell on Thin Silicon Wafer," *IEEE J. Photovoltaics*, vol. PP, no. 99, pp. 1–4, 2013.
- [4] M. A. Green, K. Emery, Y. Hishikawa, W. Warta, and E. D. Dunlop, "Solar cell efficiency tables (version 40)," *Prog. Photovoltaics Res. Appl.*, vol. 20, no. 5, pp. 606–614, 2012.
- [5] H. Matsuura, T. Okuno, H. Okushi, and K. Tanaka, "Electrical properties of n-amorphous/p-crystalline silicon heterojunctions," *J. Appl. Phys.*, vol. 55, no. 4, pp. 1012–1019, Feb. 1984.
- [6] L. F. Marsal, J. Pallarès, X. Correig, J. Calderer, and R. Alcubilla, "Electrical characterization of n-amorphous/p-crystalline silicon heterojunctions," *J. Appl. Phys.*, vol. 79, no. 11, p. 8493, 1996.
- [7] N. Jensen, U. Rau, R. M. Hausner, S. Uppal, L. Oberbeck, R. B. Bergmann, and J. H. Werner, "Recombination mechanisms in amorphous silicon/crystalline silicon heterojunction solar cells," *J. Appl. Phys.*, vol. 87, no. 5, pp. 2639–2645, Mar. 2000.
- [8] M. Taguchi, E. Maruyama, and M. Tanaka, "Temperature Dependence of Amorphous/Crystalline Silicon Heterojunction Solar Cells," *Jpn. J. Appl. Phys.*, vol. 47, no. 2, pp. 814–818, Feb. 2008.
- [9] B. Jagannathan, W. A. Anderson, and J. Coleman, "Amorphous silicon/p-type crystalline silicon heterojunction solar cells," *Sol. Energy Mater. Sol. Cells*, vol. 46, no. 4, pp. 289–310, Jul. 1997.
- [10] T. H. Wang, E. Iwaniczko, M. R. Page, D. H. Levi, Y. Yan, H. M. Branz, and Q. Wang, "Effect of emitter deposition temperature on surface passivation in hot-wire chemical vapor deposited silicon heterojunction solar cells," *Thin Solid Films*, vol. 501, no. 1–2, pp. 284–287, Apr. 2006.
- [11] Y. J. Song, M. R. Park, E. Gulians, and W. A. Anderson, "Influence of defects and band offsets on carrier transport mechanisms in amorphous silicon/crystalline silicon heterojunction solar cells," *Sol. Energy Mater. Sol. Cells*, vol. 64, no. 3, pp. 225–240, Oct. 2000.
- [12] R. V. K. Chavali, J. R. Wilcox, B. Ray, J. L. Gray, and M. A. Alam, "A Diagnostic Tool for Analyzing the Current-Voltage Characteristics in a-Si / c-Si Heterojunction Solar Cells," in *Photovoltaic Specialists Conference (PVSC), 2013 39th IEEE*, 2013, vol. 1.
- [13] U. Das, S. Bowden, M. Burrows, S. Hegedus, and R. Birkmire, "Effect of Process Parameter Variation in Deposited Emitter and Buffer Layers on the Performance of Silicon Heterojunction Solar Cells," *Photovoltaic Energy Conversion, Conference Record of the 2006 IEEE 4th World Conference on*, vol. 2, pp. 1283–1286, 2006.
- [14] T. F. Schulze, L. Korte, E. Conrad, M. Schmidt, and B. Rech, "High-forward-bias transport mechanism in a-Si:H/c-Si heterojunction solar cells," *Phys. status solidi*, vol. 207, no. 3, pp. 657–660, 2010.
- [15] T. F. Schulze, L. Korte, E. Conrad, M. Schmidt, and B. Rech, "Electrical transport mechanisms in a-Si:H/c-Si heterojunction solar cells," *J. Appl. Phys.*, vol. 107, no. 2, p. 023711, 2010.
- [16] M. Lu, U. Das, S. Bowden, S. Hegedus, and R. Birkmire, "Optimization of interdigitated back contact silicon heterojunction solar cells: tailoring hetero-interface band structures while maintaining surface passivation," *Prog. Photovoltaics Res. Appl.*, vol. 19, no. 3, pp. 326–338, May 2011.
- [17] U. Das, S. Hegedus, L. Zhang, J. Appel, J. Rand, and R. Birkmire, "Investigation of hetero-interface and junction properties in silicon heterojunction solar cells," in *Photovoltaic Specialists Conference (PVSC), 2010 35th IEEE*, 2010, pp. 1358–1362.
- [18] Q. Wang, "High-efficiency hydrogenated amorphous/crystalline Si heterojunction solar cells," *Philos. Mag.*, vol. 89, no. 28–30, pp. 2587–2598, Oct. 2009.
- [19] Z. Shu, U. Das, J. Allen, R. Birkmire, and S. Hegedus, "Experimental and simulated analysis of front versus all-back-contact silicon heterojunction solar cells: effect of interface and doped a-Si:H layer defects," *Prog. Photovoltaics Res. Appl.*, p. n/a–n/a, Jun. 2013.
- [20] A. Kanevce and W. K. Metzger, "The role of amorphous silicon and tunneling in heterojunction with intrinsic thin layer (HIT) solar cells," *J. Appl. Phys.*, vol. 105, no. 9, p. 094507, 2009.
- [21] K. Ghosh, S. Bowden, and C. Tracy, "Role of hot carriers in the interfacial transport in amorphous silicon/crystalline silicon heterostructure solar cells," *Phys. status solidi*, vol. 210, no. 2, pp. 413–419, 2013.
- [22] U. K. Das, M. Z. Burrows, M. Lu, S. Bowden, and R. W. Birkmire, "Surface passivation and heterojunction cells on Si (100) and (111) wafers using dc and rf plasma deposited Si:H thin films," *Appl. Phys. Lett.*, vol. 92, no. 6, p. 063504, 2008.
- [23] S. Dongaonkar, J. D. Servaites, G. M. Ford, S. Loser, J. Moore, R. M. Gelfand, H. Mohseni, H. W. Hillhouse, R. Agrawal, M. A. Ratner, T. J. Marks, M. S. Lundstrom, and M. A. Alam, "Universality of non-Ohmic shunt leakage in thin-film solar cells," *J. Appl. Phys.*, vol. 108, no. 12, p. 124509, 2010.
- [24] S. Dongaonkar, K. Y. D. Wang, M. Frei, S. Mahapatra, and M. A. Alam, "On the Nature of Shunt Leakage in Amorphous Silicon p-i-n Solar Cells," *IEEE Electron Device Lett.*, vol. 31, no. 11, pp. 1266–1268, Nov. 2010.
- [25] S. Dongaonkar and M. A. Alam, "PV Analyzer," Mar-2011. [Online]. Available: <https://nanohub.org/resources/11073>.
- [26] J. L. Gray, X. Wang, X. Sun, and J. R. Wilcox, "ADEPT 2.0," Mar-2011. [Online]. Available: <http://nanohub.org/resources/10913>.
- [27] "Material Data - Silicon Materials," 2012. [Online]. Available: http://www.ampsmodeling.org/materialData_silicon.html.
- [28] R. L. Anderson, "Experiments on Ge-GaAs heterojunctions," *Solid State Electron.*, vol. 5, no. 5, pp. 341–351, Sep. 1962.



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