An amorphous oxide semiconductor thin-film transistor route to oxide electronics

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Abstract

Amorphous oxide semiconductor (AOS) thin-film transistors (TFTs) invented only one decade ago are now being commercialized for active-matrix liquid crystal display (AMLCD) backplane applications. They also appear to be well positioned for other flat-panel display applications such as active-matrix organic light-emitting diode (AMOLED) applications, electrophoretic displays, and transparent displays. The objectives of this contribution are to overview AOS materials design; assess indium gallium zinc oxide (IGZO) TFTs for AMLCD and AMOLED applications; identify several technical topics meriting future scrutiny before they can be confidently relied upon as providing a solid scientific foundation for underpinning AOS TFT technology; and briefly speculate on the future of AOS TFTs for display and non-display applications.

Keywords – Oxide electronics, amorphous oxide semiconductor (AOS), thin-film transistor (TFT), flat-panel displays, indium gallium zinc oxide (IGZO), active-matrix liquid crystal display (AMLCD), active-matrix organic light-emitting diode (AMOLED)

1. Introduction

Oxide electronics is a very diverse and active field, encompassing materials such as dielectrics, ferroelectrics, magnetics, piezoelectrics, multiferroics, high-temperature superconductors, epitaxial oxides, memories, and/or sensors. These materials find interest and application in a myriad of devices ranging from high-density memories to large-scale sensor arrays. In this contribution, we focus on a branch of oxide electronics that often employs monikers such as 'oxide thin-film transistors' or 'oxide TFTs'. This topic can be further subcategorized by specifying whether the microstructure of the TFT channel layer is amorphous or polycrystalline. We will confine our attention to a specific class of amorphous channel layer materials, amorphous oxide semiconductors (AOS).

Our AOS TFT topical choice is primarily motivated by flat-panel display considerations. The dominant flat-panel display technology – active-matrix liquid crystal display (AMLCD) – would benefit from a higher performance channel layer replacement for amorphous hydrogenated silicon (a-Si:H), as is currently used in switching TFTs for backplane pixels. Such a replacement, however, should not entail a substantial cost penalty. AOS TFTs are very attractive candidates for a-Si:H TFT replacement. The amorphous nature of an AOS TFT is a key advantage. Using the success of a-Si:H TFTs as a guide, amorphous materials are more readily and economically scaled to the exceedingly large dimensions (~9 m^2) required for AMLCD high-volume manufacturing. As AOS TFTs are successfully integrated into AMLCD backplanes, other flat-panel display applications such as organic light-emitting diodes, electrophoretic displays, and transparent displays may well follow. While AOS TFT development is currently driven

by the needs of the flat-panel display industry, other large-area or conventional silicon-based electronics applications could emerge, depending on the performance, reliability, and manufacturability of AOS TFTs as established by their use in commercial displays.

This paper is organized as follows. Section 2 is devoted to AOS materials design considerations that motivate the emergence of indium gallium zinc oxide (IGZO) as the current AOS commercial material-of-choice and provide a framework for undertaking future AOS material selection and design. In Section 3, the case for IGZO TFT implementation into next-generation AMLCDs is presented. In Section 4, the more challenging task of employing IGZO TFTs into AMOLEDs is addressed. In Section 5, several questions are posed for the AOS research community regarding fundamental scientific/technical issues that, in our view, are not resolved and need to be more adequately addressed. In Section 6, we offer conclusions and perspectives on the future of AOS technology for display and other emerging applications.

2. Amorphous oxide semiconductor (AOS) design

The portion of the periodic table, highlighted in Fig. 1, was proposed by Hosono *et al.* in 1996 as a starting point for choosing multicomponent combinations of cations for the design of AOS [1]. Prior to initiating a discussion of AOS design, two historical footnotes are warranted. First, these AOS guidelines were originally formulated for the design of transparent conductive oxides (TCOs) in contrast to their application as TFT channel materials per the focus of our discussion here. The notion of using these prospective TCO materials in a TFT channel application was in fact quite non-obvious, as witnessed by the nearly one decade delay before the first AOS based TFTs were

demonstrated. The desirable traits for a candidate TCO material are substantially different than those for an AOS channel material, given the nature and constraints of their respective applications, and the recognition of the potential for high-performance AOS based TFTs in the early 2000's generated a great deal of excitement in the technical community. Second, in early publications, AOS materials designed according to Fig. 1 guidelines were referred to as amorphous multicomponent heavy-metal cation oxides. Since 'heavy metal' connotes toxicity in conventional English usage, today these materials are referred to as AOS.

11	12	13	14	15	
29 Cu 63.54	30 Zn 65.37	31 Ga 69.72	32 Ge 72.59	33 As 74.92	4
47 Ag 107.87	48 Cd 112.40	49 In 114.82	50 Sn 118.69	51 Sb 121.75	5
79 Au 196.97	80 Hg 200.59	81 Tl 204.37	82 Pb 207.19	83 Bi 208.98	6

Fig. 1 The portion of the periodic table for selecting amorphous oxide semiconductor cations. Color coding: blue = most common cations employed in AOS design, red = toxic; brown = p-type cations; orange = high cost cations; black = largely uninvestigated.

Returning to AOS design, Hosono *et al.* advocated selecting cations from the portion of the periodic table shown in Fig. 1 since materials, designed using such cations, possess conduction bands derived from large ionic-radius, spherically symmetric 4s, 5s, or 6s electron orbitals [1]. These orbitals lead to a high degree of wave-function overlap,

electron delocalization, and relatively high electron mobility, independent of whether the microstructure is crystalline or amorphous. Simple binary oxides such as ZnO, SnO_2, and In_2O_3 have a strong tendency to crystallize. This can be circumvented by specifying that cations selected from the portion of the periodic table shown in Fig. 1 should be combined in multicomponent systems to confuse the lattice as to which structure type to adopt, thereby frustrating crystallization. The simplicity and viability of these design guidelines has contributed greatly to the success of AOS.

Now consider implications of the elemental color-coding scheme adopted in Fig. 1. Of the fifteen elements proposed in Fig. 1, five of them (As, Cd, Hg, Tl, Pb; red) are avoided by most researchers because of their toxicity, three of them (Cu, Ag, Au; brown) are possibly useful for the design of a p-type semiconductor (since our current emphasis is on n-type AOS design, these elements will be eliminated from further consideration), and three of them (Ge, Ag, Au; orange) are less attractive options because of their high cost. Eliminating these elements from further consideration, six elements remain of the initial fifteen. Four of them (Zn, Ga, In, Sn) are colored blue; they are the elements most commonly used in AOS design. The other two (Sb, Bi; black) may eventually prove to be appropriate AOS cation choices, but their usefulness has apparently not yet been validated in the literature. Further inspection of the detailed color-coding scheme employed in Fig. 1 reveals that cost is also of some concern with respect to Ga and In, while In is sometimes classified as toxic. Since cost is often related to elemental abundance and/or world-wide production, these properties as well as toxicity are compared in Table 1 for the four most common AOS cations. It is very clear from Table

1 that Zn and Sn are the two most attractive AOS cation choices from the perspective of abundance, cost, world-wide production, and toxicity.

Table 1 Abundance, cost, production volume, and toxicity of the most common amorphous oxide semiconductor cations.

Element	**Abundance (Earth's Crust ppm by mass) [2]**	**Cost ($/ton 2006) [3]**	**World-wide Production (tons/year) [3]**	**Toxic? [4]**
Ga	2	443,000	73	no
In	0.0002	918,000	581	yes
Sn	0.2	12,500	302,000	no
Zn	8	3,500	9,520,000	no

Briefly, we now constrain our AOS design discussion to the use of Ga, In, Sn, and/or Zn cations for TFT channel layer applications [5-8]. The past decade of intense worldwide research has established a framework whereby the contribution of each of these cations to overall AOS TFT channel performance can be nicely rationalized. In, Sn, and Zn are intriguing AOS design starting points since their binary oxides – In_2O_3, SnO_2, and ZnO – are the three most commonly used TCOs. The small effective masses and corresponding relatively high mobilities of these oxides are valued for both TCO and AOS applications. However, TCO applications require high electron concentrations ($\sim 10^{20}$-10^{21} cm^{-3}), whereas an optimized AOS for use as a TFT channel layer must have a small electron concentration, preferably $<10^{16}$ cm^{-3}. Incorporation of In and/or Sn (to a lesser extent) in an AOS tend to increase the electron concentration. In contrast, inclusion of Zn and especially of Ga will lead to a suppression of the electron concentration. Unfortunately, use of Ga in an AOS also tends to reduce its mobility.

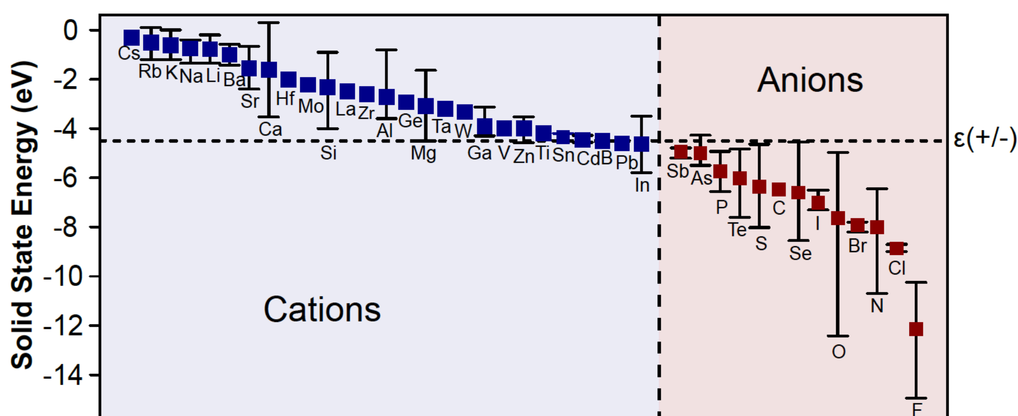

Fig. 2 Solid-state energy (SSE) values for 60 elements arranged in descending energy order. SSE is assessed as an average electron affinity EA (for a cation, shown in blue) or an average ionization potential IP (for an anion, shown in red) for binary compounds having the atom under consideration as a constituent. The variability bar included for some elements corresponds to the range of EA or IP reported in the SSE data base [9,10]. Reprinted with permission from B. D. Pelatt, R. Ravichandran, J. F. Wager, and D. A. Keszler, J. Am. Chem. Soc., 2011 133 (42), pp. 16852-16860. Copyright (2011) American Chemical Society.

The tendency for a given cation in an AOS to increase or suppress the electron carrier concentration can be rationalized by reference to the atomic solid-state energy (SSE) scale given in Fig. 2 [9,10]. The SSE for a given element constitutes an estimate of its frontier orbital energy position with respect to the vacuum level when it is incorporated into an inorganic solid. Cation and anion behavior are distinguished by the SSE position with respect to -4.5 eV, a universal energy reference corresponding to the hydrogen donor/acceptor ionization energy [ε(+/-)] or, equivalently, to the standard

hydrogen electrode (SHE) potential of electrochemistry as measured with respect to the vacuum level. Because SSE for a cation equates to the average electron affinity (EA) of a series of binary compounds, it is important to note that the EAs for In_2O_3, SnO_2, and ZnO are reported to fall in the range of -4.4 to -4.6 eV. These values are positioned very near ε(+/-), an energy where electron doping is energetically favorable. For Ga_2O_3, however, EA = -3.1 eV, i.e., it is energetically separated from ε(+/-) by 1.4 eV. At this energy, Ga becomes an electron-suppressing cation. These SSE trends are also consistent with the occasional use of Al and Hf in AOS as electron-suppressing cations [11-13], since SSE (Al) = -3.1 eV and SSE (Hf) = -2.0 eV are energetically positioned well above ε(+/-).

In addition to mobility-enhancing/degrading and electron-creating/suppressing tendencies, two other cation properties may be relevant for future AOS selection/design purposes. First, the wet etching characteristics of an AOS contribute to its process integration compatibility when it is used in a thin film. Ga, In, and especially Zn are easily etched by wet methods, Sn can present significant challenges. Thus, if an application requires increased selectivity in which the AOS is made harder to etch, the addition of Sn is likely. Second, since Ga and In melt at very low temperatures (30 and 150 °C, respectively) compared to Sn and Zn (232 and 420 °C, respectively) it is unlikely that Ga- or In-containing metal sputter targets can be fabricated. Thus, sputtering of Ga- or In-containing AOS will require the use of ceramic targets. In contrast, ZTO sputtering can be accomplished via reactive sputtering using a metal target.

Based on these guidelines, AOS designs using Ga, In, Sn, and/or Zn can be comprehensively categorized as follows, recognizing that variable relative concentrations

are possible once cation constituents have been identified. The emphasis here is on TFT channel layer applications in which the electron concentration must be reduced to as low a level as possible. Two-cation designs involving IGO, TGO, or ZGO are expected to have lower electron concentrations compared to ZIO and ZTO since the electron suppressing properties of Ga are known to be superior to those of Zn. The role of Ga is clearly to suppress the electron concentration in IGO, TGO, or ZGO whereas the role of Zn is less clear in ZIO and ZTO since Zn may be a mobility enhancer as well as an electron concentration suppressor. ITO is not expected to be a useful two-cation design channel layer since it lacks an electron suppressing constituent cation. Three-cation designs involving IGZO, IGTO, and TGZO are expected to have lower electron concentrations than ZITO, once again due to the superior electron suppression properties of Ga compared to Zn. Only one three-component AOS – IGZTO – is possible for the design constraints currently under consideration. Of the eleven compositions specified, IGZO with an $InGaZnO_4$ composition is the current consensus champion [14-17], and it is currently being commercialized. Thus, for the remainder of this review, until the conclusions section, our AOS discussion will focus on IGZO.

3. Active-matrix liquid crystal display (AMLCD) thin-film transistor (TFT) backplane technology options

The architecture of an AMLCD backplane pixel is very simple, consisting of a single voltage-controlled switch. Usually a TFT switch is used to set the optical state of an AMLCD pixel, although this can also be accomplished using single or dual diodes

[18]. Three AMLCD TFT technology options – a-Si:H [19], low-temperature polysilicon (LTPS) [20], and IGZO – are compared in Table 2.

Table 2 Comparison of amorphous hydrogenated silicon (a-Si:H), low-temperature polysilicon (LTPS), and indium gallium zinc oxide (IGZO) thin-film transistors for active-matrix liquid crystal display (AMLCD) applications. Color coding: blue = good, red = bad; green = intermediate

Property	**a-Si:H**	**LTPS**	**IGZO**
Microstructure	amorphous	polycrystalline	amorphous
V_T uniformity	good	fair*	fair*
V_T stability	poor	good	fair
Mobility	~ 1 $cm^2V^{-1}s^{-1}$	~ 50-100 $cm^2V^{-1}s^{-1}$	~ 10-30 $cm^2V^{-1}s^{-1}$
Mobility Uniformity	good	fair*	fair*
Device type	NMOS	CMOS	NMOS
Process complexity	low	high	low

*LTPS V_T and mobility uniformity are limited by intrinsic material properties associated with grain size variation amongst devices; in contrast, IGZO uniformity is determined by sputter process control (and probably associated processes such as PECVD dielectric deposition, annealing, and so on) which have not yet been optimized to the level of sophistication needed for the demands of the IGZO channel material application.

From the inception of AMLCD technology until today, a-Si:H has been the AMLCD backplane workhorse. a-Si:H is used for AMLCD applications since it is has adequate performance, process simplicity, the lowest cost, and can be readily scaled to large-area, meter-size dimensions. Three significant a-Si:H advantages highlighted in Table 2 – threshold voltage (V_T) uniformity, mobility uniformity, and process complexity – are direct consequences of the amorphous microstructure of a-Si:H. Of the three a-Si:H liabilities listed in Table 2 – poor stability, poor mobility, and NMOS – mobility is the most important consideration in precluding the use of a-Si:H for upcoming AMLCD commercial applications since its mobility is inadequate for the higher anticipated refresh rates required for future products, and limits the ability to reduce TFT size as needed for small pixels in high-resolution mobile displays.

Until recently, LTPS was universally regarded as the obvious heir-apparent to a-Si:H when its mobility performance was deemed inadequate for emerging display applications. In terms of mobility performance, LTPS is the clear winner in Table 2. Additionally, LTPS TFTs have much better stability than a-Si:H TFTs. Finally, the availability of CMOS using LTPS means that row and column drivers or other peripheral circuits can be integrated onto the glass substrate, an attractive option. With all of these performance advantages, and despite the substantial penalty in process complexity (and ultimately cost), the case for transitioning from a-Si:H to LTPS for high-performance (and high-value) display applications seemed inevitable.

Except for the emergence of IGZO, IGZO does not have the virtue of offering CMOS as an option for peripheral circuit integration. Nor does it have as high an electron mobility as LTPS. However, it is *amorphous*. This is critical. Being amorphous, it

possesses the same inherent manufacturing/scaling/cost advantages as a-Si:H involving threshold voltage (V_T) uniformity, mobility uniformity, and process simplicity. Also like a-Si:H, IGZO processing is simple. IGZO source/drain contacts can be formed directly by simply patterning the contact metal (or TCO) directly onto an IGZO channel layer. No channel layer contact doping or deposition of an additional doped contact layer between source/drain and active channel is required to form low resistance source/drain contacts, as is the case for a-Si:H and LTPS. This simplifies IGZO processing, potentially eliminating one or more process steps. However, IGZO surfaces tend to be highly sensitive so that development of a back-channel etch process such as that currently used in advanced a-Si:H TFT manufacturing appears to be challenging. First-generation IGZO technology will be implemented using etch-stop processing, thus requiring an extra masking step compared to that of advanced a-Si:H TFT processing, but still fewer than required for an LTPS TFT process.

In assessing the case for choosing between LTPS or IGZO as a replacement for a-Si:H AMLCD applications, the elephant-in-the-room is a-Si:H process compatibility. For a relatively modest capital investment, an operating a-Si:H TFT fab (perhaps operating below capacity or in the queue for mothballing) can be retrofitted for IGZO by replacing the a-Si:H PECVD channel layer process with PVD IGZO and the SiN_x PECVD gate dielectric process with PECVD SiO_2. With a few exceptions, the a-Si:H and IGZO process flows will look quite similar, having comparable process complexity. Because of the amorphous microstructural nature of IGZO, scaling-to-larger-area-substrates considerations are expected to be similar also, as are cost and yield. If, as expected, the converted IGZO line enables production of high-end displays, the relatively high margins

associated with this type of shift in factory output are an attractive prize in the largely commoditized LCD business.

This is not true when considering LTPS as a possible replacement for a-Si:H. LTPS processing is distinctly different, generally requiring construction of a new fab rather than retrofit of an existing a-Si:H plant. This is an important consideration. LTPS processing is more complex than a-Si:H / IGZO processing, typically requiring several additional masking steps. Elevated temperatures are often necessary for channel dehydrogenation, channel crystallization, dopant activation, and/or interface state control [20]. Channel crystallization is normally accomplished by excimer laser annealing (ELA) which in addition to adding cost comprises a major challenge in scaling to the large glass substrate dimensions necessary for efficient production of TV size backplanes (although we do not dismiss the legitimate efforts underway, notably by Samsung, to work through this challenge). LTPS S/D doping and patterning is more complicated since dopants must be selectively implanted and activated rather than simply incorporated into a doped PECVD layer as accomplished in a-Si:H processing. A lightly-doped drain (LDD) or gate-overlapped LDD (GOLDD) TFT architecture is typically used in order to reduce leakage, adding to LTPS processing complexity. Many of these process steps are not readily scalable to larger substrate dimensions.

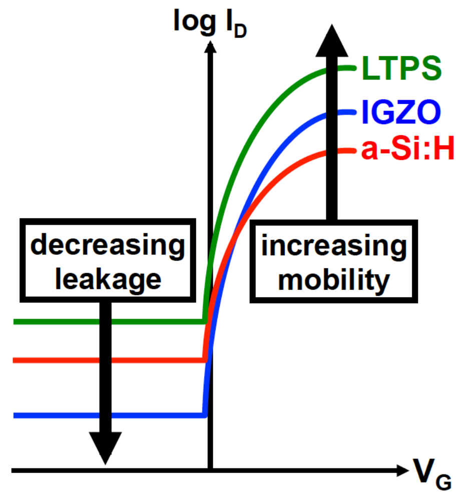

Fig. 3 Idealized drain current – gate voltage [log (I_D) – V_G] transfer curve comparison of amorphous hydrogenated silicon (a-Si:H; red), indium gallium zinc oxide (IGZO; blue), and low-temperature polysilicon (LTPS; green) thin-film transistors.

A compelling case for selecting IGZO instead of LTPS as an a-Si:H replacement was put forward recently by Sharp and may be developed with the assistance of Fig. 3 [21]. Figure 3 shows an idealized comparison of log (I_D) – V_G transfer curves for a-Si:H, IGZO, and LTPS TFTs. As indicated in Fig. 3, increasing mobility and decreasing leakage are two primary transfer curve considerations that determine the suitability of a TFT for an AMLCD switching application.

Until recently, mobility considerations have been primarily emphasized when assessing a channel layer for AMLCD TFT switching applications. In terms of mobility, LTPS is the clear winner (see Table 1), although IGZO offers significant mobility improvement compared to a-Si:H. A higher channel layer mobility is attractive since (i) TFTs may be reduced in physical size and yet still supply the required current, thereby reducing the pixel fill factor, thus reducing backlight power and improving power

efficiency (especially important for battery-powered mobile devices); and (ii) the TFT response time will be faster due to reduced parasitic capacitance, enabling increased display refresh rate for sharper moving images and additional content options such as 3D.

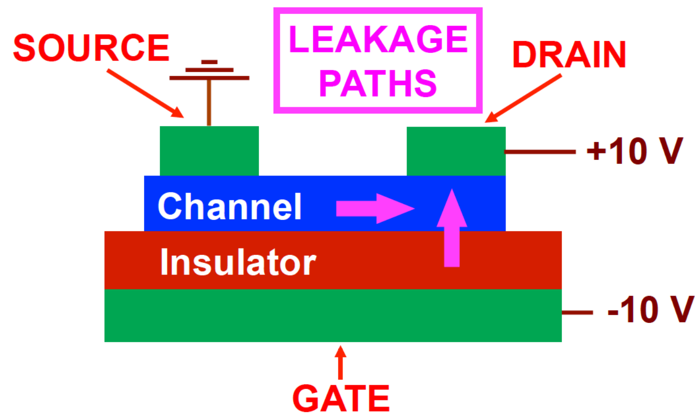

Fig. 4 Arrows indicating the directions of electron flux for the primary leakage paths giving rise to the off-state drain current leakage in a bottom-gate TFT. The horizontal (vertical) arrow corresponds to channel (gate insulator) leakage.

As indicated in Fig. 3, off-state drain current leakage considerations are also pertinent when evaluating a TFT for its suitability for AMLCD switching. Figure 4 clarifies that there are two primary contributions to off-state drain current leakage, involving leakage in the channel and/or through the gate insulator.

In terms of off-state drain current leakage, IGZO is the clear winner. IGZO TFTs have lower leakage across the channel because IGZO is a wide band gap [i.e., E_G(IGZO)= 3.25 eV] unipolar semiconductor. In contrast, LTPS and a-Si:H have significantly narrower band gaps [i.e., E_G(LTPS)= 1.1 eV, E_G(a-Si:H)= 1.7 eV] and are

bipolar so that channel inversion occurs at sufficiently large reverse gate bias. Under reverse bias operation, leakage through the gate insulator may also constitute a significant contribution to the measured off-state drain current leakage. IGZO TFTs tend to have relatively low gate leakage since they employ a high-quality SiO_2 gate insulator (superior to that of SiN_x used in a-Si:H TFTs) and they have smooth surfaces so that a uniform electric field develops across the gate insulator / IGZO interface (not the case for LTPS since grains give rise to pronounced roughness at an insulator / LTPS interface). A lower leakage is desirable since (i) less power is dissipated when a TFT is off; (ii) the TFT switch can retain internal pixel charge for a longer period of time so that display refresh rate may be reduced, leading to: (a) reduced power dissipation; and (b) improved touch capability (due to less noise / interference with touch detection since the display refresh and touch-sensing cycles may be interleaved rather than run simultaneously).

To a large extent, the superior off-state drain current leakage characteristics of IGZO are a consequence of its large band gap compared to LTPS and a-Si:H. A quantitative argument for this correlation between wide band gap and low off-state drain current leakage may be formulated as follows. For a TFT with a perfect gate insulator (i.e., no gate insulator leakage), a lower limit estimate of channel leakage is given by [22]

$$J_R = \frac{q n_i t_{channel}}{\tau_g} + q\, n_i s_g, \tag{1}$$

where q = electron charge, n_i = intrinsic carrier concentration, $t_{channel}$ = channel layer thickness, τ_g = generation lifetime, and s_g = surface generation velocity. The key term in Eq. 1 is the intrinsic carrier concentration since it is equal to

$$n_i = \sqrt{N_C N_V} e^{-\frac{E_G}{2k_B T}}, \tag{2}$$

where N_C (N_V) is the effective conduction (valence) band density of states, k_B is Boltzmann's constant, and T is temperature. Given that the band gap is in the exponential in Eq. 2, its influence dominates in establishing both the intrinsic carrier concentration and the off-state leakage characteristics as per Eq. 1. Since the intrinsic carrier concentration of IGZO is approximately 18 orders of magnitude smaller than that of LTPS, the channel current contribution to the off-state drain current leakage is negligibly small for IGZO compared to LTPS. In fact, it is often difficult to unambiguously distinguish between gate and channel leakage in an IGZO TFT because the channel leakage is so small that displacement current artifacts and the lack of being able to establish charge neutrality due to fact that IGZO is a relaxation semiconductor (see Section 5.1) makes such assessment problematic.

An Eq. 1 comparison of the off-state drain current leakage properties of IGZO and LTPS is a somewhat misleading since it does not account for the possibility of inversion layer formation under reverse gate bias and its deleterious effects with respect to leakage. In a relatively narrow band gap semiconductor such as LTPS an inversion layer is readily formed under a reverse gate bias since only a modest surface potential excursion of 0.6 V is required to achieve strong inversion for 10^{15} cm^{-3} n-type doping. Once an inversion layer is formed, the off-state drain current leakage characteristic is dominated by the inversion layer so that the leakage current increases exponentially with increasing reverse bias. In contrast, for identical n-type doping the surface potential would have to be modulated 2.75 V in order to reach strong inversion in IGZO! These as well as other chemical and physical considerations indicate that the formation of an inversion layer in

an IGZO TFT channel is highly improbable under normal device conditions. This is a key advantage of IGZO, in terms of off-state drain current leakage.

In summary, it appears that IGZO is moving very quickly towards commercialization as a replacement for a-Si:H in AMLCD applications. Cost and scalability seem to be the primary driving force for choosing IGZO rather than LTPS. Since IGZO-based products are already being shipped, there do not appear to be any 'show-stoppers' impeding successful commercialization of IGZO technology.

We note that in the literature the negative bias illumination stress (NBIS) instability (involving a threshold voltage shift to negative voltages for an IGZO TFT subjected to a large negative applied gate voltage and simultaneous near-band gap optical excitation) is often proposed as the greatest technical challenge facing IGZO TFT technology [14-17,23-37]. Our perspective on NBIS with respect to AMLCD applications is as follows. While this is a legitimate challenge, it is worth bearing in mind that all AMLCD backplane technology channel layers are light sensitive in some fashion. Technologies employing a channel layer with a smaller band gap (e.g., a-Si:H and LTPS) require light-shielding measure(s) to suppress leakage associated with photoconductivity. NBIS in IGZO technology is in many respects analogous to photoconductivity problems witnessed in a-Si:H technology. Thus, while IGZO TFT technology will require proper passivation and appropriate light shielding for viable display backplane use, such measures are already generally employed in Si TFT-based backplanes and thus do not comprise a structural disadvantage for IGZO, although the details of their effective implementation for IGZO's unique light interaction mechanism(s) will likely involve upfront development time and cost. NBIS is discussed further in Section 5.3.

4. Active-matrix organic light-emitting diode (AMOLED) backplane applications

An LCD pixel is essentially a valve that controls the transmitted intensity of light incident from a backlight source. Thus, an LCD is a *non-emissive* (transmissive) display. In contrast, an OLED is an *emissive* display. An emissive display offers a multiplicity of advantages including wider viewing angle, higher contrast, faster response time, and lower power consumption. Also, emissive displays have sleek/lighter/thinner form factors that are more appealing to the consumer and are better suited to flexible substrate applications.

Practical LCD and OLED displays require active matrix addressing, giving rise to AMLCD and AMOLED displays. Basically, active matrix addressing involves providing two-dimensional electrical interconnectivity that facilitates periodically selecting and refreshing a pixel so that it sources the appropriate intensity and color of light required in order to present a desired visual image. Active matrix addressing is accomplished using one or more active device(s), usually TFTs, in the pixel backplane. AMLCDs and AMOLEDs require differing pixel backplane architectures in order to accomplish active matrix addressing.

Recall that the architecture of an AMLCD backplane pixel is very simple, consisting of a single *voltage-controlled* switch. Unfortunately, the architecture of an AMOLED pixel is more complex. An OLED is a *current-controlled* device. Consequently, active matrix current control is more difficult to accomplish in an AMOLED, requiring more than one TFT per pixel. In addition to requiring multiple TFTs to provide the basic current-control function, current-control circuit architectures

are very sensitive (far more than a voltage-control LCD pixel circuit) to variation and drift in TFT parameters, particularly threshold voltage. Since threshold voltage stability and uniformity can be problematic for some TFT families (as noted in Table 2 above), this comprises a major factor in implementing an AMOLED backplane with suitable lifetime for display products.

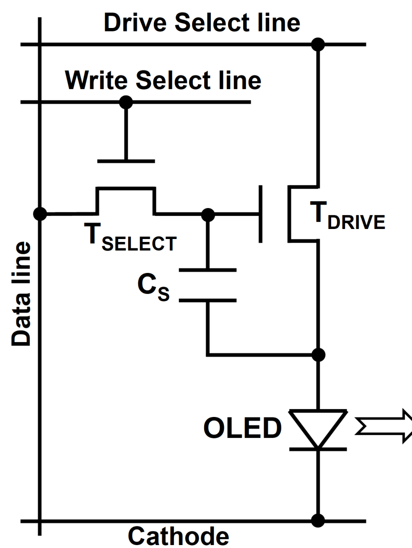

Fig. 5 Two-transistor one-capacitor (2T+1C) active-matrix organic light-emitting diode (AMOLED) pixel architecture proposed by Sony [36,37].

The simplest practical AMOLED pixel architecture consists of two TFTs and one capacitor (2T+1C), e.g., Fig. 5. One TFT is used for selecting and charging a storage capacitor during addressing. The second TFT functions as a current source to drive the OLED, based on the TFT gate voltage developed across the charged storage capacitor. The simplicity of a 2T+1C architecture is very attractive for AMOLED backplanes. However, a conventional 2T+1C circuit (different than that shown in Fig. 5, having only one select line) is susceptible to pixel dimming due to changes in TFT and/or OLED

threshold voltage during operation. The 2T+1C circuit shown in Fig. 4 was proposed by Sony [38,39]. Since Write Select and Drive Select lines can be independently controlled, this circuit may be useful in compensating for TFT and/or OLED threshold voltage drift. Alternatively, other more complex AMOLED pixel architectures employing compensation may be required, e.g., 4T+1C [40].

The case for choosing IGZO TFTs for AMOLED backplanes was forcefully made recently by LG Display Co. with their demonstration of an impressive 55” full high definition (1920 × 1080 = 2.1 megapixel) OLED TV using Gen. 8 glass (2220 mm × 2520 mm) [41]. Although IGZO TFTs were employed, the pixel architecture used was not specified.

Recent publications by Sony provide further support for advocating IGZO TFTs for AMOLED backplane applications [38,39]. They assert that a channel mobility of ~16 $cm^2V^{-1}s^{-1}$ is adequate for realizing AMOLED displays with UHD resolution (3840 × 2160 = 8.3 megapixels) at a frame rate of 480 Hz or with 8K UHD resolution (7680 × 4320 = 33.2 megapixels) at a frame rate of 240 Hz. They are confident that IGZO can meet this requirement since they have demonstrated IGZO TFTs with mobility of 24.2 $cm^2V^{-1}s^{-1}$. Moreover, they have also developed ITZO TFTs with even higher mobility of 30.9 $cm^2V^{-1}s^{-1}$. Additionally, they describe a novel, 5-mask self-aligned top gate IGZO TFT process with significantly reduced parasitic capacitance and excellent AMOLED brightness uniformity. Industrial reports of IGZO TFT technology improvements applied to commercial AMLCD and AMOLED displays – such as these from Sony – are becoming a regular occurrence at Society of Information Display (SID) and other international display conferences.

In summary, IGZO appears promising for AMOLED backplane applications. a-Si:H TFTs do not have adequate channel mobility and threshold voltage stability for this application. As is the case for AMLCD trends, cost seems to be the main driving force for preferring IGZO to LTPS for AMOLED applications. Given recent industrial inclinations, we believe that the sixty-four-dollar question for large-area, high-performance, high-volume displays may soon transition from “LTPS or IGZO?” to “AMLCD or AMOLED using IGZO?”

5. Scientific and technical issues of concern

In any newly emerging scientific and/or technical discipline, a certain amount of controversy is inevitable. Debate and resolution of such controversies may lead to new insight and perhaps further innovation. Three topics are tagged below as being ripe for further consideration and/or investigation.

5.1 Unipolar relaxation semiconductors

Silicon is a *bipolar* semiconductor. This means that it can be readily doped either n- or p-type and that the minority carrier lifetime often plays a central role in establishing the dynamic response of a semiconductor device.

Silicon is also a *lifetime* semiconductor. In a lifetime semiconductor, the dielectric relaxation time is negligibly small compared to the minority carrier lifetime, i.e., $\tau_{DR} << \tau_o$ where $\tau_{DR} = \rho\ \varepsilon$, ρ = semiconductor resistivity, and ε = semiconductor dielectric constant [42]. The dielectric relaxation time is a characteristic time corresponding to the time delay required for majority carriers to rearrange and reestablish charge neutrality if it is perturbed (e.g., by application of a voltage to a nearby contact). The condition $\tau_{DR} <<$

τ_o is readily met in silicon and other lifetime semiconductors, e.g., τ_{DR} ~ 17 ps and τ_o ~ 0.5 μs for p-type silicon doped to a concentration of 10^{15} cm^{-3}.

IGZO is a *unipolar*, n-type-only semiconductor. Moreover, it appears that IGZO is a *relaxation* semiconductor [42] in which τ_{DR} is of the same order of magnitude as τ_o. In a relaxation semiconductor, τ_o typically is given by the lifetime of injected nonequilibrium *majority* carriers. For IGZO, τ_{DR} ~ 3-300 ns, assuming a relative dielectric constant of 5, an electron mobility of 10 $cm^2V^{-1}s^{-1}$, and an electron concentration ~10^{12}-10^{14} cm^{-3}. Estimating τ_o for IGZO is more difficult. Employing the simplistic single-trap model, $\tau_o = (\sigma\, v_{th}\, N_T)^{-1}$, where σ = capture cross section (assumed to be 10^{-15} cm^2 as appropriate for neutral trap capture), v_{th} = electron thermal velocity, and N_T = trap density (~10^{14}-10^{16} cm^{-3}) leads to τ_o ~ 10-1000 ns. Thus, these crude calculations suggest that IGZO is a *relaxation* semiconductor in which $\tau_{DR} \sim \tau_o$.

Since IGZO is a *unipolar*, *relaxation* semiconductor with a wide band gap, it is dangerous to simply model it as a normal – i.e., *lifetime* – semiconductor. Can generation-recombination be accurately modeled via standard Shockley-Read-Hall theory [43]? Can the n_i ~ 10^{-8} cm^{-3} intrinsic carrier concentration of IGZO be employed in a semiconductor statistics-based calculation or is this value so small that non-equilibrium, non-steady state considerations render it meaningless [44]? Do technology computer-aided design (TCAD) simulators adequately account for non-lifetime-semiconductor aspects of IGZO modeling [45]? Are quasi-static models adequate for IGZO TFT high-frequency circuit assessment, or are much more complicated non-quasi-static models required [46]? These questions are illustrative of the types of issues that might be useful to pursue in future IGZO studies.

5.2 Capacitance-voltage analysis and punchthrough

Capacitance-voltage (C-V) analysis is an effective classical method for assessing the device physics of metal-oxide-semiconductor (MOS) interfaces in conventional silicon microelectronics [47]. Unfortunately, this method has been used – and primarily abused – in attempts to elucidate IGZO-based MOS interfaces [48-49]. The crux of the problem is that silicon wafers are quite thick (e.g., a 300 mm silicon wafer is 775 μm thick) so that a MOS capacitor can be biased strongly into depletion without encountering punchthrough, i.e., a condition in which the depletion layer thickness exceeds the thickness of the wafer or thickness of the relevant layer under investigation). In contrast, most IGZO C-V measurements reported in the literature have been conducted using TFT structures, in which the IGZO channel is extremely thin, i.e., ~50 nm. Since IGZO doping is so low and the IGZO channel is so thin, punchthrough occurs almost immediately upon application of a depleting gate bias. For example, a 50 nm thick IGZO layer with an electron carrier concentration of 10^{15} cm^{-3} will reach punchthrough when the IGZO surface potential is only ~ 5 mV! This means that changes in the measured capacitance are almost exclusively established by backside electronic boundary conditions and/or two-dimensional encroachment of the depletion layer with respect to the source and drain. Since C-V curve interpretation is based on assuming one-dimensional behavior of the depletion layer prior to encountering punchthrough, it is impossible to interpret most of the IGZO C-V curves found in the published literature. Although these punchthrough problems could in principle be circumvented with the availability of IGZO channel layers ~5-10 μm thick, series resistance effects would make it difficult to interpret measured

curves in the straightforward fashion expected when the C-V method is employed, and in any case the material properties (microstructure, defect distribution, etc.) of a several-μm-thick deposited IGZO may be substantially different than those of a ~50 nm film as required for a TFT channel.

A second challenge in making meaningful C-V measurements involves the formation of an appropriate structure for the test. In Si CMOS the Si wafer bulk provides an effectively ideal contact to the semiconductor side of the MOS structure, and the physical contact to the bulk wafer is spatially removed from the electrically active portion of the MOS device. Conversely, in an IGZO MOS capacitor, the semiconductor comprises a thin (~50 nm) layer and electrical contact to this layer for C-V characterization is provided either laterally (e.g., from source and drain contacts in a TFT-like structure) or by adding a backside metal contact not present in the corresponding TFT structure. In the former case, the structure is no longer electrically one-dimensional and proper analysis of C-V measurements requires the use of a model that accounts for lateral charge flow from perimeter contacts (which the conventional textbook C-V analysis does not). In the latter case, although the structure is electrically one-dimensional, the addition of an ohmic contact at the semiconductor back surface fundamentally modifies the nature of the structure being analyzed (since the semiconductor back surface is now a metal-semiconductor contact, rather than an insulator-semiconductor contact as in the TFT structure) so that the measured behavior and extracted characteristics are no longer fully representative of the TFT structure of interest.

5.3 Negative bias illumination stress (NBIS)

The negative bias illumination stress (NBIS) instability is a key challenge that appears to have somewhat delayed commercial adoption of IGZO TFT technology [14-17,23-37]. The NBIS instability involves a persistent negative shift in the turn-on voltage of an IGZO TFT when its gate is negatively biased and is simultaneously illuminated with near-band gap energy photons. The physical mechanism responsible for the NBIS instability is controversial. We will now concentrate on using Fig. 6 as a means of summarizing essential electrostatic aspects of NBIS. For a more detailed discussion of NBIS, the interested reader is advised to consult the references cited above.

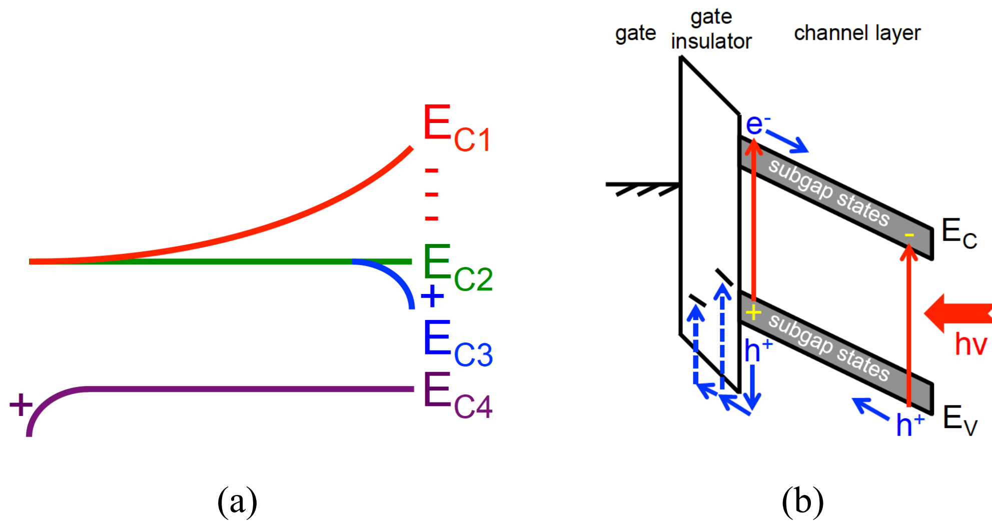

Fig. 6 (a) IGZO conduction profile from the gate insulator-channel interface (left) to the unpassivated or passivated backside channel interface (right) for (i) a channel depleted by negative charge at the backside interface (red, E_{C1}), (ii) flatband (green, E_{C2}), (iii) a backside accumulation layer formed by positive charge at the backside interface (blue, E_{C3}), (iv) a frontside accumulation layer formed by positive charge at the frontside interface (purple, E_{C4}). (b) Near-band gap photon absorption via subgap states leading to the creation of free electrons (holes) in the conduction (valence) band.

Simple electrostatic charge balance considerations can provide critical insight into the likely nature of NBIS, as summarized in Fig. 6a. The four conduction band profiles given in Fig. 6a illustrate the expected equilibrium (zero bias) band-bending situation if negative, positive or no charge is present at the backside interface, i.e., E_{C1}, E_{C2}, and E_{C3}, respectively, or if positive charge is present at the frontside interface, i.e., E_{C4}. Note that positive (negative) charge present at an interface is balanced by negative (positive) charge in the channel as evident by the negative (positive) curvature of the energy bands.

E_{C1} illustrates a depleting backside boundary condition. The positive curvature of E_{C1} in the channel region means that positive charge exists in the channel. This positive charge is balanced by negative charge located at the backside surface. A near-zero turn-on voltage is expected for this case if channel depletion arises exclusively from negative charge present at the backside surface/interface. E_{C1} corresponds to the situation expected prior to NBIS when the backside surface is unpassivated. Chemisorbed oxygen present at the backside surface constitutes a negative surface charge since formation of a chemisorbed oxygen bond requires electron transfer from the channel layer to the initially physisorbed oxygen. Note that electron transfer to form chemisorbed bonds leads to depletion of the channel layer, thereby pushing the turn-on voltage towards zero. NBIS instability is anticipated for this unpassivated case since direct photoionization and/or recombination-enhanced ionization of adsorbed oxygen is expected to negatively shift the turn-on voltage. Thus, suppression of the NBIS instability in a bottom-gate IGZO TFT will require passivation of the top surface.

The E_{C2} conduction band profile given in Fig. 6a corresponds to flatband. From an NBIS perspective, the E_{C2} case is perhaps the ideal situation, as long as the separation between the conduction band minimum and the Fermi level is large enough (i.e., equal or greater than ~ 0.22 eV) so that the electron carrier concentration in the channel layer is sufficiently small (i.e., less than ~10^{15} cm^{-3}). This will ensure that the turn-on voltage is near-zero. Flatband implies that a negligible charge density exists at the frontside and backside surface/interface. Since a shift in the turn-on voltage requires a change in the charge density at the frontside or backside surface/interface, the NBIS instability is avoided if flatband persists after NBIS testing.

The E_{C3} and E_{C4} conduction band profiles shown in Fig. 6a correspond to accumulating backside or frontside boundary conditions that give rise to strongly negative turn-on voltages, a signature of an undesirable NBIS instability. Thus, E_{C3} and E_{C4} conduction band profiles must be avoided in order to eliminate NBIS instabilities. This means that NBIS-induced formation of positive charge at either interface should be suppressed.

To pursue this further, consider Fig. 6b, illustrating the energy band situation under NBIS. The creation of delocalized electrons and/or holes in the conduction or valence band, respectively, by near-band gap light illumination is mediated by direct excitation from or into subgap states (as shown in Fig. 6b) or indirectly by subgap state ionization after excitation (not shown in Fig. 6b). Under negative bias, the electric field profile in the IGZO channel will tend to drive spatial separation of photo-generated electrons and holes, drawing holes toward the gate insulator interface and pushing electrons toward the back channel (passivation) interface. The accumulation of holes at

the gate insulator interface is a unique aspect of NBIS conditions in an IGZO TFT, because as discussed previously the wide bandgap nature of IGZO tends to preclude the formation of a hole inversion layer under normal operating conditions. Under NBIS, the gate bias induced field is a driving force for injection and trapping of holes in the gate insulator, as indicated in Fig. 6b. Depending on the choice of gate insulator material, the valence band discontinuity between IGZO and gate insulator may range from a few eV to zero or even negative. In the latter case, the lack of an appreciable barrier to hole injection means that substantial numbers of holes will be trapped at or near the gate insulator interface producing (after removal of bias and illumination) a band profile E_{C4} with positive trapped charge and IGZO accumulation layer as indicated.[32]

Table 3 Band gap (E_G), electron affinity (χ), ionization potential (IP), and valence band offset (ΔE_V) with respect to IGZO.

Material	E_G (eV)	χ (eV)	IP (eV)	ΔE_V (eV)	Reference
IGZO	3.25	3.9	7.15	NA	37
SiO_2	9	0.9	9.9	2.75	37
Si_3N_4	5.4	1.65	7.05	-0.1	50
Al_2O_3	~6.5	~2	~8.5	~1.35	37
HfO_2	6.0	2.4	8.4	1.25	37

Examination of Fig. 6b indicates that suppression of undesirable NBIS-induced positive charge injection into the gate insulator is best accomplished by (i) minimizing

the IGZO subgap state density, and (ii) choosing a gate insulator with a sufficiently large valence band offset with respect to IGZO, in order to provide a suitable barrier against hole injection into the gate insulator under negative bias. As indicated in Table 3, SiO_2 appears to be an excellent IGZO TFT gate insulator choice.

Perhaps the most popular proposed physical mechanism for the NBIS instability is to ascribe it to oxygen vacancies, to assert that an oxygen vacancy acts as a negative-U center, and to invoke persistent photoconductivity (PPC) as the experimental signature confirming negative-U behavior [25-28]. This model is not explicitly considered within the context of our NBIS discussion since it is unclear how it should be formulated within the electrostatic perspective we have employed. Presumably positive charge associated with ionization of the oxygen vacancy into its double positively charged (V_O^{2+}) state would be distributed throughout the IGZO channel layer and, moreover, the metastability barrier giving rise to the persistence of NBIS would presumably arise as a consequence of a large lattice relaxation of the oxygen vacancy cavity upon ionization, thereby precluding recapture of ionized electrons. If so, it is difficult to explain why NBIS is so much more problematic than PBIS since there is no obvious asymmetry in the oxygen vacancy negative-U model.

In summary, from an electrostatic, charge balance perspective it appears that minimization of the NBIS instability will require passivation of the top surface, reduction in the density of subgap states in the IGZO, and use of an appropriate gate insulator such as SiO_2 whose valence band alignment with IGZO provides a reasonably large barrier against hole injection under negative bias. This physical origin of subgap states in IGZO is not yet conclusively established, but is likely due to incomplete oxidation of the IGZO

and associated oxygen vacancies, suboxides, and/or variable cation coordination. If NBIS cannot be adequately controlled via materials fixes involving passivation and a reduction of the subgap state density, aggressive light-shielding measures may be required.

6. Conclusions

The future of AOS TFT technology looks very bright. IGZO appears to be an excellent choice for first-generation AOS TFT applications, as witnessed by its recent commercial insertion into AMLCD displays. Also, IGZO will likely be the AOS material-of-choice for emerging AMOLED applications. Comparing IGZO and LTPS, IGZO offers higher performance in terms of lower off-state drain current leakage as well as simple process and superior scalability (both translating to lower cost), while LTPS is attractive because of its higher mobility and its ability to provide implementation of CMOS circuitry as an option. As AOS technology evolves, it is likely that other materials beyond IGZO will be gainfully employed. We believe that ZTO is one particularly promising candidate material with respect to the always-important factor of cost. Increasing mobility is always of interest, and the vast materials space associated with multicomponent AOS compositions provides fertile ground for exploration.

Although IGZO technology currently is strongly targeted for AMLCD and AMOLED applications because of the size and potential size of their respective markets, IGZO appears to be a better semiconductor platform than a-Si:H for migrating towards other applications. Thus, other flat-panel display applications such as e-paper / electrophoretic displays and transparent displays or other non-display applications such

as RFID or integration with silicon-based integrated circuits are likely to emerge, laying the groundwork for a new wave of TFT innovation and profitable industry growth.

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