Materials Science Forum Vols. 740-742 (2013) pp 699-702
Online available since 2013/Jan/25 at www.scientific.net

doi:10.4028/www.scientific.net/MSF.740-742.699

A nanoscale look in the channel of 4H-SiC lateral MOSFETs

Patrick Fiorenza[1, a], Alessia Frazzetto[2,3], Lukas K. Swanson[1], Filippo Giannazzo[1,b] and Fabrizio Roccaforte[1,c]

[1]CNR-IMM, Catania, Italy

[2]Scuola Superiore – University of Catania, Italy

[3]STMicroelectronics, Catania, Italy

[a]patrick.fiorenza@imm.cnr.it, [b]filippo.giannazzo@imm.cnr.it, [c]fabrizio.roccaforte@imm.cnr.it

Keywords: 4H-SiC, SiO_2, Post-Oxidadion Annealing, Scanning Probe Microscopy, Scanning Capacitance Microscopy.

Abstract. In this work the field effect mobility measured on lateral n-channel MOSFETs in 4H-SiC with Al implanted body was correlated with the interface trap density measured on MOS capacitors. The test devices were fabricated on samples subjected to different post implantation annealing conditions (i.e. *with* or *without* a protective carbon capping layer) and to an identical post-oxidation annealing in N_2O. Despite the improved interfacial morphology, a reduction of the peak mobility (from 40 to 24 $cm^2V^{-1}s^{-1}$) was observed using the carbon capping layer. An increase in the density of interface traps was consistently found. Nanoscale measurements of the active doping concentration in the SiC channel region by cross-sectional scanning capacitance microscopy showed an higher compensation of p-type SiC for the sample processed *without* the capping layer, which indicates a more efficient incorporation of nitrogen at the SiO_2/SiC interface.

Introduction

Despite the excellent physical properties which make silicon carbide (4H-SiC) the most prominent material for future power electronics devices, the available MOSFETs devices have not yet reached the expected optimal performances, due to some scientific issues related to the SiO_2/SiC interface [1,2]. In particular, while post-oxide-deposition-annealings (POA) of the gate oxide in nitrogen-rich ambient (NO, N_2O) can be efficient to obtain adequate mobility values in the range of 30-50 $cm^2V^{-1}s^{-1}$ [3-6], the role of nitrogen remains object of scientific debate. In particular, recent findings suggested that nitrogen atoms are not only embedded in the gate oxide layer but also incorporated in the SiC substrate and introduce shallow donors responsible for the increased conductivity of the MOSFET channel [7,8].

A further issue in vertical 4H-SiC MOSFETs is that the selective p-type doping of the channel region is obtained by Al-ion-implantation followed by high-temperature annealing processes for electrical activation of the implanted-species [9]. Under these annealing conditions, the morphology of the channel region can be severely degraded. Hence, to alleviate this problem the surface can be protected during the post implantation annealing (PIA) using a carbon capping layer [10]. While Haney *et al.* [11] observed that the use of the capping layer does not significantly affect the channel mobility in a wide PIA range (1200-1800°C), Naik *et al.* [12] recently reported a reduction of the mobility when the devices are processed with a capping layer.

Recently, Frazzetto et al. observed that Al-implanted lateral MOSFETs processed without a cap during PIA show a higher channel mobility with respect to devices fabricated using a protecting carbon capping layer [13]. In both cases, the temperature dependence of mobility indicated Coulomb scattering by interface charges as the major limitation to carrier transport in the inversion channel. By modeling this temperature behavior, a lower interface charge density was estimated in the case of a rougher interface (*no cap*) with respect to the smoother one (*cap*).

In this work the channel mobility measured on 4H-SiC n-channel MOSFETs was correlated with the interface trap density (D_{it}) measured on MOS capacitors fabricated on n-type regions of the same wafers. The samples were subjected to a post implantation annealing *with* or *without* a capping layer, respectively, and to an identical POA in N_2O. These macroscopic measurements showed an higher mobility and lower D_{it} on the samples processed *without* cap. Nanoscale measurements of the active doping concentration in the SiC channel region by cross-sectional Scanning Capacitance Microscopy (SCM) showed an higher compensation of the p-type body for the sample processed *without* cap, which indicates a more efficient incorporation of nitrogen at SiO_2/SiC interface.

Experimental

The starting material was a n-type (0001) 4H-SiC epitaxial layer 4° off-axis cutting angle toward the <11-20> direction, 8µm-thick with a doping concentration of 1×10^{16} cm^{-3}, grown on heavily doped n^+-type 3-inches 4H-SiC substrate. Lateral n-channel MOSFETs (with L= 40 µm and W= 16 µm) were fabricated to determine the field effect channel mobility μ_{FE}. Al implantation was used to create the p-type body region, while the n-type source and drain regions were doped by heavy P-implantation. The implantations were followed by two different doping activation annealings both at 1650°C, either *with* or *without* a protective carbon capping layer on the sample surface. AFM analyses (not reported) showed a surface with a significant step bunching in the sample annealed without the cap layer, resulting in a RMS roughness of 1.75 nm, whereas a nearly flat surface (RMS= 0.36 nm) was obtained using the protective cap. For both samples similar values of the roughness have been obtained in the implanted body and un-implanted areas. Then, a 30 nm-thick SiO_2 layer was deposited by plasma enhanced chemical vapor deposition as gate dielectric, followed by a POA at 1150°C in a N_2O. Nickel silicide was used for Ohmic contacts.. The interface states density D_{it} has been estimated using the conductance method on Metal-Oxide-Semiconductor (MOS) capacitors fabricated on the same wafers of the investigated MOSFETs on the non-implanted n-type regions.

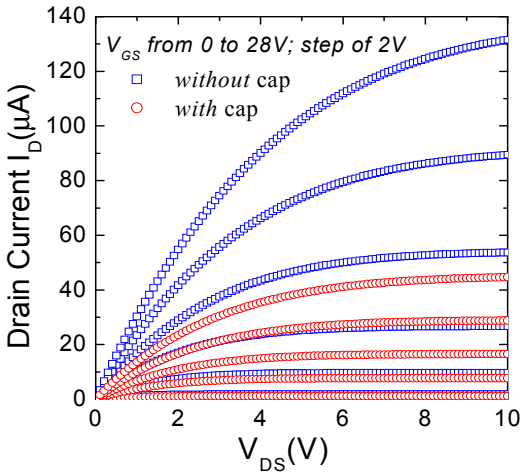

Fig. 1: I_D-V_D curves of MOSFETs processed with cap (circle) and without cap (square).

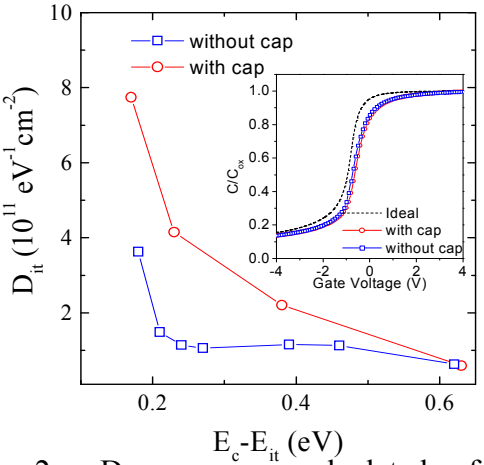

Fig. 2: D_{it} curves calculated from conductance measurements. In the inset the experimental C-V curves compared with the theoretical one.

The SCM has been used here to carry out capacitance variation applying an ac bias between the tip and the sample in the 1–10 V peak-to-peak range at 100 kHz; the resonator frequency was in the range 1.0±0.1 GHz [14] mounted on an atomic force microscope Digital Instrument D3100 equipped with the nanoscope V controller.

The capacitance voltage (C-V) and the current voltage (I-V) characteristics of the devices were measured in a Karl-Suss probe station using a Agilent B1500A parameter analyzer.

Results and Discussion

In Fig.1 the drain current (I_D) vs. the drain voltage (V_{DS}) characteristics at different gate bias (V_{GS}) values are reported for the MOSFETs processed *with* and *without* the protective capping layer. For the same gate bias, a higher drain current is measured in MOSFETs processed without capping layer. From the transfer characteristics in the linear region (at V_{DS} = 200mV) of the I_D - V_{DS} curves, the field-effect channel mobility μ_{FE} was determined. The values of the peak mobility determined at room temperature were 40 and 24 $cm^2\ V^{-1}s^{-1}$, for the samples processed *without* and *with* capping layer, respectively. The rougher sample posses the higher mobility [13].

The fixed charge density (N_t) and the density of interface traps (D_{it}) were extracted from capacitance voltage (C-V) and conductance measurements on the MOS capacitors. Fig. 2 reports the energy distribution of the interface traps for the two samples. As can be seen, a reduction of the D_{it} value close to the conduction band edge of a factor two was observed in the sample annealed without cap. Furthermore, in the inset in Fig.2, the measured C-V characteristics for the two samples are compared to the calculated ideal C-V curve. The fixed charge density N_t estimated from the flat band voltage shift are $4.8\times10^{11}\,cm^{-2}$ and $2.7\times10^{11}\,cm^{-2}$ for the samples processed *with* and *without* cap, respectively. Indeed, the results demonstrated that both in the MOSFETs [13] and in the MOS capacitors, the total amount of trapped charges at the interface is lower in the sample processed without the carbon capping layer.

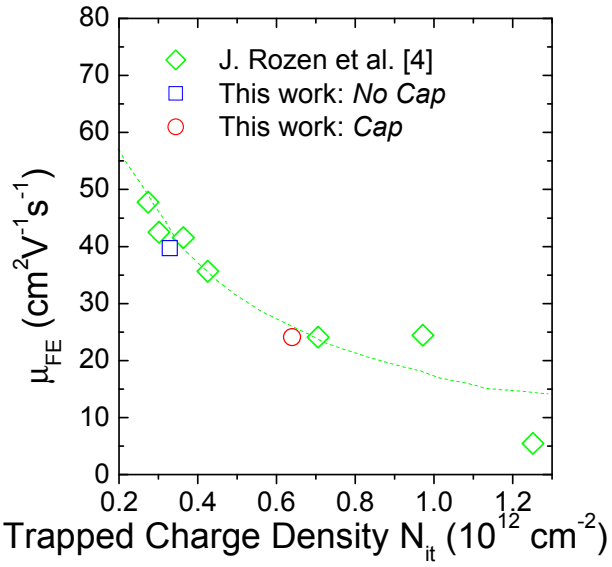

Fig. 3: μ_{FE} points for the sample processed with cap (circle) and without cap (square) compared with the results reported in REF [4](diamond).

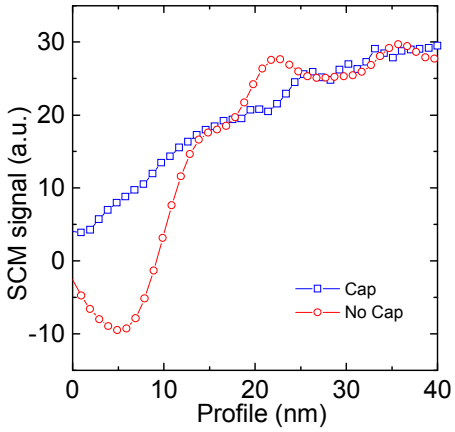

Fig. 4: SCM depth profiles in the sample processed *without* and *with* capping layer

Recently, Rozen et al. showed an clear correlation between channel mobility and the total interface trapped charge in 4H-SiC MOSFETs [4]. Fig.3 shows how our experimental data of mobility μ_{FE} and total trapped charge densities $N_{it} = N_t + \int_{E_V}^{E_C} D_{it}\,dE$ for the samples processed *with* and *without* cap perfectly follow this general trend.

Clearly, the above electrical characterization of MOS capacitors revealed that nitrogen treatment leads to a more efficient passivation of interface traps in the sample processed *without* cap than in the sample processed by cap. Beside interface state passivation, nitrogen incorporation may also affect the doping of the sub-interface SiC region [7]. High resolution scanning capacitance microscopy across the channel region was applied to get a deeper insight into this aspect. Fig. 4 shows the SCM signal vs. depth profiles collected both on the sample processed *without* and *with* capping layer in the 40 nm 4H-SiC region under the SiO_2/SiC interface. The two profiles are almost

coincident for depths higher than ~20 nm, while they are significantly different in the SiC interfacial region up to ~15 nm, where the SCM signal in the sample treated *without* capping layer is lower than in the sample protected *with* the capping layer. A lower SCM signal indicates a higher compensation of Al acceptors, which is consistent with a more efficient incorporation of substitutional nitrogen atoms in SiC.

The peculiar morphology of the annealed SiO_2/4H-SiC interface in the sample processes *without* the capping layer can be invoked to explain the better nitrogen incorporation during POA, leading to a more efficient passivation of interface traps and to a higher compensation of interfacial SiC. In fact, for a surface with step bunching, SiO_2/SiC interface is not only formed on the basal plane (0001), but a significant fraction of the interface area is formed on the (11-2n) facets [15]. Accordingly, a different efficiency of nitrogen incorporation on the (0001) and (11-2n) facets during the POA process could explain the different D_{it} values in the two samples. This observation is coherent with experimental evidences, indicating a lower D_{it} at the SiO_2/SiC interface with (11-20) non polar face [16] and a correlation between the amount of incorporated nitrogen with the trend of D_{it} and μ_{FE} in 4H-SiC MOSFETs [4].

Summary

In this paper, a nanoscale structural and electrical characterization of SiO_2/4H-SiC interfaces within lateral implanted MOSFETs is reported. In particular, irrespective of the interface roughness originating by post-implantation annealing, lower values of D_{it} were measured in the sample with a higher channel mobility and higher surface roughness. A nanoscale SCM analysis showed a localized preferential n-type doping concentration at the SiO_2/4H-SiC interface correlated with a preferential nitrogen incorporation during the POA on the peculiar morphology of the annealed 4H-SiC surfaces

Acknowledgements

This work has been partially supported by the projects PON Ambition Power (PON01_00700), ENIAC-JU LAST POWER (grant agreement n. 120218) and by the Marie Curie ITN NetFISiC (FP7 grant agreement n. 264613.

References

[1] S.-H. Ryu, et al, Mater. Sci. Forum **615-617**, 743 (2009).
[2] F. Roccaforte, F. Giannazzo, V. Raineri, J. Phys. D: Appl. Phys. **43,** 223001 (2010).
[3] F. Ciobanu, G. Pensl, V.V. Afanas'ev, A. Schoner, Mater. Sci. Forum, **483-485** 693 (2005).
[4] J. Rozen, et al., IEEE Electron Dev. Lett... **58**, 3808, (2010)
[5] T.L. Biggerstaff, et al., Appl. Phys. Lett. **95**, 032108 (2009).
[6] Y. Wang, et al., IEEE Trans. Electr. Dev., **55**, 2046 (2008).
[7]T. Umeda,K. Esaki,R. Kosugi,K. Fukuda,T. Ohshima,N. Morishita, J. Isoya, Appl. Phys. Lett. **99**, 142105 (2011)
[8] R. Kosugi,T. Umeda, Y. Sakuma, Appl. Phys. Lett. **99**, 182111 (2011)
[9] F. Giannazzo, F. Roccaforte, V. Raineri, Appl. Phys. Lett. **91**, 202104 (2007).
[10] A. Frazzetto, et al., J. Phys. D: Appl. Phys. **44**, 255302 (2011).
[11] S. Haney, A, Agarwal, Journal of Electronic Materials, **37(5)**, 666 (2008).
[12] H. Naik, K. Tang, T.P. Chow, Mater. Sci. Forum, **615-617**, 773 (2009).
[13] A. Frazzetto, et al., Appl. Phys. Lett. **99**, 072117 (2011)
[14] P.Fiorenza, R. Lo Nigro, V. Raineri, R. G. Toro, M. R. Catalano; J. Appl. Phys. **102,** 116103 (2007).
[15] H. Nakagawa, S. Tanaka, I. Suemune, Phys, Rev. Lett. **91** 226107-(2003)
[16] H. Saitoh, A. Seki, A. Manabe, T. Kimoto, Materials Sci. Forum **556-557** 659 (2007).

Silicon Carbide and Related Materials 2012
10.4028/www.scientific.net/MSF.740-742

A Nanoscale Look in the Channel of 4H-SiC Lateral MOSFETs
10.4028/www.scientific.net/MSF.740-742.699