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# Characterization of $SiO_2$/SiC interfaces annealed in $N_2O$ or $POCl_3$

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**Abstract**. This paper reports a comparative characterization of $SiO_2$/SiC interfaces subjected to post-oxide-deposition annealing in $N_2O$ or $POCl_3$. Annealing process of the gate oxide in $POCl_3$ allowed to achieve a notable increase of the MOSFET channel mobility (up to 108 $cm^2V^{-1}s^{-1}$) with respect to the $N_2O$ annealing (about 20 $cm^2V^{-1}s^{-1}$), accompanied by a different temperature behaviour of the electrical parameters in the two cases. Structural and compositional analyses revealed a different surface morphology of the oxide treated in $POCl_3$, as a consequence of the strong incorporation of phosphorous inside the $SiO_2$ matrix during annealing. This latter explained the instability of the electrical behaviour of MOS capacitors annealed in $POCl_3$.

## Introduction

In order to improve the electronic quality of the $SiO_2$/SiC interface and to increase the channel mobility of 4H-SiC MOSFETs, different annealing processes of the gate oxide in NO or $N_2O$ have been proposed already in the last two decades [1-4]. However, although these nitridation processes are able to increase the channel mobility up to the range 20-50 $cm^2V^{-1}s^{-1}$, a technological breakthrough seems to be necessary to further improve the mobility of 4H-SiC MOSFETs. In this context, a promising approach alternative to the gate oxide nitridation was recently proposed by Okamoto *et al.* [5], who introduced post-deposition-annealing (PDA) in phosphoryl chloride ($POCl_3$), enabling to obtain a channel mobility of about 90 $cm^2V^{-1}s^{-1}$. Following this work, the effects of phosphorous-based annealings on the electrical characteristics of 4H-SiC MOS [6] and MOSFETs [7] have been investigated but some reliability concerns remained under debate.

In this work, we report a comparative study of the gate oxide annealed in $N_2O$ or $POCl_3$. The different morphology and electrical behaviour observed in MOS interfaces was ascribed to the strong incorporation of phosphorous inside the $SiO_2$ matrix during annealing in $POCl_3$, as revealed by chemical microanalysis. The related electrical instability of MOS capacitors was discussed**.**

## Experimental

Nitrogen-doped 4H-SiC epitaxial layers with a nominal concentration $N_D=1\times10^{16}$ $cm^{-3}$, grown on heavily doped substrate, were used to fabricate lateral MOSFETs and MOS capacitors.

The gate oxide (a 45 nm-thick $SiO_2$ layer, deposited by plasma enhanced chemical vapour deposition) was subjected to PDA at atmospheric pressure either in $N_2O$ for 4 hours at 1150°C or $POCl_3$ for 1 hour at 1000°C. Annealed nickel films were used as Ohmic contacts for devices and test patterns. More details on the devices fabrication processes can be found in our previous works [8-10].

Lateral MOSFETs were used to determine the field effect mobility $\mu_{FE}$, while vertical MOS structures served for the estimation of interface state density $D_{it}$ and to explore the conduction through the insulating layer.

Transmission electron microscopy (TEM) combined with energy dispersive x-ray (EDX) analysis was performed to monitor the structure and the composition of the annealed gate oxide.

## Results and Discussion

The field effect mobility $\mu_{FE}$, extracted from the transfer characteristics of the MOSFETs at room temperature, is reported in Fig. 1 as a function of the gate bias $V_g$ for the two annealing conditions. As can be seen, the maximum values of the mobility (peak mobility) were 19 $cm^2V^{-1}s^{-1}$ and 108 $cm^2 V^{-1}s^{-1}$, for the devices subjected to PDA in $N_2O$ and $POCl_3$, respectively. The huge increase of the channel mobility observed upon annealing of the gate oxide in $POCl_3$ was accompanied by a reduction of the interface state density $D_{it}$ close to the conduction band edge. In particular, the values of $D_{it}$ at about $E_c$-$E_{it}$=0.2eV, determined by the C-V analysis of the MOS capacitors, were $5.7\times10^{11}$ $eV^{-1}cm^{-2}$ for the $POCl_3$ and $1.8\times10^{12}$ $eV^{-1}cm^{-2}$ for $N_2O$ case. Many authors described the channel mobility in 4H-SiC MOSFETs considering different physical components (bulk mobility, surface roughness, phonon scattering, Coulomb scattering) [9, 11,12]. In these works, the temperature dependence of the channel mobility was studied to identify the main mechanism of carrier transport in the MOSFET channel. With the same purpose, also in our case, both the field effective mobility $\mu_{FE}$ and the threshold voltage $V_{th}$ were measured at different temperatures in the range 298-423 K. Interestingly, a different behaviour of these parameters was observed in the two PDA conditions. In the MOSFET annealed in $N_2O$ the mobility increased with the temperature (up to 25 $cm^2V^{-1}s^{-1}$ at 423 K), while the threshold voltage decreased in the same range (from 10 V to 6.24 V). On the other hand, the MOSFET annealed in $POCl_3$ showed the opposite trend, i.e. with the mobility decreasing down to 75 $cm^2V^{-1}s^{-1}$ at 423 K, and the threshold voltage increasing up to 13.3 V. The observed temperature dependence of the mobility indicates that Coulomb scattering governs the carrier transport in the channel after PDA in $N_2O$. On the other hand, a decreasing mobility with increasing temperature in $POCl_3$ suggests rather that phonon scattering dominates over the other contributions. In spite of their opposite trend with the temperature, a correlation between $\mu_{FE}$ and $V_{th}$ was found, as can be clearly observed in Fig. 2, reporting the field effect mobility as a function of the threshold voltage for the two cases. The correlation observed here in the measure of the single device at different temperatures is similar to that observed when measuring a batch of several devices at room temperature [13].

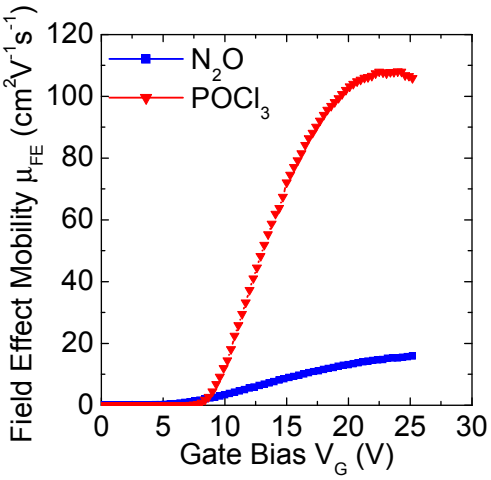


Fig. 1: Field effect mobility ($\mu_{FE}$) as a function of the gate bias ($V_g$) for 4H-SiC MOSFETs: Comparison of devices processed with PDA in $N_2O$ (squares) and $POCl_3$ (triangles).

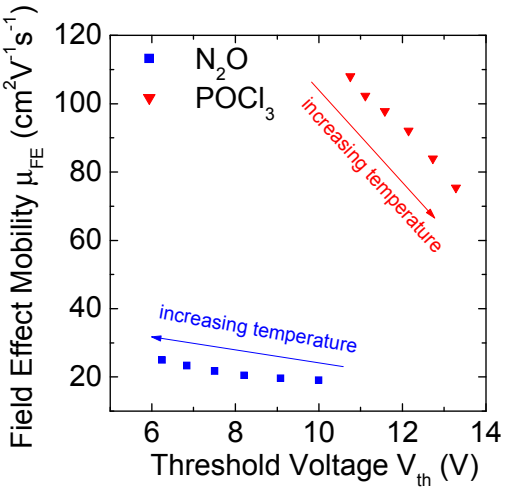


Fig. 2: Field effect mobility ($\mu_{FE}$) as a function of the threshold voltage ($V_{th}$) at different temperatures of devices processed with PDA in $N_2O$ (squares) and $POCl_3$ (triangles).

To get insights into the modification of the gate oxide induced by PDA, additional structural and electrical characterizations have been carried out. TEM analyses of the oxide/SiC interface region of the devices were performed on cross sectional samples prepared the slice with a cut along the [11-

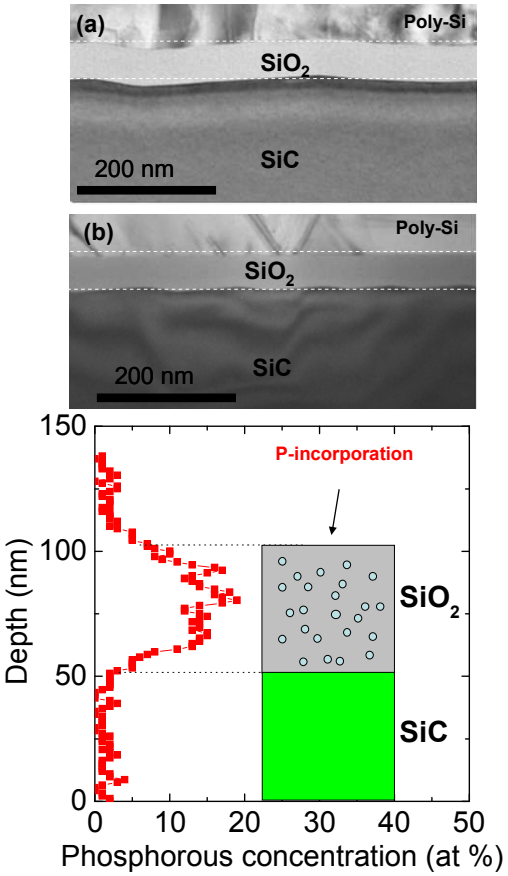


Fig. 3: Low resolution TEM micrographs of the $SiO_2$/4SiC interface after annealing in $N_2O$ (a), $POCl_3$ (b) and phosphorous concentration profile extracted by EDX (c)

annealed in $POCl_3$ (Fig. 3c) clearly shows that a significant amount of phosphorus diffused inside the oxide after PDA in $POCl_3$ and it is almost homogeneously distributed within the insulating layer. From the quantitative analysis of the EDX signals, it was possible to estimate a phosphorous concentration of about 12 at.%**.** The dissolution of such a large amount of phosphorous inside the $SiO_2$ network during annealing in $POCl_3$ typically results in the formation of a phosphosilicate glass [14] and can explain the planarization of the interface between the $SiO_2$ and the poly-Si observed in Fig. 3b. In fact, it is known that P-doped $SiO_2$ can soften and reflow above 950°C, creating a smooth topography that is beneficial for the subsequent poly-Si deposition [15].

20] misorentation direction, in order to visualize the 4H-SiC "surface steps". Fig. 3 shows the cross section TEM images of the gate region for the samples annealed in $N_2O$ and in $POCl_3$. Only a very small difference in the gate oxide thickness could be estimated in the two cases, i.e., 46 nm in the sample annealed in $N_2O$ and 46-50 nm in the case of the sample annealed in $POCl_3$. An interesting feature, that has not been previously addressed in the other studies, is the different morphology of the oxides surfaces after the PDA treatments. In fact, as can be seen, the oxide layer annealed in $N_2O$ exhibits a conformal coating, i.e., with periodical undulations (steps) along the [11–20] direction. On the other hand, the oxide annealed in $POCl_3$ shows a high degree of surface planarization (as deduced by the flat interface $SiO_2$/poly-Si interface). Consequently, with this peculiar morphology the oxide thickness extracted by the TEM image ranges between 46 and 50 nm.

The composition of the gate oxide was determined by EDX analysis. In particular, while the sensitivity of this technique cannot give significant information in the case of nitrogen-rich ambient annealing, the EDX elemental profiles acquired in the oxide

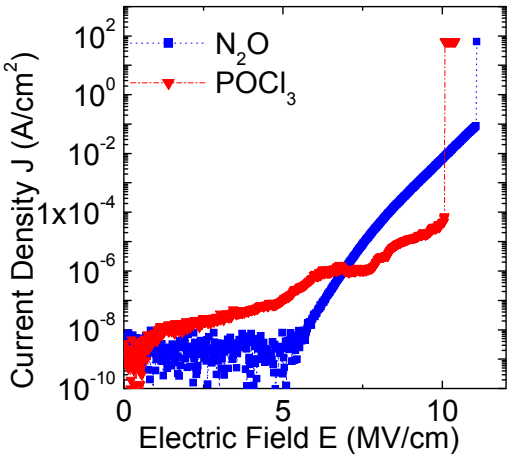


Fig. 4: Current density as a function of the electric field in 4H-SiC MOS capacitors annealed either $N_2O$ and in $POCl_3$

To have additional information on the reliability of the oxides, the stability of the flat band voltage $V_{FB}$ of MOS capacitors was monitored by cyclical C-V measurements, i.e., sweeping the bias from accumulation to depletion with increasing starting voltages at each cycle. Under these conditions, while the sample annealed in $N_2O$ shows only a small variations of $V_{FB}$ (<0.3V), the

sample annealed in $POCl_3$ exhibited a large positive shift, i.e. up to 2 V already below 5MV/cm. We argue that this instability is due to the electron trapping in the oxide, associated to the presence of "P-related defects". In fact, in the presence of such an amount of P in the $SiO_2$ network, a large variety of defects can be generated, leading to negative charge trapping and flat band voltage shift [16]. Another consequence appeared through the anomalous conduction in the gate oxide treated in $POCl_3$. Fig. 4 shows a semilog plot of the current density ($J$) as a function of the electric field ($E_{ox}$) for MOS capacitors after PDA in $N_2O$ and $POCl_3$. As can be seen, while the breakdown field of the two oxides is very similar (11.31 MV/cm and 10.74 MV/cm, for $N_2O$ and $POCl_3$, respectively), the MOS treated in $POCl_3$ exhibits a deviation from the Fowler-Nordheim behaviour and a higher leakage current than those in the MOS annealed in $N_2O$.

## Summary

In summary, this paper compared the electrical and structural properties of $SiO_2$ gate dielectrics on 4H-SiC annealed in $N_2O$ and $POCl_3$. The significant increase of the channel mobility (up to 108 $cm^2V^{-1}s^{-1}$) obtained in $POCl_3$ results in a different temperature dependence of mobility, due to the lowering of the $D_{it}$. A correlation between mobility and threshold voltage values is observed at different temperatures. The notably morphological and compositional changes of the gate oxide, characterized by a strong incorporation of phosphorous inside the $SiO_2$ matrix, determined an instability of the electrical behaviour of the MOS capacitors. According to the above results, the interactions of P with the $SiO_2$/SiC system deserve further attention by the SiC community, to make P-based PDA processes really employable in 4H-SiC MOSFET technology.

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