Fowler-Nordheim tunneling at SiO2/4H-SiC interfaces in metal-oxide-semiconductor field effect transistors

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The conduction mechanisms and trapping effects at SiO_2/4H-SiC interfaces in metal-oxide-semiconductor field effect transistors (MOSFETs) were studied by Fowler-Nordheim (FN) tunnelling and frequency dependent conductance measurements. In particular, the analysis of both MOS capacitors and MOSFETs fabricated on the same wafer revealed an anomalous FN behavior on *p*-type implanted SiC/SiO_2 interfaces. The observed FN instability upon subsequent voltage sweeps was correlated to the charge-discharge of hole trap states close the valence band edge of 4H-SiC. The charge-discharge of these traps also explained the recoverable threshold voltage instability observed in lateral MOSFETs. © *2014 AIP Publishing LLC*. [http://dx.doi.org/10.1063/1.4898009]

Owing to its physical properties, silicon carbide (4H-SiC) is a first choice material for the next generation of efficient power electronic devices.[1,2] Although metal-oxide-semiconductor field effect transistors (4H-SiC MOSFETs) with excellent performances have been demonstrated,[3] the inversion channel mobility (μ_{FE}) and the threshold voltage (V_{th}) are continuously debated. The low mobility values are typically ascribed to electron trapping at interface states (D_{it}) near the conduction band and Coulomb scattering by the trapped charges.[4–7] On the other hand, charge trapping at SiO_2/SiC interfaces is in turn indicated as a possible reason for V_{th} instabilities occurring under prolonged application of a gate bias.[8–11] In this context, Singh and Hefner[12] argued that the MOSFET reliability is essentially limited by the smaller band offset between SiC and SiO_2 (2.7 eV) as compared to silicon (3.2 eV), leading to higher tunnelling currents which can enhance electron trapping and oxide degradation. Furthermore, they pointed out that trap states at SiO_2/SiC interface not only affect the channel mobility but also influence the barrier height for Fowler-Nordheim (FN) tunnelling.[12]

In this letter, conduction mechanisms and trapping effects at SiO_2/4H-SiC interfaces in MOSFETs were studied by FN tunnelling and frequency dependent conductance measurements, with special attention to the *p*-type Al-implanted 4H-SiC regions of the devices.

n-MOS capacitors were fabricated using nitrogen doped 4H-SiC epitaxial layers with a doping concentration of $10^{16}\,cm^{-3}$. Lateral n-channel MOSFETs were fabricated on the same wafer using P- and Al-implantations to create the *n*-type source-drain and the *p*-type body regions, respectively. The doping level of the *p*-type body region was about $10^{17}\,cm^{-3}$.[13] The p-type MOS capacitors were also fabricated in the Al-implanted body region. Nickel silicide was used for Ohmic contacts, both for *n*-type and *p*-type regions.[14] A 40 nm-thick deposited SiO_2 layer, subjected to an annealing in N_2O at 1150 °C for 4 h, was used as gate dielectric.[13]

The capacitance voltage (C-V) and current voltage (I-V) characteristics of the devices were measured in a Karl-Suss probe station, using an Agilent B1500A parameter analyzer.

Figs. 1(a) and 1(b) report representative I-V characteristics acquired on the epitaxial *n*-MOS and on Al-implanted *p*-MOS capacitors. Fig. 1(a) shows three I-V characteristics collected consecutively on a *n*-MOS device. As can be seen, the curves show a typical FN behaviour and are almost perfectly overlapped in the three I-V measurements, thus being an indication of a stable electrical behavior. Fig. 1(b) shows three I-V characteristics collected consecutively on a *p*-MOS device. In this case, it can be noticed that during the first I-V measurement, a significant current increase is observed above a gate bias of $V_G = -20$ V. On the other hand, during the subsequent I-V, this current rise becomes steeper and occurs at a more negative gate bias ($V_G = -30$ V). No further instability of the I-V curves is observed during the third measurement. Hence, the behavior of *p*-MOS indicates an instability in the FN conduction of the holes through the insulator layer.

To quantify this effect, the I-V characteristics were analyzed using the FN formalism

$$\ln\left(J/E_{ox}^2\right) = \frac{q^3\left(\frac{m}{m_{ox}}\right)}{8\pi h\Phi_B} - \frac{8\pi\sqrt{2m_{ox}\Phi_B^3}}{3qh}\frac{1}{E_{ox}}, \qquad (1)$$

where J is the current density, E_{ox} is the electric field across the oxide, m and m_{ox} are the free and effective electron (hole) masses, respectively, and q is the electron (hole) charge, h is the Plank constant, and Φ_B is the tunnelling barrier height for electrons (holes). By the fits in the linear region of the "FN plots" $\ln(J/E_{ox}^2)$ vs $1/E_{ox}$ (not reported here), it was possible to determine the values of Φ_B for both electrons and holes.[15]

While in *n*-type MOS capacitors an electron tunnelling barrier height of $\Phi_B^{E_C}(\exp) = 2.79$ eV was determined, i.e., only slightly larger than the theoretical value of 2.7 eV, in *p*-MOS capacitors, the valence band hole barrier height increased during the subsequent I-V measurements, from $\Phi_B^{E_V}(\exp) = 1.2$ eV (in the first I-V) up to $\Phi_B^{E_V}(\exp) = 3.1$ eV (when the FN I-V characteristics became stable). This latter is approaching the theoretical one of $\Phi_B^{E_V}(th) = 2.9$ eV.

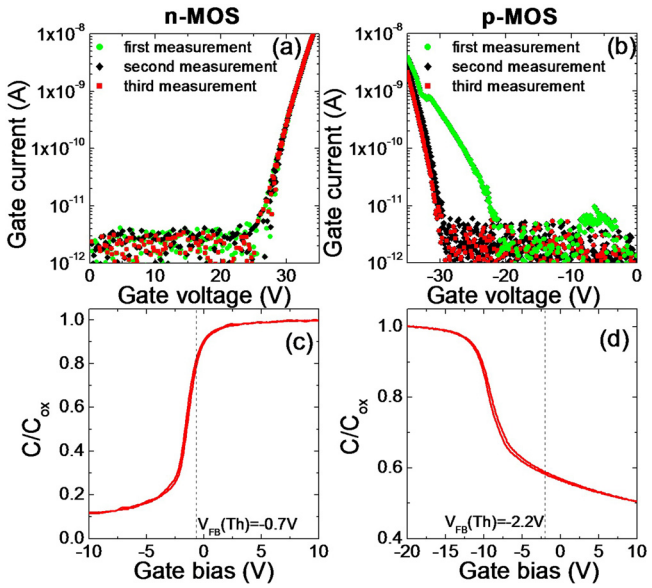

FIG. 1. Fowler-Nordheim I-V characteristics of the epitaxial *n*-MOS (a) and of Al-implanted *p*-MOS (b). C-V curves collected on epitaxial *n*-MOS (c) and on Al-implanted *p*-MOS (d).

The C-V characteristics of the same devices collected from accumulation to inversion and backward are shown in Figs. 1(c) and 1(d). It is worth noting that the *n*-MOS C-V curves (Fig. 1(c)) show a flat-band voltage $V_{FB} = -0.4\,V$, that is, close to the theoretical value of $-0.7\,V$ (dashed line). This difference can be attributed to an amount of negative effective charges in the insulator of $N_{eff} = (\Delta V_{FB} C_{ox})/q \approx 2 \times 10^{11} cm^{-2}$. This value is comparable to that of state of the art 4H-SiC MOS-based devices.[16] The presence of a negative effective charge in the insulator increases the electrons tunnelling barrier height, as it was indeed deduced by the FN analysis. On another hand, the *p*-MOS C-V curves (Fig. 1(d)) show a flat-band voltage value of $V_{FB} = -10\,V$, i.e., significantly shifted towards negative values with respect to the theoretical value of $-2.2\,V$ (dashed line). Since both capacitors were fabricated on the same wafer, i.e., with the same interface preparation and post-deposition-annealing of the SiO_2 layer, the large negative shift of V_{FB} in the *p*-MOS cannot be ascribed to a positive effective charge in the oxide, as the same shift would have been expected also in the *n*-MOS. More likely, it can be argued that the presence of deep states, located in the lower portion of the gap and acting as hole traps in the *p*-type Al-implanted material, can be responsible for such a large negative shift. In fact, a similar behaviour has been already reported for *p*-type 4H-SiC epitaxial layers and attributed to the presence holes that are trapped at deep states (hole traps) and behave like positive fixed charge.[17,18]

To get more insights on the previous results, the C-V curves of the *p*-type material were collected also on lateral MOSFETs operating in a configuration often regarded as "gate-controlled-diode" (GCD).[17] In this operation mode, the source, drain, and body electrodes of the MOSFET are grounded, while the gate electrode becomes the anode of the GCD. In fact, due to the low minority carrier generation rate in wide band gap 4H-SiC at room temperature, a conventional *p*-MOS capacitor is typically driven into deep depletion. Thus, deep states are not in equilibrium with the dc bias sweep and, therefore, cannot be detected during the measurement using a conventional *p*-MOS capacitor. On the other hand, in a GCD (inset in Fig. 2), the n^+-*p* source-body (SB) junction of the lateral MOSFET can be used as an external source of minority carriers (electrons), allowing detection of hole traps even at room temperature.[17]

In the cyclic C-V measurements collected on the gate-controlled diode reported in Fig. 2, the bias was swept from accumulation to inversion and backward. As can be seen, the C-V curves acquired in this configuration show again a large negative flatband shift from the theoretical value, similar to that observed in the case of the conventional *p*-MOS capacitor (Fig. 1(d)). Also in this case, this large negative shift cannot be attributed to fixed charges in the oxide. However, in this case, the inversion-to-accumulation curve does not overlap the accumulation-to-inversion one, consistent with charge trapping/detrapping effects. The shape of the C-V curves can be explained by the hole trapping mechanism (charge-discharge of the states) as follows. In the sweep from accumulation-to-inversion, a "deep-depletion hook" is visible between $V_G = -3\,V$ (point "A") and $V_G = +2.5\,V$ (point "B"), and can be attributed to the presence of such hole traps. The semiconductor surface reaches strong inversion at point $V_G = -3\,V$ (point "A"). However, at this gate bias, the SB junction keeps the SiC-SiO_2 interface adjacent to the n^+ island in equilibrium. This implies that an extra gate bias (more positive) is required to get the SB junction barrier region inverted. As a consequence, the capacitance decreases below the inversion value reaching the minimum capacitance between the points A and B in Fig. 2. At this point, the electrons can flow into the region beneath the whole gate area. Under this condition, discharging of hole traps occurs, i.e., the trapped holes are neutralized by the provided minority carriers (electrons).

On the other hand, the sweep from inversion-to-accumulation reveals a "ledge" in the C-V curve (point "C"). In particular, when the bias approaches point "C," the bands begin to unbend towards the flatband condition. Then, holes can be again captured in the deep states, and these states change

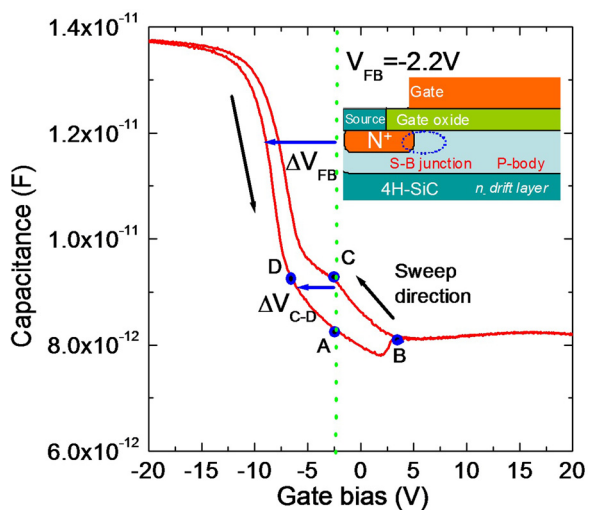

FIG. 2. Cyclic C-V curves acquired on the "gate-controlled diode" (see inset) in lateral MOSFETs.

their condition from neutral to positive (charging). Consequently, a large flatband voltage shift (typical of the conventional *p*-MOS) is again observed (point "D").

This behavior cannot be observed in the conventional *p*-MOS capacitor (Fig. 1(d)), due to the lack of minority carrier generation. However, a similar trend has been already observed in *p*-MOS capacitors using photo-generation as a source of minority carriers.[19]

The amount of hole traps could be estimated from the shift between the C-V curves during the charging-discharging, i.e., namely the shift (ΔV_{C-D}) at the ledge between the point "C" (on the inversion-to-accumulation curve) and the point "D" on the accumulation-to-inversion C-V curve at the same capacitance value: $N_{it} \approx (\Delta V_{C-D} C_{ox})/q$, where C_{ox} is the capacitance per unit area in accumulation. In our case, it has been found $N_{it} = 2.9 \times 10^{12} \mathrm{cm}^{-2}$.

The correlation between the FN instability observed in *p*-MOS capacitors (Fig. 1(b)), and the charging-discharging of trap states was monitored using lateral MOSFET as test vehicle to monitor at the same time the barrier height for electrons and holes. In particular, in this case, the current-voltage (I_G-V_G) measurements were carried out by shorting the body, source, and drain terminals, and sweeping the gate bias both in the positive and negative direction. Fig. 3 shows the I_G-V_G characteristics collected on the MOSFETs in two different bias conditions. Also in this case, different bias sweeps have been performed to check the stability.

First of all, from the I_G-V_G characterization of the MOSFETs under positive gate bias, the electron conduction through the oxide layer (at $V_G > +20$ V) appears to be stable, since the first positive voltage sweep (from $V_G = 0$ to $V_G = +35$) confirms the behaviour observed on the epitaxial *n*-MOS in Fig. 1(a). On the other hand, under negative gate bias, the hole conduction through the oxide layer (at $V_G < -25$ V) exhibits a small instability (similar to the *p*-MOS capacitors), that can be recovered after the subsequent negative voltage sweep (from $V_G = 0$ to $V_G = -35$). Notably, only a moderate FN barrier instability with respect to that observed in the *p*-MOS capacitor (Fig. 1(b)) is observed in the GCD configuration. However, it interesting to observe the current peaks appearing in the I_G-V_G curves in Fig. 3, both in the positive bias condition (from $V_G = 0$ to $V_G = +5$) and in the negative bias condition (from $V_G = 0$ to $V_G = -10$). Considering the bias (between 0 and 10 V) and current values (between 10^{-14} and 10^{-13} A) involved in the measurement, for an oxide thickness of 40 nm, the experimentally observed current peaks cannot be related to a conduction current. More likely, the observed peaks are due to a displacement current related to capacitance variations occurring in the system during the gate bias sweep. Moreover, there is a correspondence between the hook and ledge observed in the C-V curves and the evolution of these peaks occurring during the subsequent gate voltage sweeps. Interestingly, the pairs of points A-B and C-D possess both the same capacitance (see Fig. 2) value and the same current value (Fig. 3). This latter corroborates the hypothesis of a displacement current related to the capacitance variation during the charging-discharging mechanism of the hole traps. Moreover, the peaks in the negative bias region shift for the same quantity ΔV_{C-D} as in case of the cyclic C-V depicted in Fig. 2. Hence, the total amount of hole traps can be also estimated by these shifts.

It has to be emphasized that the features present the I-V curves in Fig. 3 were observed also when the gate voltage V_G was cyclically swept from +35 V to −35 V.

In Fig. 4, the distribution of the SiO_2/SiC interface states D_{it}, determined by frequency dependent conductance measurements[20] on both epitaxial *n*-MOS and Al-implanted *p*-MOS, is reported as a function of the energy position between the conduction band bottom E_C and valence band top E_V. The epitaxial n-MOS was used to determine the distribution of D_{it} close to the conduction band bottom (bold dots). The D_{it} at 0.2 eV below E_C is about $8 \times 10^{11}\,\mathrm{cm}^{-2}\mathrm{eV}^{-1}$. On the other hand, the implanted p-MOS was used to determine the distribution of D_{it} close to the valence band top (open dots). In this case, the

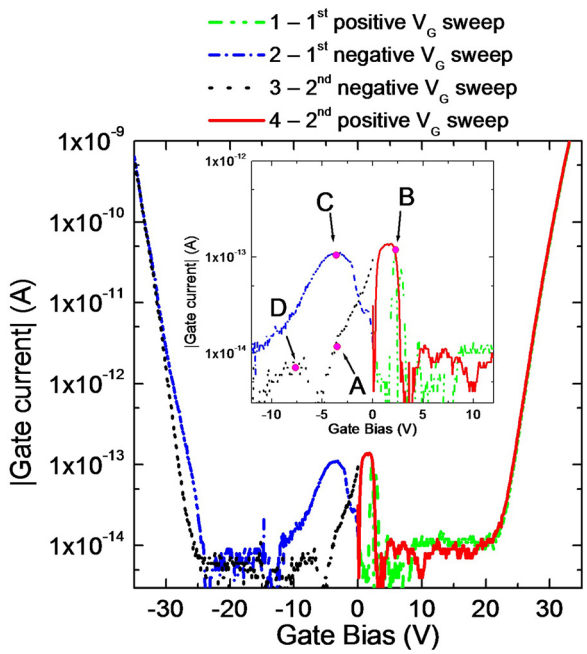

FIG. 3. I_G-V_G characteristics of MOSFETs, acquired in the sequence: 1—1st positive V_G sweep from 0 to 35 V (green); 2—1st negative V_G sweep from 0 to −35 V (blue); 3—2nd negative V_G sweep (black); 4—2nd positive V_G sweep (red). In the inset, a zoom of the low voltage region between −12 and +12 V.

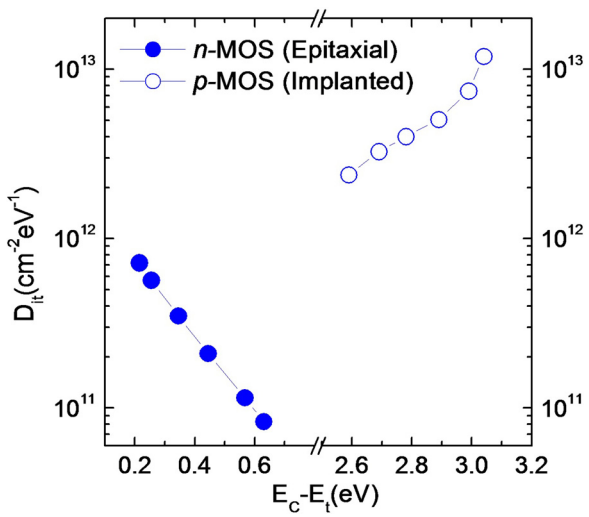

FIG. 4. Density of the SiO_2/4H-SiC interface states D_{it} as a function of the energy on both epitaxial *n*-MOS and Al-implanted *p*-MOS.

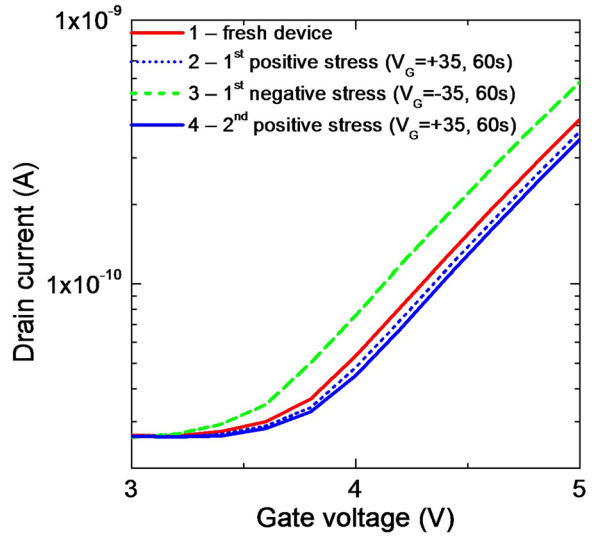

FIG. 5. I_D-V_G characteristics of MOSFETs acquired in the sequence: 1—fresh device (red dashed line); 2—after 60 s 1st positive stress at $V_G = +35$ (blue dotted line); 3—after 60 s 1st negative stress at $V_G = -35$ (green dashed line); 4—after 60 s 2nd positive stress at $V_G = +35$ (blue bold line).

value of D_{it} at 0.2 eV above E_V is about $1 \times 10^{13}\,cm^{-2}eV^{-1}$, i.e., much higher than the D_{it} close to conduction band edge E_C. Notably, the integral of the D_{it} distribution close to the valence band edge is $2.2 \times 10^{12}\,cm^{-2}$, i.e., very close to the amount of traps estimated by the shift of the C-V curves in Fig. 2 ($2.9 \times 10^{12}\,cm^{-2}$).

It is worth noting that, while for *p*-type epitaxial material the interface state density D_{it} in the lower part of the gap is often lower than near the conduction band edge,[21–23] this value can increase by the introduction of nitrogen at the interface (by nitridation annealing or implantation).[21,24] In addition, in our case, besides employing nitridation annealing, the measurement was done on *p*-type implanted material, which is known to exhibit higher D_{it} than the epitaxial one.[25]

To monitor the possible implications of the aforementioned charge-discharge mechanism of hole traps in practical devices, the transcharacteristics (I_D-V_G) of lateral MOSFETs at a drain bias of $V_{DS} = 10$ V were acquired both on "fresh devices" and after positive ($V_G = +35$) and negative ($V_G = -35$) gate stress for 60 s, i.e., similar to the stress conditions used in the FN investigation. Fig. 5 shows the I_D-V_G characteristics. First, it can be noticed that the positive stress does not significantly affect the value of V_{th}. In fact, the positive stress induces only a negligible shift of the curve (blue line) toward more positive gate bias values with respect to the transcharacteristic of the fresh device (red dashed curve). Conversely, by applying a negative stress, a more relevant shift of the I_D-V_G curves toward negative gate bias values occurs ($\Delta V_{th} = -0.25$ V). It is worth nothing that this small instability of V_{th} is fully reversible, consistent with the reversibility of trapping/detrapping mechanism described before. In fact, by performing an additional positive gate stress at $V_G = +35$ for 60 s (blue line), the initial I_D-V_G curve of the fresh device is recovered.

The trapping/detrapping mechanism of the interface states has a similar impact on the threshold voltage in high current vertical 4H-SiC MOSFETs subjected to cyclic bias stress.[26]

In conclusion, the conduction mechanisms and trapping effects at *p*-type SiO_2/4H-SiC interfaces in the channel region of a MOSFETs were studied. Fowler-Nordheim measurements on both *n*-type and *p*-type MOS capacitors revealed an instable hole tunnelling barrier. Such instability has been explained in terms of charging-discharging mechanism of deep holes traps close to the valence band edge. The same mechanism also explained the reversible threshold voltage instability observed in lateral MOSFETs upon gate bias stress.

[1]M. Shur, S. Rumyanstev, and M. Levinshtein, *SiC Materials and Devices* (World Scientific Singapore, 2006), Vol. 1.
[2]F. Roccaforte, P. Fiorenza, G. Greco, R. Lo Nigro, F. Giannazzo, A. Patti, and M. Saggio, Phys. Status Solidi A **211**, 2063 (2014).
[3]S.-H. Ryu, S. Dhar, S. Haney, A. Agarwal, A. Lelis, B. Geil, and C. Scozzie, Mater. Sci. Forum **615–617**, 743 (2009).
[4]V. V. Afanas'ev, F. Ciobanu, S. Dimitrijev, G. Pensl, and A. Stesmans, J. Phys.: Condens. Matter **16**, S1839–S1856 (2004).
[5]F. Ciobanu, G. Pensl, V. V. Afanas'ev, and A. Schöner, Mater. Sci. Forum **483–485**, 693 (2005).
[6]E. Arnold and D. Alok, IEEE Trans. Electron Devices **48**, 1870 (2001).
[7]N. S. Saks and A. K. Agarwal, Appl. Phys. Lett. **77**, 3281 (2000).
[8]M. Gurfinkel, H. D. Xiong, K. P. Cheung, J. S. Suehle, J. B. Bernstein, Y. Shapira, A. J. Lelis, D. Habersat, and N. Goldsman, IEEE Trans. Electron Devices **55**, 2004 (2008).
[9]T. Kikuchi and M. Ciappa, Microelectron. Reliab. **53**, 1730 (2013).
[10]M. Noborio, M. Grieb, A. J. Bauer, D. Peters, P. Friedrichs, J. Suda, and T. Kimoto, Mater. Sci. Forum **645–648**, 825 (2010).
[11]H. Yano, Y. Oshiro, D. Okamoto, T. Hatayama, and T. Fuyuki, Mater. Sci. Forum **679–680**, 603 (2011).
[12]R. Singh and A. R. Hefner, "Reliability of SiC MOS devices," Solid-State Electron. **48**, 1717–1720 (2004).
[13]A. Frazzetto, F. Giannazzo, P. Fiorenza, V. Raineri, and F. Roccaforte, Appl. Phys. Lett. **99**, 072117 (2011).
[14]M. Vivona, G. Greco, F. Giannazzo, R. Lo Nigro, S. Rascunà, M. Saggio, and F. Roccaforte, Semicond. Sci. Technol. **29**, 075018 (2014).
[15]R. K. Chanana, K. McDonald, M. Di Ventra, S. T. Pantelides, L. C. Feldman, G. Y. Chung, C. C. Tin, J. R. Williams, and R. A. Weller, Appl. Phys. Lett. **77**, 2560 (2000).
[16]J. Rozen, S. Dhar, S. K. Dixit, V. V. Afanas'ev, F. O. Roberts, H. L. Dang, S. Wang, S. T. Pantelides, J. R. Williams, and L. C. Feldman, J. Appl. Phys. **103**, 124513 (2008).
[17]S. T. Sheppard, J. A. Cooper, Jr., and M. R. Melloch, J. Appl. Phys. **75**, 3205 (1994).
[18]N. Inoue, T. Kimoto, H. Yano, and H. Matsunami, Jpn. J. Appl. Phys., Part 2 **36**, L1430 (1997).
[19]H. Yano, F. Katafuchi, T. Kimoto, and H. Matsunami, IEEE Electron. Device Lett. **46**, 505 (1999).
[20]E. H. Nicollian and J. R. Brews, *MOS Physics and Technology* (Wiley, New York, 1982).
[21]G. Y. Chung, C. C. Tin, J. R. Williams, K. McDonald, M. Di Ventra, S. T. Pantelides, L. C. Feldman, and R. A. Weller, Appl. Phys. Lett. **76**, 1713 (2000).
[22]V. V. Afanas'ev, A. Stesmans, F. Ciobanu, G. Pensl, K. Y. Cheong, and S. Dimitrijev, Appl. Phys. Lett. **82**, 568 (2003).
[23]M. Noborio, M. Grieb, A. J. Bauer, D. Peters, P. Friedrichs, J. Suda, and T. Kimoto, Jpn. J. Appl. Phys., Part 1 **50**, 090201 (2011).
[24]G. Pensl, F. Ciobanu, T. Frank, D. Kirmse, M. Krieger, S. Reshanov, F. Schmid, M. Weidner, T. Ohshima, H. Itoh, and W. J. Choyke, Microelectron. Eng. **83**, 146 (2006).
[25]S. Noll, D. Scholten, M. Grieb, A. J. Bauer, and L. Frey, Mater. Sci. Forum **740–742**, 521 (2013).
[26]M. Saggio, A. Guarnera, E. Zanetti, S. Rascunà, A. Frazzetto, D. Salinas, F. Giannazzo, P. Fiorenza, and F. Roccaforte, Proceedings of the 10th European Conference on Silicon Carbide and Related Materials, Grenoble (France), 21–25 September 2014.