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A Compact Analytical Design of Dual-Loop 18 GHz Frequency Synthesizer to Enhance Signal Reliability in Digital Millimeter Radio Link System

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Abstract. In this paper a high resolution dual-loop 17.7–19.7 GHz frequency synthesizer is presented which is compatible with ITU-R (F.595-6) standards. The investigations of phase noise and spur frequency contents are discussed in detail. The simulated and measured phase noise and spur frequency contents are similar to one another. Phase noise of −81 dBc/Hz in 17.7 GHz at 10 KHz offset frequency is measured by (HP8560) series Spectrum analyzer and it matches with predicted measurements.

Keywords. Dual-Band, Frequency Synthesizer, IRTU-R (F.595-6), Digital Millimeter Radio Link System.

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1 Introduction

A high frequency dual-loop frequency synthesizer is very complex to construct but it is a crucial functional block in telecommunication systems. It has the least trade-offs among all synthesizer structures. In a dual-loop frequency synthesis structure, one synthesizer loop operates in high frequency and consumes more power than other loops.

In wireless transmission systems, synthesizers are the heart of the system in which data transmission performances such as channel speed switching, signal purity and integrity are determined. Indirect synthesis such as dual-loop structure can offer these performance requirements unlike direct-digital synthesis (DDS) where the modulated signal is directly synthesized at the output frequency with adequate performance quality ([1–3]). The high resolution property allows not only a fine channel frequency selection, but accurate constant-amplitude continuous-phase modulation at the output frequency ([4]).

Figure 1 illustrates a general synthesizer block diagram.

The relationship between input reference frequency and output frequency is shown by equation (1):

$$F_{\text{output}} = \frac{M}{R} F_r. \tag{1}$$

The relationship between the output phase noise and reference frequency phase noise is as below:

$$\text{PN}_{\text{output}} = \text{PN}_r + 20 \log \frac{M}{R}. \tag{2}$$

For achieving an acceptable phase noise with good resolution, a dual-loop synthesizer structure is introduced, in which one loop generates low frequency with low step size, and the other loop generates high frequency with large step size. By mixing the output frequency of these two loops, a high frequency with low step size can be achieved.

A general dual-loop synthesizer block diagram is shown in Figure 2.

The output frequency equation is given by equation (3):

$$F_{\text{out}} = \frac{M_1}{R_1} F_{r1} + \frac{M_2}{R_2} F_{r2}. \tag{3}$$

For dual-loop synthesizers working in Ku band, one single loop in L band and one single loop in X-band are designed to achieve 18 GHz output.

The modeled phase noise contributed from each functional synthesizer loop block is shown in Figure 3.

Table 1 shows an extensive performance comparison between various synthesizer structures based on their performance.

2 Phase Noise Modeling

Phase noise dictates the performance quality of the high-speed telecommunication transceivers. Phase noise in frequency-domain and jitter noise in time-domain are used to characterize digital micrometer wave link systems for high-speed radio application.

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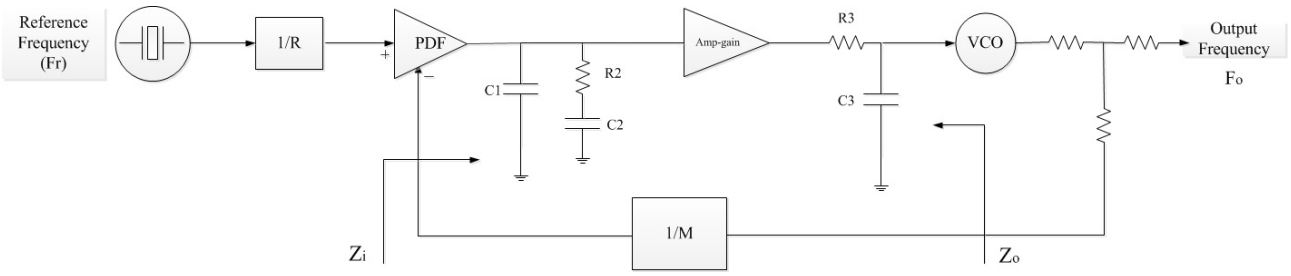

Figure 1. Basic single loop block diagram of a synthesizer.

In Figure 1, the third order loop filter, trans-impedance can be expressed as:

$$G(s) = \frac{Z_i(f) \times \frac{1}{i2\pi f C_3}}{Z_i(f) + R_3 + \frac{1}{i2\pi f C_3}}, \tag{4}$$

$$G(s) = \frac{i2\pi f R_2 C_2 + 1}{i2\pi f \times (i2\pi f R_2 C_2 C_1 + C_1 + C_2)}. \tag{5}$$

Generally, every functional loop block in the synthesizer is a noise source (intrinsic). All the intrinsic noise sources in the synthesizer loop are uncorrelated. Hence the power-spectrum density (PSD) noise at the output is the superposition of all the noise contributions from each block multiplied by their noise transfer function ([5]).

Reference noise N_{ref} is the phase noise contribution of reference oscillator in (f) offset frequency, and it can be modeled as:

$$N_{\text{ref}}(f) = N_{\text{ref}}(\Delta f)\frac{(\Delta f)^2}{f^2} + N_{\text{ref-floor}} \tag{6}$$

where $N_{\text{ref}}(\Delta f)$ is the phase noise at Δf offset frequency in the -20 dB/dec spectrum region, $N_{\text{ref-floor}}$ is the noise floor of the reference oscillator.

The noise from the reference oscillator in the output will be

$$N_{\text{ref,inoutput}} = N_{\text{ref}} N^2 H^2$$
$$\text{where} \quad H = 1 - \frac{1}{1 + \frac{H_0}{N}}. \tag{7}$$

Phase detector noise $N_{\text{PDF-ref}}$ is generated in transistor-level integrated-circuitry (IC) fabricated in factory, whose noise floor is proportional to $10\log(F_{\text{ref}}/1\text{ Hz})$. The actual noise is flat with respect to the operating frequency, and by setting a proper loop bandwidth, the effective N_{PFD} can be filtered out ([6]).

$$\log(N_{\text{PFD}}) = G_{\text{cl}}(f) \times \frac{N_{\text{PDF-ref}} + 10\log(\frac{F_{\text{ref}}}{1\text{ Hz}})}{20} \tag{8}$$

where $G_{\text{cl}}(f)$ is the close-loop gain of the synthesizer loop ([8]).

Loop filter noise N_{fil} can be modeled from noise current and the admittance of the loop filter, Y_{fil}.

$$N_{\text{fil}}(s) = 2 \cdot K \cdot T \cdot Re(Y_{\text{fil}}(s)) \tag{9}$$

where K is Boltzmann's constant, T is the absolute temperature, and Y_{fil} is $1/Z_i + 1/Z_o$, as shown in Figure 2, the complex admittance of the loop filter. Finally the loop filter contribution in output can be expressed as ([7, 8])

$$N_{\text{fil,inoutput}} = N_{\text{fil}}(s)\,|G(s)|^2 \left|\frac{K_{\text{VCO}}}{s}\right|^2 \cdot (1 - H^2) \tag{10}$$

Charge-pump noise N_{CP} exhibits flicker noise $(1/f)$ and thermal noise, which is proportional to the duty cycle α_{CP}. For a large α_{CP}, the flicker noise corner will be high and the generated thermal noise will be small compared to flicker noise ([8]).

$$N_{\text{CP,inoutput}} = N_{\text{CP}} \cdot |G(s)|^2 \cdot \left|\frac{K_{\text{VCO}}}{s}\right|^2 \cdot (1 - H^2). \tag{11}$$

VCO noise N_{VCO} can be modeled as

$$N_{\text{VCO}}(f) = N_{\text{VCO}}(\Delta f)\frac{(\Delta f)^2}{f^2}\left(1 + \frac{f_{c,\text{VCO}}}{f}\right) + N_{\text{VCO,floor}} \tag{12}$$

where $N_{\text{VCO}}(\Delta f)$ is the VCO phase noise at Δf offset frequency, $f_{c,\text{VCO}}$ is the $1/f^3$ noise corner of VCO and $N_{\text{VCO,floor}}$ is the noise floor of VCO. The VCO noise contribution in the output frequency can be expressed as ([6])

$$N_{\text{VCO,inoutput}} = N_{\text{VCO}}\,|1 - H|^2. \tag{13}$$

For uncorrelated noise sources, the respective noise spectra must be summed up to obtain total phase noise spectrum at the frequency synthesizer output.

$$N_{\text{total,inoutput}} = N_{\text{ref,inoutput}} + N_{\text{PFD,inoutput}} + N_{\text{CP,inoutput}} + N_{\text{fil,inoutput}} + N_{\text{VCO,inoutput}} + N_{\text{divider,inoutput}}.$$

The modeled phase noise contributed from each functional synthesizer loop block is shown in Figure 3.

Table 1 shows an extensive performance comparison between various synthesizer structures based on their performance.

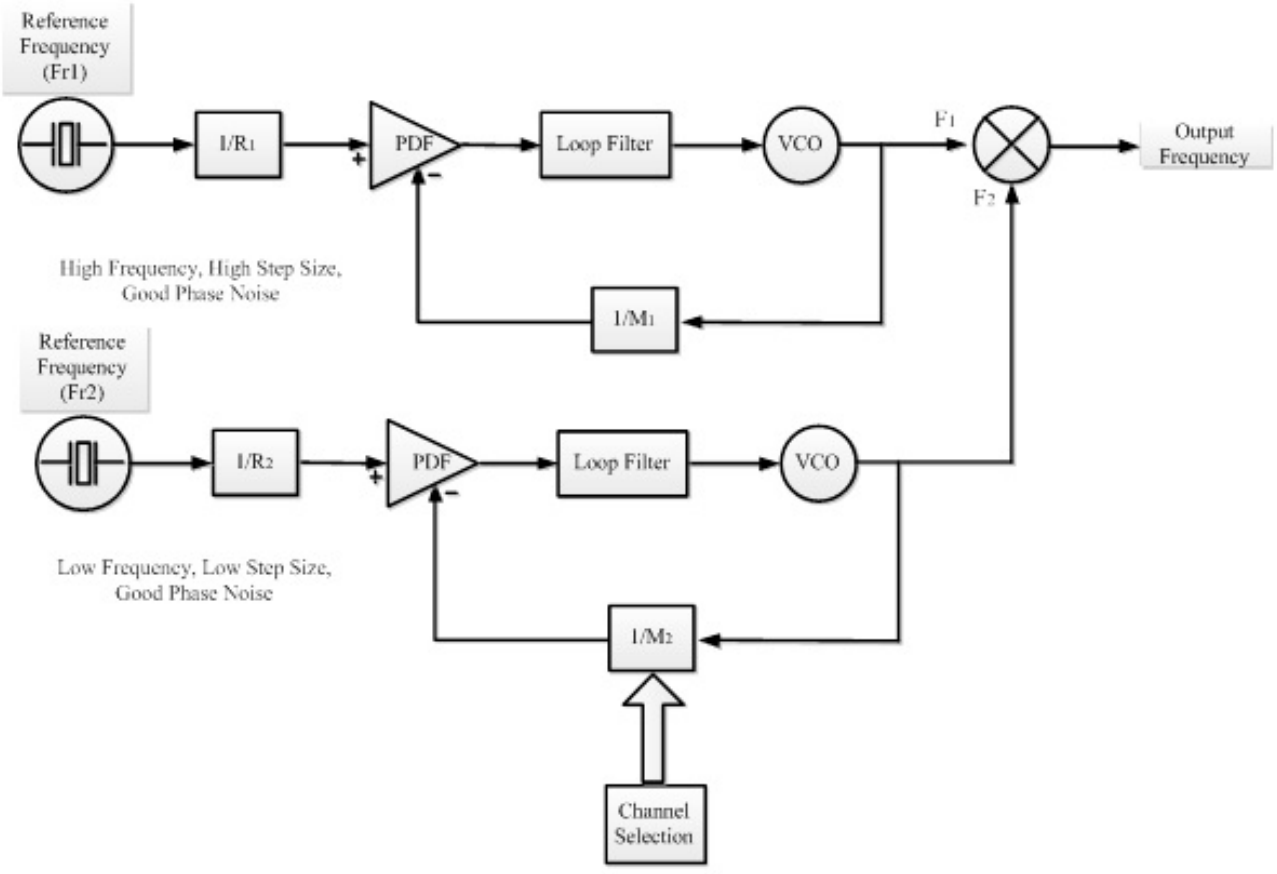

Figure 2. Basic block diagram of dual-loop synthesizer.

3 System Block Diagram

The block diagram of the 18 GHz synthesizer is shown in Figure 4. The structure is dual loop and thus there are two phase lock loops to generate the IF and LO signals. Both signals are combined in a sub harmonic mixer, generating the desired output frequency.

In the IF PLL, a TCXO10 is used as the reference of 10 MHz half sinewave signal. The used crystal's high phase noise performance (Table 3) and high slope in the lower edge of the signal are the main advantages of this chip which improves the phase detector efficiency.

For the phase detection part, a chip is selected that includes a phase/frequency detector and two internal digital frequency dividers M and R. The M and R values are determined by a programmable microcontroller and applied to the phase detector.

An MMIC is used as the VCO. This MMIC operates at 5 v, 10 mA DC bias. The output signal frequency of the VCO is in the 970–2150 MHz range and has a good phase noise as indicated in Table 2. The VCO's output signal is sampled and used as a feedback to PD.

In the fabricated synthesizer, the R and M values are programmed to be 5 and 518, respectively. The resulting

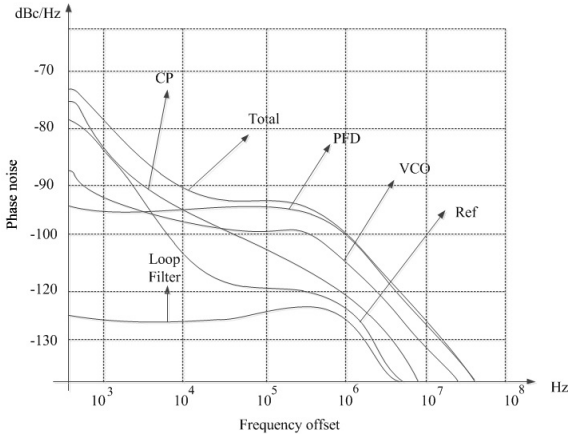

Figure 3. Modeled phase noise spectrum using the formulas.

output frequency signal f_{IF} in the locked loop state is equal to

$$f_{IF} = \frac{M}{R} f_r \Longrightarrow f_{IF} = 1036 \text{ MHz}. \qquad (14)$$

The IF signals is passed through an amplifier to have an acceptable power level at the mixer input. The schematic of

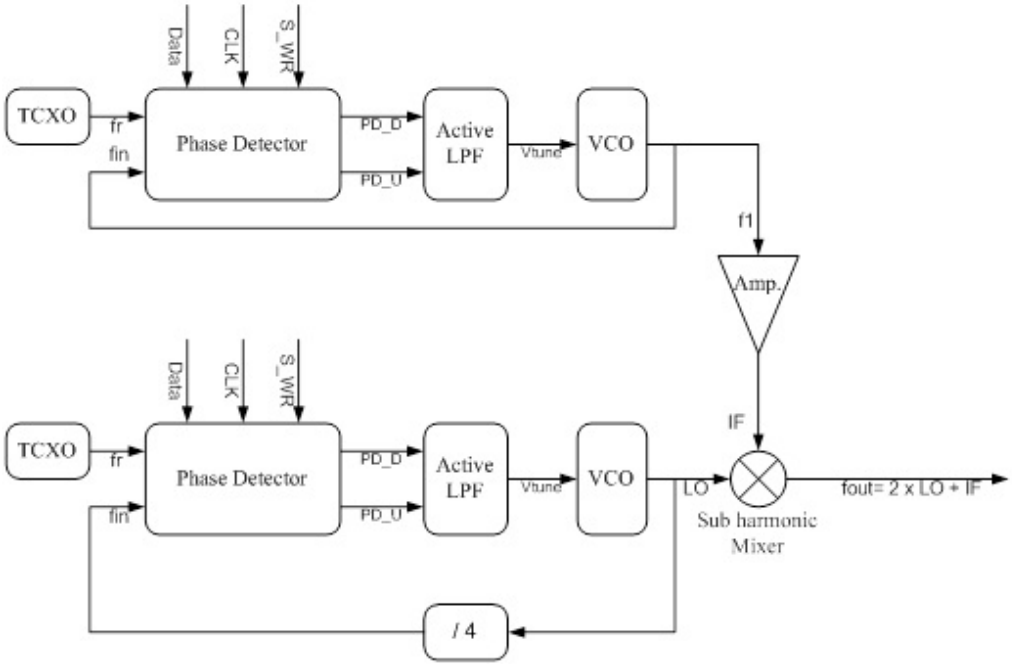

Figure 4. The 18 GHz synthesizer block diagram.

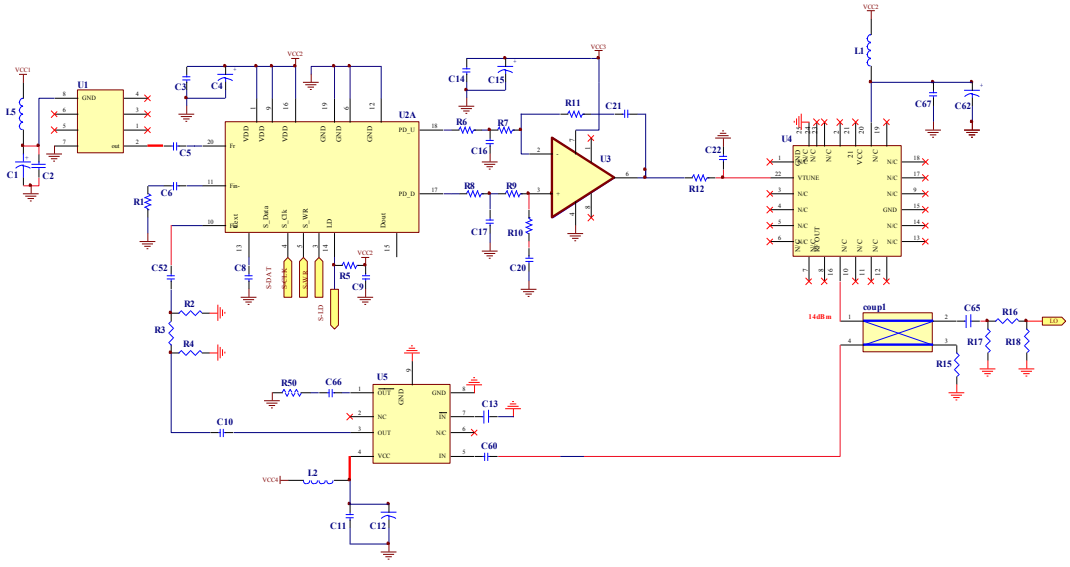

Figure 5. The IF PLL circuit schematic.

Reference	Frequency range (GHz)	Structure	Technology	Tuning (%)	Phase noise (dBc/Hz)	Supply voltage (V)	Spurs content (dBc)	Gain power
[9]	24	2 step up-conversion mixer	0.18um CMOS	5	—	2.5	—	26.5 dBm
[10]	13.9–15.6	Integer-N	0.18um CMOS	12.2	−103.8 @ 1 MHz	1.8	—	60 dBc
[11]	2–18	MMIC	0.2um PHEMT	88	−80 @ 100 KHz	—	< 55	—
[12]	17	Integer-N, QVCO	0.18um CMOS	16.5	−110 @ 1 MHz	1	—	—
[13]	6.3–9	Integer-N	0.18um CMOS	30	−109 @ 1 MHz	1.8	−52	—
[14]	10	Integer-N	0.18um CMOS	—	−102 @ 1 MHz	1.8	−48	—
[15]	22–29	Direct-conversion	0.18um SiGe BiC-MOS	24	−100.4 @ 1 MHz	1.8	−47	35/31 dB
[16]	24.2	Integer-N	0.18um CMOS	6	−106 @ 100 KHz	1	—	—
[17]	3.1–8	Integer-N, mixer	0.18um CMOS	158	−126 @ 10 MHz	1.8	—	81.5–85.2 dB
[18]	16–18.8	Integer-N	0.13um SiGe BiC-MOS	14.89	−90 @ 100 KHz	1.8	−65	—
this work	17.7–19.7	Dual-loop	Discrete	11.29	−81 @ 10 KHz	0–5.5	−57	51.83 dB

Table 1. Performance comparison between various synthesizer structures.

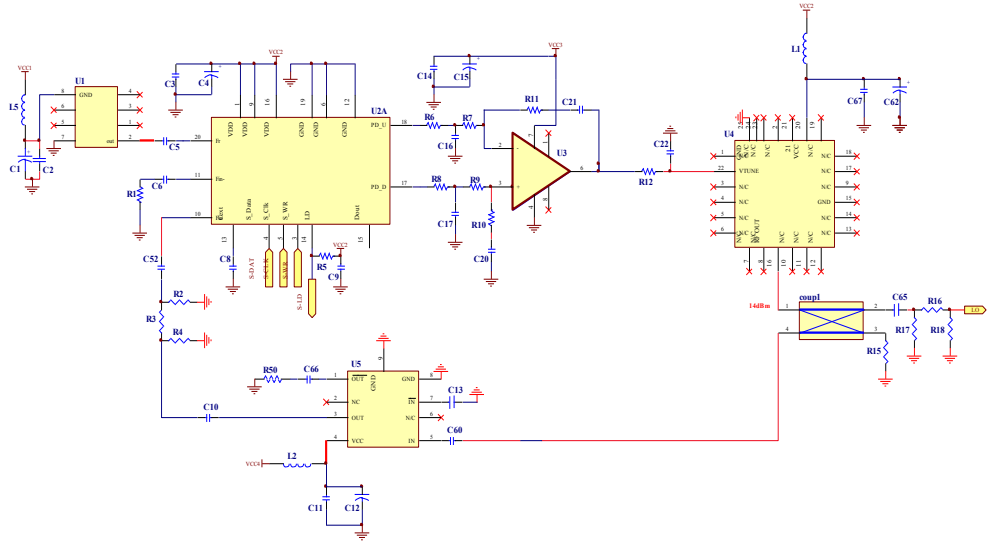

Figure 6. The LO PLL circuit schematic.

Offset frequency	Phase noise (dBc/Hz)
1 KHz	−70
10 KHz	−96
100 KHz	−118
1 MHz	−138

Table 2. VCO phase noise versus offset frequency.

Offset frequency	Phase noise (dBc/Hz)
1 KHz	−55
10 KHz	−85
100 KHz	−110
1 MHz	−125

Table 3. Xtal phase noise versus offset frequency.

the IF PLL is indicated in Figure 5. In the LO PLL, the reference frequency is generated by another TCXO, a product of RAKON Inc., to have a very low noise and high stability of 5 PPM. The phase noise versus offset is presented in Table 3 for this chip. The applied PD in the loop is the same chip as described in the previous section. An MMIC is selected for the VCO block. The MMIC has an operation frequency range of 7.8–8.7 GHz and is capable of changing the output frequency by a tune voltage of 1–11 v range. A 10 dB directional coupler is used to sample the output frequency, since the power level of the output is high enough (14 dBm). The sampled frequency is passed through a frequency divider, so $f_{\text{in}} = f_{\text{LO}}/4$.

The selected chip for the frequency divider block has a very low noise. Its operation frequency range is from DC to 12.5 GHz and its supply voltage and current are 5 v, 100 mA, respectively. In the fabricated synthesizer, M and R are set to 4 and 83, to provide the LO output signal frequency f_{LO}:

$$\frac{f_{\text{LO}}}{4} = \frac{M}{R} f_r \Longrightarrow f_{\text{LO}} = 8300 \text{ MHz}. \quad (15)$$

The schematic diagram of the LO PLL is shown in Figure 6.

Finally, the IF and LO signals are applied to a sub harmonic mixer in order to generate the required frequency. The sub harmonic mixer MMIC has a LO internal amplifier and its conversion loss is equal to 10 dB. The frequency ranges of IF and LO signals of this chip are DC 3 GHz and 7–10.5 GHz respectively.

Considering the sub harmonic mixer characteristic, the output signal frequency will be equal to

$$f_{\text{out}} = 2 \times f_{\text{LO}} + f_{\text{in}} = 17706 \text{ MHz}. \quad (16)$$

Figure 7 illustrates the schematic of the sub harmonic mixer.

The phase noise of the fabricated synthesizer is measured and presented in the next section.

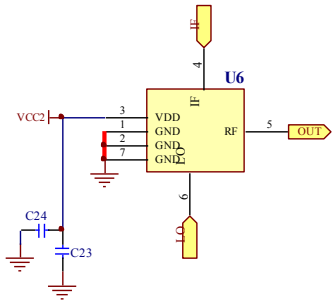

Figure 7. Modeled mixer circuit schematic.

4 Fabrication and Measurement Results

The synthesizer is fabricated and shown in Figure 8. The LO and IF PLL loop's VCOs have a phase noise around −90 dBc/Hz and −96 dBc/Hz at 10 KHz offset, respectively, according to their datasheets. The phase noise of the LO signal decreases by 10log2 factor, after multiplying by 2 in the sub harmonic mixer. Therefore, there are two signals at the sub harmonic mixer inputs: a signal with frequency of $2 \times f_{\text{LO}}$ and −87 dBc/Hz phase noise, and an IF signal with −96 dBc/Hz phase noise. The output signal phase noise follows the $2 \times f_{\text{LO}}$ signal phase noise considering the higher phase noise of the IF signal. So a phase noise of −84 dBc/Hz is predicted for output signal because of the sub harmonic mixer characteristic.

Measurement results of the fabricated synthesizer are shown in Figure 9. The frequency spectrum is observed by an HP8563A spectrum analyzer. The frequency span, RBW, and VBW are set to 50 KHz, 1 KHz, and 30 Hz, respectively. The difference between carrier and 10 KHz offset power level is equal to −51.83 dB, as indicated in Figure 9. Thus the phase noise of the output signal is obtained by the following relation ([10, 11]):

$$\begin{aligned} \text{Measured phases noise} &= -51.83 - 10 \log \text{RBW} \\ &= -81.83 \text{ dBc/Hz}. \end{aligned} \quad (17)$$

Phase noise at 1 KHz and 100 KHz offset are −60 and −100 dBc/Hz, respectively. Spur frequency contents are measured at −57 dBc. The predicted performance parameters such as gain, spur contents and phase noise are in comparable to the measured results. The comparison results indicate that the phase noise of the system is superior to its rivals.

5 Conclusion

The modeling representations of all intrinsic phase noise spectrum sources of frequency synthesizer loop are discussed. The block-circuit analysis of a dual-loop synthesizer is presented. A carefully calculated frequency resolutions and design parameters in each loop are analyzed. This

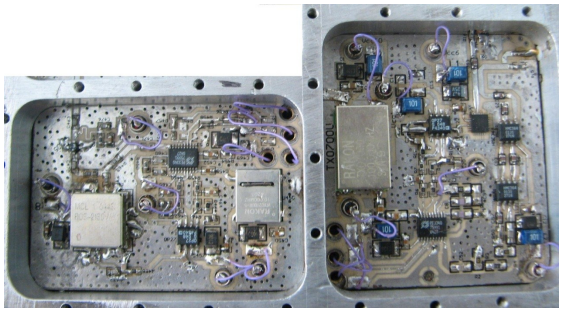

Figure 8. The fabricated synthesizer.

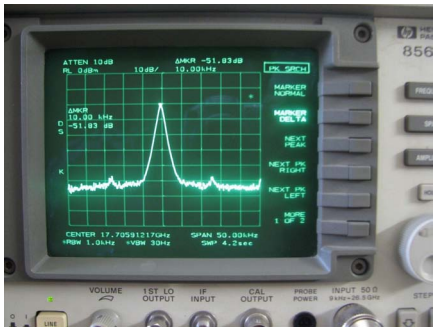

Figure 9. The measurement result.

method is proposed to dramatically reduce the phase noise effect in output oscillating frequency due to performance trade-offs in all the other synthesizer loop structures. In this paper, the methodology analysis of dual-loop frequency synthesizer and spur frequency contents and phase noise are analyzed. The performance comparison between the proposed method and previous works in this frequency is presented. The channel switching is fully programmable for 17.7–19.7 GHz frequency range. Test results indicate that the fabricated synthesizer has a phase noise of −81 dBc/Hz, much superior to the phase noise reported in the references.

Acknowledgments

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