III-V-on-Si Transistor Technologies: Performance Boosters and Integration

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Abstract— In this work, we review progress in III-V transistor technologies. Key approaches for silicon integration are described, with a distinction being made between large area layer transfer and selective growth techniques. We show how the integration approach must be tailored for the intended application to maximize performance, functionality and minimize cost. We also highlight performance boosters such as heterostructure channel stacks, which offer increased carrier mobility towards improved RF and RF-CMOS performance. Recent progress in tunneling field-effect transistors (TFETs) have enabled the TFET architecture as a process module, allowing for dense integration with MOSFETs on the same chip towards an extremely low-power CMOS technology. Finally, we highlight emerging applications for III-V devices at cryogenic temperatures, where there is a rising need for low-power electronics to support the scaling of quantum computers. The unique properties of III-V, their high mobility and band gap engineering make them highly suitable for this application.

Introduction

III-V electronics based on the InGaAs(Sb) system have attracted significant research attention over the last 15 years, due to the high carrier mobilities of the III-V materials and the potential for band gap engineering [1]–[3]. Several key applications for III-V field-effect transistors (FETs) have crystallized in this time period, in both the high-frequency and low-power logic domains [1], [3]. For logic applications, high electron mobility III-Vs such as InGaAs has already been shown to enable NFETs that clearly outperform Si CMOS in several key logic power metrics, though high-performance III-V PFETs using GaSb remain challenging to realize due to typically high defect densities near the valence band [4]. Meanwhile, CMOS has scaled to gate lengths, L_G, below 30 nm and has entered the quasi-ballistic regime, where there is less of a need for high mobility. III-V tunneling FETs (TFETs) have instead emerged as strong contenders for low-power logic applications [5], [6]. While integrated III-V channels on Si were intended as performance booster modules in CMOS, TFETs instead appeared as a disruptive technology due to their need for relatively complex heterostructures [5]. Therefore, there is significant research required to establish the commercial viability of TFET technology. However, recent progress in TFETs is highly promising and as more and more research groups are achieving TFETs with subthermionic subthreshold swings, our understanding of TFET properties is expanding rapidly [7], [8]. Regardless of how III-Vs will impact CMOS technology, it has become clear that Si integration is a requirement for commercial viability. The plethora of different integration techniques explored in

litterature demonstrates this fact: From layer transfer techniques such as direct wafer bonding, to selective epitaxy based on aspect ratio trapping and nanowires [9], [10]. The optimal integration route remains an open question but will likely depend on the device type at hand and the intended application.

In the high-frequency domain, III-V FETs such as InP/InAs HEMTs are important in low-noise amplifiers (LNAs) and have found a stable niche within the landscape of commercial amplifiers [11], [12]. While there has been promising research on the implementation of thin gate oxides in HEMTs in order to improve scaling, in terms of key performance metrics, power dissipation is becoming increasingly important [13]. A key emerging research challenge here is within quantum computing. Inside the quantum computer cryostat, at a temperature of 3 K, the low-power qubit signal must be amplified by around 30 dB in order to be transferred out of the cryogenic environment [14], [15]. This gain must be provided with very little added noise and is today done by InP HEMTs. However, one such HEMT consumes around 5 mW of DC power. As qubit scaling roadmaps target over 1000 qubits by 2023, this implies a need to amplify approximately 100 qubit channels (assuming a 1:10 readout multiplexing). Within 10 years, the qubit number could be as large as 1 million. Clearly, to enable efficient readout of such complex quantum computers, LNA technology must evolve. Therefore, there is a need to elucidate the cryogenic properties of III-V materials and devices in order to enable technologies tailored for this environment. In this paper, we review recent progress in III-V transistor technologies integrated on Si, to provide an overview of key performance boosters and the challenges to further mature III-V devices.

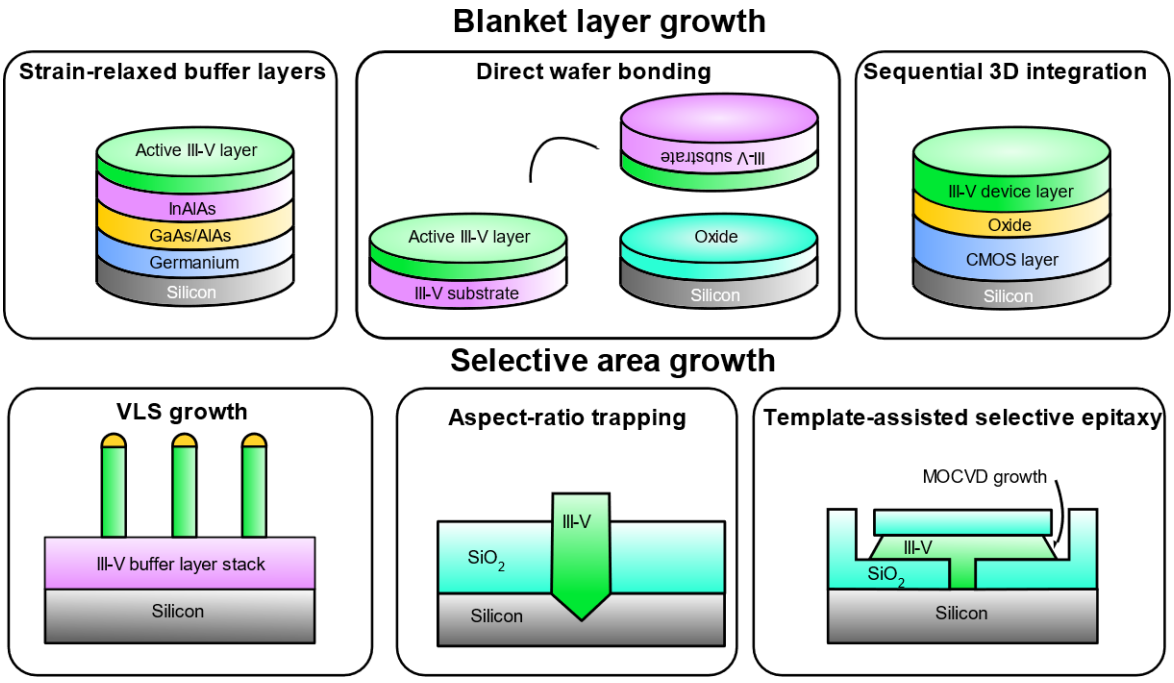

Figure 1: Various approaches that have been explored to integrate III-V materials on Si substrates.

Integration of III-Vs on Si

Figure 1 shows an overview of various integration approaches for III-V-on-Si explored in litterature. We make a distinction between blanket layer growth and selective epitaxy, where selectivity between the substrate and an oxide masking determines the regions of growth. The latter allows local integration of III-Vs and as such enables tighter integration with CMOS devices (in a hybrid technology). A more economical use of III-V materials is also a benefit of selective epitaxy.

Strain-relaxed buffer layers using metamorphic buffers falls in the category of blanket layer growth techniques. Promising transistor results using this technology were demonstrated by Huang et al. [16], showing a scaled ultrathin body InAs MOSFET on an GaAs/InP/InAlAs metamorphic layer stack grown by MOCVD. A surface roughness RMS of 6.9 nm indicates that obtaining high-quality III-V layers on such buffers is challenging. A direct comparison with the equivalent technology on InP showed approximately a 50% reduction of the on-current I_{ON} at fixed off-current I_{OFF} and drive voltage V_{DD} [17]. Further improvements to the buffer layer growth stack have been shown to result in increased mobility, showing a path forward for this technology [18].

In the direct wafer bonding (DWB) integration technique, the III-V growth can be done lattice-matched on a donor wafer thus suppressing the formation of mismatch-related defects [19]. The donor wafer with the grown active layer (III-V-on-III-V) is put into physical contact with a target wafer, after coating both surfaces with an adhesive oxide (Al_2O_3). After annealing the wafer stack at around 300^{o}C, the donor wafer can be removed. To recycle the InP substrate, a smart cut technique can be utilized [20], [21]. The resulting structure is III-V-on-BOX, which is ideal for applications requiring strong electrostatic control, such as logic. High-performance transistor demonstrators have been achieved using DWB by several groups, even with logic performance surpassing that of state-of-the-art Si CMOS technology [22]–[25]. The main limitations of DWB include challenging integration of large-area wafers (though 200 mm transfer was achieved [26]) and reduced carrier mobility of transferred layers. Hybrid integration approaches combining DWB and buffer layers have also been explored to demonstrate co-integration of III-V NFETs and Ge PFETs by first transferring a Ge active layer by DWB and subsequently growing an InGaAs active layer on top of GaAs/GaSb buffers [27]–[29].

A further development of DWB integration is sequential 3D integration. In this scheme, the active III-V layer is tranferred by DWB on top of a highly planarized already fabricated device layer [30]. Following, the III-V device layer is fabricated sequentially. Compared to packaging-based 3D integration, this approach has the benefit of allowing tight integration between the device layers down to the resolution of the lithography tool [31], [32]. III-V device layers are suitable as top-layers in 3D

stacks due to their relatively low process thermal budget [33]. Junctionless III-V FETs particularly interesting for this purpose since they can omit the high-temperature source/drain regrowth step [34]–[37]. Planarization of surfaces is a key challenge in this approach, particularly those of the already fabricated layers which exhibit relatively large topographies. Planarization down to <0.5 nm is necessary for all surfaces. Moreover, care must be taken to avoid outgassing from the thick planarization oxides on top of the fabricated layers, which can degrade carrier mobility.

Selective area epitaxial integration approaches have also reported excellent device performance. Vapor-liquid-solid (VLS) metal-catalyzed vertical nanowires can produce defect-free and extremely scaled III-V channels. Transistors using these channels have reported among the highest values of transconductance to date for FETs, over 3 mS/µm [38]. A key aspect of the technology is that it allows highly efficient band gap engineering in III-V heterostructures as the scaled nanowire dimensions suppress defect formation due to strain-relaxation at the III-V/Si interface [2], [3]. Selective epitaxy using growth masks can also produce vertical nanowires (without the use of a catalyst) as well as arbitrary shapes. Although high-material quality may be achieved in this fashion, the high-aspect ratio makes the fabrication of advanced vertical nanowire devices in a VLSI process challenging. Furthermore, the capability for the growth of in-situ homo-and heterojunctions is somewhat off-set by the non-zero radial growth rates, which often leads to an overgrowth of such junctions.

Aspect ratio trapping (ART) is a technique whereby line defects are terminated at the walls of the growth structure before reaching the active area of the grown III-V layer [9]. This is done by crystal plane engineering through growth at selective Si planes. To apply standard CMOS fabrication techniques, a planar active region is typically desirable, which can be arrived at by subsequent chermical mechanical polishing steps (ref). Template-assisted selective epitaxy (TASE) is an alternative to ART which allows the direct integration of such quasi-planar III-V crystals [39]. In TASE, a hollow oxide cavity is first fabricated using a sacrificial material which is selectively etched [40]. In the cavity, the Si seed area is exposed, from which growth initiates. By engineering of the growth template, the defect lines can be terminated at the inactive part of the III-V crystal. Promising FET demonstrators have been shown using both ART and TASE [9], [39].

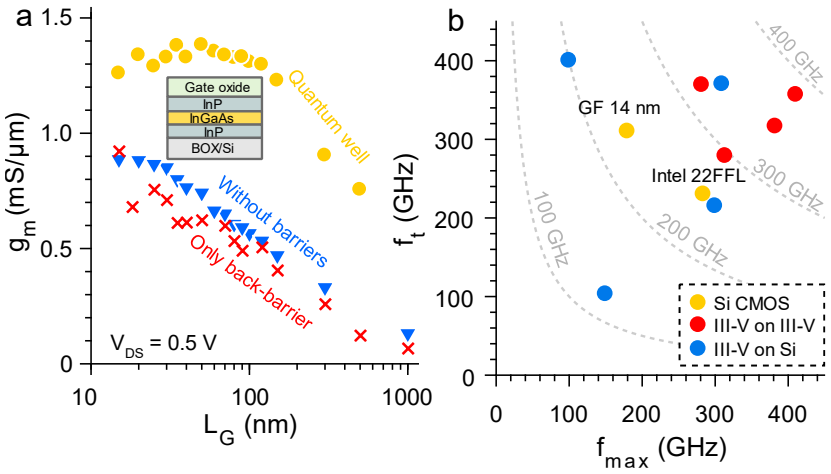

Figure 2: (a) Transconductance versus gate length for three different channel heterostructures. The devices with quantum wells have the channel heterostructure shown in the inset. The structure without barriers is lacking both InP barriers, and the structure with only back-barrier is lacking the top InP barrier. (b) Benchmark of high-frequency properties of demonstrated III-V and Si FETs. Devices shown here are suitable for both logic and RF, i.e. towards an RF-CMOS technology.

III-V Performance Boosters

Realization of high-performance FETs on integrated III-V layers depends on optimization of several key process modules: channel structure, gate oxide, ohmic contacts, electrostatics, device designs and scalability, to name a few. Channel structure optimization has received significant research attention. While InAs is a promising channel material for NFETs due to its high bulk electron mobility, its narrow band gap makes it susceptible to band-to-band tunneling increasing off-currents, and poor electrostatic control [1]. It's low density of states (DOS) is also a concern for extremely scaled devices. Ultrathin channel thicknesses down to 3 nm improve electrostatic control but relatively high I_{OFF} remains a challenge for short gate lengths [41]. Gate all-around structures such as in vertical nanowire FETs are promising to further increase electrostatic control. Nonetheless, in terms of gain and current density, InAs channels are the superior choice, as demonstrated by several groups in FETs with transconductance g_m above 3 mS/µm, very high on-currents at fixed off-currents, and as is clear by the adoption of InAs/InP HEMT technology in state-of-the-art LNAs [38], [42]–[45]. InAs channels are typically used in a quantum well architecture, with thin InGaAs top and bottom barriers.

InGaAs channels (with In content around 0.53-0.8) can offer an attractive compromise between off-state and on-state performance. For the barriers in InGaAs quantum wells, InP is a promising choice. Figure 2a shows g_m versus L_G for InGaAs MOSFETs with three different channel architectures: (1) Quantum well structure with 3 nm InP/10 nm InGaAs/20 nm InP integrated on Si using DWB, (2) a similar structure but using only the bottom 20 nm InP barrier and (3) a structure without any InP barriers [46]. From measurements of on-state resistance, field-effect mobilities of 1500 and 500

cm^2/Vs were determined for structures (1) and (2), (3), respectively. This is reflected in the g_m at long gate lengths where the devices are operating in the drift-diffusion regime and g_m is linearly proportional to the electron mobility. At short channels lengths the device is operating in the quasi-ballistic regime and the dependence is no longer linear [47]. At such gate lengths the quantum well offers a 60% boost of g_m. The back-barrier InP offers here no benefit over the barrier-less structure, indicating that mobility is limited by scattering at the front interface, rather than the back-interface to the BOX layer. While quantum well structures invariably decrease gate capacitance through an increase of the effective oxide thickness (EOT), they present a key design parameter to tune the low-power performance to the optimum point. In particular, QWs can enable RF-CMOS applications (i.e. both logic and high-frequency) leveraging the large gain towards higher cut-off f_t and maximum oscillation frequencies f_{max} [48]. Figure 2b shows a benchmark of state-of-the-art III-V MOSFETs and their RF performance towards such applications [49]. While III-V-on-III-V FETs have shown the highest f_t/f_{max}, the gap to III-V-on-Si technologies is rapidly shrinking with the highest reported f_t now being on Si [50]–[52]. In comparison with state-of-the-art Si RF-CMOS, III-Vs are here already outperforming, indicating that RF-CMOS is a key potential application for III-V technologies. These types of devices are also promising for implementing 1T DRAM, which has been shown to result in low-power and highly scaled memory cells [53]. These types of memories make use of charge retention in the channel, which is controlled by a body contact and can leverage the high mobilities of III-Vs towards lower power operation.

For strictly high-frequency applications such as in LNAs, the combination of QW and gate oxide – the MOSHEMT structure – is promising to optimize the trade-off between gate leakage and the scalability of gain and currents [54], [55]**.** Scaling of HEMTs to ultra-short gate lengths <20 nm must be accompanied by scaling of the gate barrier to avoid short-channel effects. Due to the narrow band gap of the barrier material, this scaling can result in a sharp increase of the off-current. By implementing both a thin gate oxide and thin top-barrier, the device could exhibit both strong electrostatics and high mobility. Experimental realizations of this technology have already shown g_m = 2.2 mS/um and f_{max} above 600 GHz as well as high-performance LNAs [13], [56].

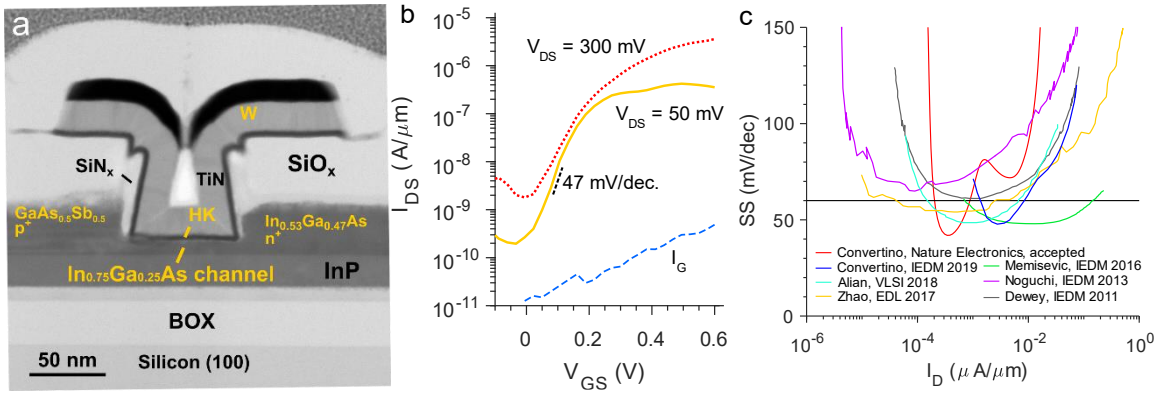

Figure 3: (a) Bright field STEM image of the cross-section of a CMOS-like TFET device. (b) Associated transfer characteristics of a similar devie. (c) Benchmark of subthreshold swings for state-of-the-art TFET devices.

III-V Tunneling Field-Effect Transistors

The tunneling field-effect transistor (TFETs) is a promising new low-power transistor that can overcome the thermal limit of the subthreshold swing SS in standard FETs [5], [6], [57]. Standard FETs have an SS limited to 60 mV/decade at room temperature due to thermionic injection of carriers over the channel potential [57]. The transfer characteristics in the subthreshold regime are determined by the Fermi-Dirac distribution of the carriers in the conduction band and are thus temperature-dependent. Since SS gives the voltage swing required to achieve one order of magnitude change of the current, it will limit how low the drive bias V_{DD} can be reduced without increasing the off-current above the highest acceptable level. Thus, SS will limit V_{DD} and in turn the total dissipated power in the device $P_{tot} = CV_{DD}^2 f(V) + I_{off}V_{DD}$, where C is the capacitance of the device. As V_{DD} has been a historically important parameter to tune in order to reduce power density and allow higher transistor densities, the thermal limitation of SS is a serious challenge to scaling. While there have been several sub-thermal device architectures proposed in literature, the TFET is perhaps the most promising [5]. The TFET operates by implementing a Fermi filter using a tunneling barrier [6]. The Fermi filter is a feature which opens a tunneling path for carriers inside the Fermi-Dirac distribution, i.e. it filters out the high-energy tail which gives rise to the 60 mV/decade limit in standard FETs. Typically, the TFET is implemented in a heterostructure p-i-n structure and operates by field-effect control of the heterojunction diode at the interface of the i-region, and the n- or p-doped source region, respectively for an n-TFET or p-TFET. A tuneling path from the valence band (p-TFET) of the source-side material to the conduction band of the i-region.

TFETs have been implemented in a wide range of very different device architectures and material systems [58]–[60]. The most successful demonstrations have been those that can achieve both accurate material control of the III-V heterostructure, and a scaled channel with strong electrostatic

control. In fact, electrostatic control has been shown to be essential to achieving deep sub-60 mV/decade operation [61]–[63]. The vertical nanowire architecture has been remarkably successful here, with reports of SS around 40 mV/decade and relatively high on-state current levels [7]. The reasons for the success of vertical nanowires here are that they can implement complex heterostructures with minimal defect formation as well as obtain highly scaled and electrostatically efficient gate-all-around channel structure. While several groups have now reported TFETs with sub-thermal operation, the question of the technological viability of TFETs remain [8], [64], [65]. To establish such viability, several challenges must be solved relating to CMOS compatibility, Si integration, self-aligned process steps, co-integration with MOSFETs and scalability.

While the TFET is considered a unique transistor architecture, by careful process design, the TFET structure can be implemented locally in a III-V FET technology platform. In this sense, it can function as a performance booster module in such a technology platform. This was demonstrated experimentally in Convertino et al. [66]. The fabrication process mirrored a standard CMOS process with replacement metal gate and regrown raised S/D. The TFET module was implemented by a masking of the source-side during n^+ contact growth. Subsequently, the n^+ growth area was masked and the p+ growth was performed locally at the location defining the TFETs (Figure 3a). Following that, the fabrication flows were identical for both FETs and TFETs. The resulting TFETs showed excellent off-state performance with SS = 47 mV/decade at L_G around 30 nm (Figure 3b and 3c) and represent the first demonstration of a CMOS-like and highly scalable TFET platform, allowing fro the hybrid integration of MOSFETs and TFETs.

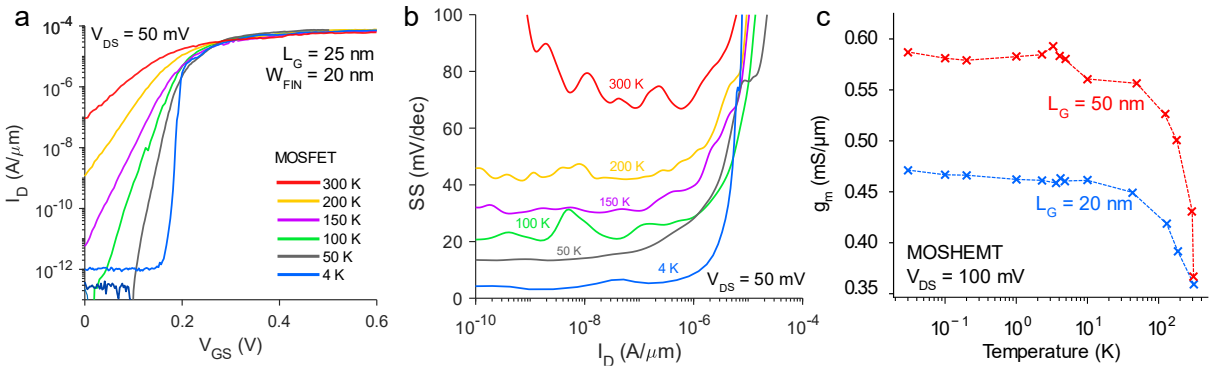

Figure 4: Temperature-dependent transfer (a) and subthreshold (b) characteristics of a III-V FinFET devices. (c) Transconductance versus temperature for a MOSHEMT device.

Cryogenic III-V Devices

Cryogenic electronics is a field that is gaining increased research attention recently for its use in a wide range of applications, from space, radio astronomy, physics and high-performance computing [15], [67]. In quantum computing, cryogenic electronics can support the increase of quantum bit density in the quantum processor [68]. These electronics can replace some of the standard room-temperature

systems with integrated ICs that reduce the complexity of the overall quantum architecture [69]. III-V materials are particularly interesting for cryogenic environments, where the cooling power is typically limited, especially at temperatures below 3 or 4 K [70]. As III-Vs excel as low-power devices due to their high carrier mobilities, they are promising for these kinds of environments. Moreover, in a quantum computer, the readout path already today contains III-V technology in the cryogenic LNAs that are amplifying the quantum bit signals as they are transferred to room-temperature equipment [71].

To allow tailored cryogenic transistor technologies, the cryogenic device properties must be thoroughly understood. Modeling of cryogenic Si CMOS has advanced significantly over the years, and similar work must be done for III-V devices [72]. Figure 4a shows the transfer characteristics for III-V n-type FinFETs with L_G = 25 nm at temperatures from 300 K to 4 K. The corresponding subthreshold swings are shown in Figure 4b. As expected from the thermal injection transport mode of these devices, SS is sharply decreased at cryogenic temperatures and reaches a minimum value of around 5 mV/decade. Simultaneously, the threshold voltage shifts by around 200 mV. Due to the V_T shift, operating this device at a low V_{DD} in order to leverage the reduced SS will not result in an improvement of performance. Rather, the technology must be designed with prior knowledge of the V_T shift, in order to achieve a proper value of V_T at the intended operating temperature. V_T tuning using a body contact is a promising approach to achieve this type of tunability, and can result in a factor 2 increase of the on-current at fixed off-current for Si CMOS [73].

Changes to the on-state FET characteristics are by different mechanisms. Figure 4c shows the transconductance g_m at V_{DS} = 100 mV versus temperature for two gate lengths, 50 and 20 nm, MOSHEMTs integrated on Si. A boost in g_m of 60% and 30%, respectively, is observed for these devices, going from 300 K to a few K. Most of the boost occurs already at a few tens of kelvin. The larger g_m for the longer gate length device can be explained by short-channel effects, whereby a larger output conductance will reduce the extrinsic transconductance. The increase of g_m can be attributed to a reduction of phonon-electron scattering in the channel and corresponds to approximately 2-3 times increase of electron mobility. The reduced boost of the short-channel g_m is consistent with the quasi-ballistic transport expected in such scaled and high-mobility channels. In essence, the shorter the channel, the lesser is the impact of mobility on the current [74]. The cryogenic mobility-enhancement observed in these III-V MOSHEMTs is much stronger than other reports on III-V MOSFETs [75]. The reason is likely that scattering in such devices is to a larger degree coulomb-based scattering at the oxide interface due to ionized impurity which is not strongly temperature-dependent.

Scaled III-V quasi-1D channels can at cryogenic temperatures exhibit step-like current features related to quantized conductance [76]–[78]. While these types of devices can provide insights into the operation of FETs at the scaling limit, they also exhibit effects that can be leveraged towards new types of devices. For instance, at one of the current-steps due to quantized conductance, the transconductance is predicted to significantly increase above the room-temperature value. Experimental realizations have shown an increase of more than a factor 2, while theory predicts that even an order of magnitude increase is possible [79]. This increased g_m can be traded off for reduced operating bias, indeed it is only visible at extremely low biases of less than 50 mV. A transistor utilizing this effect was proposed and simulated, showing the potential of 50x reduction of DC power in cryogenic LNAs [80]. Due to the low linearity of the device, the applications are limited to those requiring low input powers. However, qubit readout is exactly such an application, making this type of device highly suitable for scalable qubit readout stages.

Conclusions

In this work, we have reviewed key progress in III-V transistor technologies and highlighted promising performance boosters, fabrication modules and silicon integration approaches. While integration work continues to be a rich research topic, a division between large area layer transfers and local III-V integration using selective growth techniques has become clear. The choice for implementation in a commercial technology will depend on the application at hand – for low-cost and dense integration with Si technologies on the same layer the selective growth methods are likely superior, while layer transfer methods are promising for 3D integration schemes. In terms of performance boosters, channel engineering has received much attention, and the implementation of MOSHEMT architectures represents a key path forward for both RF and RF-CMOS applications. Recent progress in TFETs has shown that this once exotic device in fact can be implemented as a performance booster in a standard III-V FET fabrication flow using Si CMOS-like methods and device architecture. As CMOS has now scaled to the deeply quasi-ballistic transport regime, the need for mobility booster such as III-V channels is less. On the other hand, the power density issue stemming from the thermal limitation of off-state characteristics is becoming more severe, for which III-V TFETs are one of the most promising solutions. Finally, cryogenic temperature has emerged as a highly interesting arena for III-V electronics, where their unique properties, mobilities and band gap engineering could be leveraged for new cryogenic devices. Key challenges in the scaling of quantum computers require that new ultra-low power devices be developed, for which III-V materials are highly promising.

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