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VERIFICATION OF DRIVER LOGIC USING AMBAAXI UVM

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ABSTRACT

Advanced Extensible Interface (AXI) is the most commonly used bus protocols in the day-to-day because of its high performance and high-frequency operation without using complex bridges. AXI is also backwardcompatible with existing AHB and APB interfaces. So verification of driver logic using AMBA-AXI UVM is presented in this paper. The AXI is used for multiple outstanding operations which is only possible in the other protocol but it is possible in AXI because it contains different write address and data channels and AXI also supports out of order transfer based on the transaction ID which is generated at the start of the transfer. The driver logic for the AXI has been designed and implemented using the Universal Verification Methodology (UVM).The signaling of the five channels such as write address, write data, write response, read address, read data channel of AXI protocol are considered for verification. According to the AXI protocol,the signals of these channels are driven to the interconnect and results are observed for single master and single slave. The driver logic has been implemented and verified successfully according to AXI protocol using the Rivera Pro. The results observed for single master and single slave have shown the correctness of AMBA-AXI design in Verilog.

KEYWORDS

AMBA(Advance Microcontroller Bus Architecture),AXI(Advanced Extensible Interface),UVM(Universal Verification Methodology),channel.

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VLSI DESIGN OF AMBA BASED AHB2APB BRIDGE

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ABSTRACT

The Advanced Microcontroller Bus Architecture (AMBA) is an open System-on-Chip bus protocol for highperformance buses to communicate with low-power devices. In the AMBA Advanced High Performance bus (AHB) a system bus is used to connect a processor, a DSP, and high-performance memory controllers where as the AMBA Advanced Peripheral Bus (APB) is used to connect (Universal Asynchronous Receiver Transmitter) UART. It also contains a Bridge, which connects the AHB and APB buses. Bridges are standard bus-to-bus interfaces that allow IPs connected to different buses to communicate with each other in a standardized way. So AHB2APB bridge is designed, implemented using VERILOG tool and tested using Verilog testbench and is reported in this paper. A synthesizable RTL code of a complex interface bridge between AHB and APB is developed and known as AHB2APB Bridge. The simulated AHB2APB Bridge results are promising and can be further tested for its verstality by writing a verification program using UVM in future.

KEYWORDS

AMBA; AHB2APB; SOC; VERILOG; XILINX

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DESIGN AND IMPLEMENTATION OF CAR PARKING SYSTEM ON FPGA

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ABSTRACT

As, the number of vehicles are increased day by day in rapid manner. It causes the problem of traffic congestion, pollution (noise and air). To overcome this problem A FPGA based parking system has been proposed. In this paper, parking system is implemented using Finite State Machine modelling. The system has two main modules i.e. identification module and slot checking module. Identification module identifies the visitor. Slot checking module checks the slot status. These modules are modelled in HDL and implemented on FPGA. A prototype of parking system is designed with various interfaces like sensor interfacing, stepper motor and LCD.

KEYWORDS

Finite State Machine; Parking System; Virtex- 5;

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MULTISIM DESIGN AND SIMULATION OF 2.2GHZ LNA FOR WIRELESS COMMUNICATION

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ABSRACT

This paper presents the work done on the design and simulation of a high frequency low noise amplifier for wireless communication. The purpose of the amplifier is to amplify the received RF path of a wireless network. With high gain, high sensitivity and low noise using Bipolar Junction transistor (BJT). The design methodology requires analysis of the transistor for stability, proper matching, network selection and fabrication. The BJT transistor was chosen for the design of the LNA due to its low noise and good gain at high frequency. These properties were confirmed using some measurement techniques including Network Analyzer, frequency analyzer Probe and Oscilloscope for the simulation and practical testing of the amplifier to verify the performance of the designed High frequency Low noise amplifier. The design goals of noise figure of 0.52dB- 0.7dB and bias conditions are Vcc = 3.5 V and Icc= 55 mA to produce 16.8 dB gain across the 0.4–2.2GHz band.

KEYWORDS

Amplifier, Bipolar Junction Transistor, Stability, LNA, Fabrication, Multism

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EVALUATION OF ATM FUNCTIONING USING VHDL AND FPGA

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ABSTRACT

It has been almost four decades that banks and other financial organizations have been gradually computerised, in order to improve service and efficiency and to reduce cost. The birth of Electronic Fund Transfer and Automated Teller Machines has given rise to 24-hour banking and a greater variety of services for the customer. This method uses a computer to transfer debits and credits, with the help of electronic pulses, which are carried through wires either to a magnetic disk or tape. ATM (Automated Teller Machine) has become an important part in our daily lives. People use ATM for various purposes such as money withdrawal, checking balance, changing password etc. Since it mainly deals with people's money, it has to be a secure system on which we can rely. We have taken a step towards increasing this security and integrity by trying to implement the functioning of an ATM using VLSI-based programming, HDL(Hardware Description Language).The conventional coding languages such as C,C++ are replaced by VHDL(Very High Speed Integrated Circuit Hardware Description Language) so that the code cannot be easily hacked or changed. This article consists of an insight into the various functions that can be performed using an ATM, a brief description of the Coding and the obtained simulation results. It also consists of the implementation of the code using FPGA Kit (Spartan3; Model no.-XC 3S50).

KEYWORDS

ATM (Automated Teller Machine), Security, HDL (Hardware Description Language), FPGA (Field Programmable Gate Array).

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EXTENDED K-MAP FOR MINIMIZING MULTIPLE OUTPUT LOGIC CIRCUITS

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ABSTRACT

Minimization of multiple output functions of a digital logic circuit is a classic research problem. Minimal circuit is obtained by using multiple Karnaugh Maps (K-map), one for each function. In this paper we propose a novel technique that uses a single Karnaugh Map for minimizing multiple outputs of a single circuit. The algorithm basically accumulates multiple K-Maps into a single K-Map. Finding minimal numbers of minterms are easier using our proposed clustering technique. Experimental results show that minimization of digital circuits where more than one output functions are involved, our extended K-Map approach is more efficient as compare to multiple K-Map approach.

KEYWORDS

Boolean Algebra, Karnaugh Map, Digital Logic Circuit, Clustering.

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SINGLE ELECTRON TRANSISTOR: APPLICATIONS & PROBLEMS

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ABSTRACT

The goal of this paper is to review in brief the basic physics of nanoelectronic device single-electron transistor [SET] as well as prospective applications and problems in their applications. SET functioning based on the controllable transfer of single electrons between small conducting "islands". The device properties dominated by the quantum mechanical properties of matter and provide new characteristics coulomb oscillation, coulomb blockade that is helpful in a number of applications. SET is able to shear domain with silicon transistor in near future and enhance the device density. Recent research in SET gives new ideas which are going to revolutionize the random access memory and digital data storage technologies.

KEYWORDS

Nanoelectronics; Single-electron transistor; Coulomb blockade, Coulomb oscillation, Quantum dot

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DESIGN OF HIGH EFFICIENCY TWO STAGE POWER AMPLIFIER IN 0.13UM RF CMOS TECHNOLOGY FOR 2.4 GHZ WLAN APPLICATION

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ABSTRACT

A two stage CMOS power amplifier is implemented in 0.13µm RF CMOS technology using ADS tool operating at 2.4 GHz with dc supply of 2.5 V. Driver stage as the input stage and power stage as the output stage are the two stages. A cascode topology is used in the driver stage and basic topology is used in the power stage. Output power at 1dB compression point is 20.028 dBm and maximum output power delivered by this circuit is 22.002 dBm. Power added efficiency calculated at 1 dB compression point is 44.669 % whereas the maximum power added efficiency comes out to be 70.196 %. The input return and output return losses are -11.132 dB and -12.467 dB respectively. Isolation loss and small signal gain are calculated to be -61.889 dB and 43.745 dB respectively. This circuit shows power gain of 42.728 dB at 1dB compression point. The total dc current flowing through this circuit is 0.0901 A. MOSFET only bias circuits are used to reduce total dc current. This circuit is designed for application in WLAN.

KEYWORDS

RFIC, RF CMOS, PAE, Impedance Matching, Cascode Topology

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DESIGN AND PERFORMANCE ANALYSIS OF NINE STAGES CMOS BASED RING OSCILLATOR

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ABSTRACT

This paper deals with the design and performance analysis of a ring oscillator using CMOS 45nm technology process in Cadence virtuoso environment. The design of optimal Analog and Mixed Signal (AMS) very large scale integrated circuits (VLSI) is a challenging task for the integrated circuit(IC) designer. A Ring Oscillator is an active device which is made up of odd number of NOT gates and whose output oscillates between two voltage levels representing high and low. There are a number of challenges ahead while designing the CMOS Ring Oscillator which are delay, noise and glitches. CMOS is the technology of choice for many applications, CMOS oscillators with low power, phase noise and timing jitter are highly desired. In this paper, we have designed a CMOS ring oscillator with nine stages.Previously, the researchers were unable to reduce the phase noise in ring oscillators substantially with nine stages. We have successfully reduced the phase noise to -6.4kdBc/Hz at 2GHz center frequency of oscillation.

KEYWORDS

Analog and mixed signal (AMS), VLSI circuit, CMOS Ring oscillator (RO), integrated circuit (IC), phase noise, center frequency of oscillation

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COMPARATIVE PERFORMANCE ANALYSIS OF XORXNOR FUNCTION BASED HIGH-SPEED CMOS FULL ADDER CIRCUITS FOR LOW VOLTAGE VLSI DESIGN

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ABSTRACT

This paper presents comparative study of high-speed, low-power and low voltage full adder circuits. Our approach is based on XOR-XNOR design full adder circuits in a single unit. A low power and high performance 9T full adder cell using a design style called "XOR (3T)" is discussed. The designed circuit commands a high degree of regularity and symmetric higher density than the conventional CMOS design style as well as it lowers power consumption by using XOR (3T) logic circuits. Gate Diffusion Input (GDI) technique of low-power digital combinatorial circuit design is also described. This technique helps in reducing the power consumption and the area of digital circuits while maintaining low complexity of logic design. This paper analyses, evaluates and compares the performance of various adder circuits. Several simulations conducted using different voltage supplies, load capacitors and temperature variation demonstrate the superiority of the XOR (3T) based full adder designs in term of delay, power and power delay product (PDP) compared to the other full adder circuits. Simulation results illustrate the superiority of the designed adder circuits against the conventional CMOS, TG and Hybrid full adder circuits in terms of power, delay and power delay product (PDP). .

KEYWORDS

Hybrid full adder, XOR-XNOR circuit, High Speed, Low Power, Very Large Scale Integrated (VLSI) Circuits,

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