

## Design and Implementation of 2 Bit Ternary ALU Slice

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### ABSTRACT

*This paper describes the architecture, design & implementation of two bit ternary ALU (T-ALU) slice. The proposed ALU is designed for two-bit operation & can be used for  $n$  bit operations by cascading  $n/2$  ALU slices. This ALU is implemented the usage of C-MOS ternary logic gates (T-Gates) for ternary mathematics & good judgment circuits. Ternary gates are implemented the use of enhancement / depletion MOSFET generation, consequently proposed ALU is appropriate for LSI / VLSI implementation. The designed approach used right here calls for best levels i.e. decoder & T-gates, as towards three ranges i.e. decoder, binary gates & encoder require in traditional ternary common sense Implementation.*

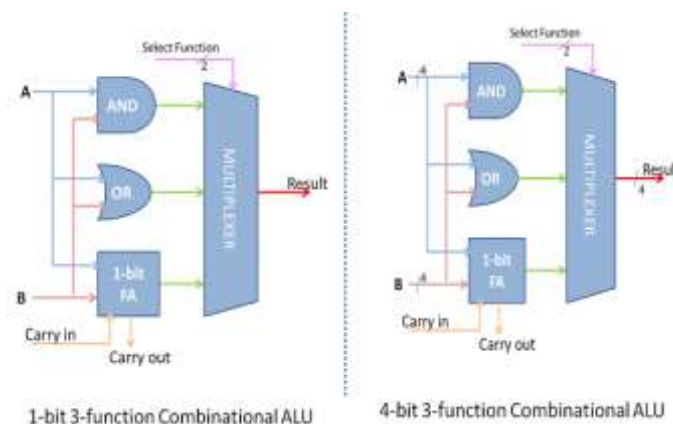
**Keywords:** ALU, MOSFET, logic gates

### INTRODUCTION

Alexander [1964] confirmed that natural base ( $e = 2.71828$ ) is the maximum radix for implementation of switching circuits. It seems that most efficient radix for the implementation of digital device is 3 than 2. Ternary logic device, meaning that it has 3 valued switching.

Ternary system has numerous vital advantages over binary. It may be summarized as discounts within the interconnections require to implement good judgment functions, thereby reducing

chip place, extra information can be transmitted over a given set of lines, lesser memory requirement for a given statistics duration. Except this serial & a few serial-parallel operations may be finished at better speed. It has been verified that consciousness & implementation of combinational & sequential characteristic is possible for ternary systems. The implementation is based around bipolar transistors, MOSFETs and many others. A primary switching factors, that's referred to as T-Gates.[1-4]



## **METHODOLOGY**

### **What is an ALU?**

ALU is formed through the combinational circuit. The combinational circuit used logical gates like AND, OR, no longer, XOR for their construction.

The combinational circuit does not have any reminiscence element to save a preceding information bit. Adders are the main a part of the mathematics common sense unit to perform addition, subtraction by 2's complement.

Logic gates are the constructing block of ALU. Logic gates are made from diode, resistors or transistors. These gates are used in integrated circuit constitute binary enter as 'ON' and 'OFF' state. Binary variety 0 is represented by 'OFF' and Binary quantity '1' is represented via 'ON' in an included circuit.

Registers: Registers provide rapid memory admission to cache, RAM, disks. They're constructed on CPU. They are small in size. They Process Intermediate data saved in registers.

Some of registers used for specific cause are, ALU used four standard purpose sign in. a majority of these four registers are sixteen-bit check in that is divided into registers. Sixteen-bit sign up implies that sign in can save maximum 16 bit of facts.[5-7]

### **Accumulator**

Accumulator is sixteen register. By using default way that any operand in practise does not specify a selected register for holding the operand at that point operand will routinely store in AC. AC is used as separate registers of 7 bit AL and AH. AC located inside the ALU. Intermediate facts and end result after execution will save in AC.AC uses MBR to address reminiscence.

Software Counter: pc stands for program counter. It's a sixteen-bit check in. It counts the range of instruction left for execution. It acts as a pointer for commands and also referred to as education pointer register.

### **Flag check in**

It's also known as a status register or software popularity check in. Flag register holds the Boolean value of status word used by the process.

### **Auxiliary flag**

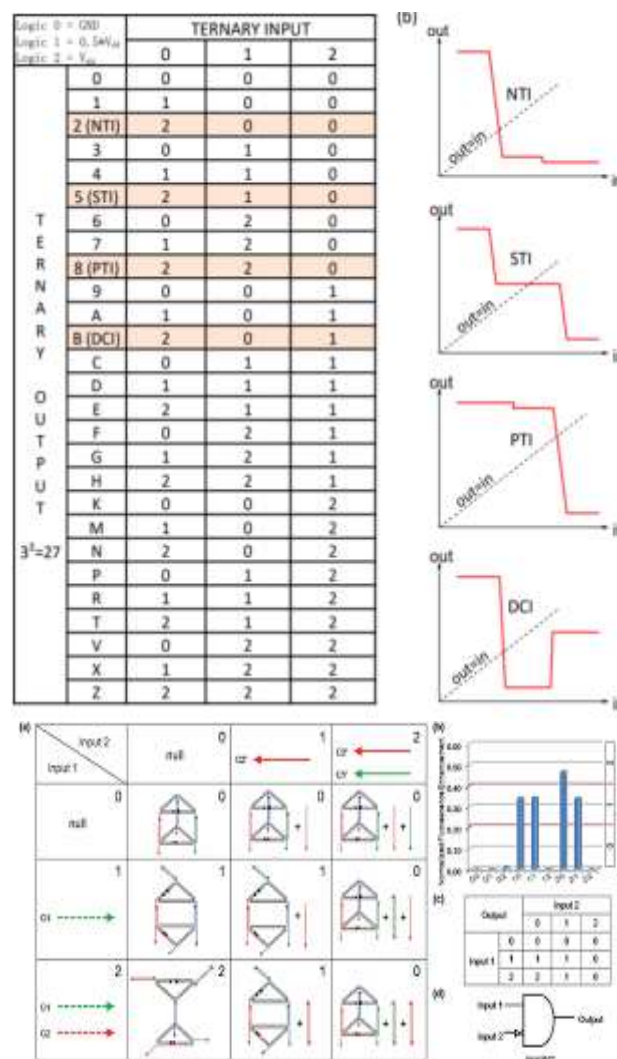
If two numbers are to be brought such that if within the starting of a higher bit there's a carry, this is called an auxiliary bit.

### **Basics of Ternary Logic Design**

In traditional binary Boolean logic, there are a complete of twenty-two = four monadic functions. Even as in ternary common sense, the quantity of monadic capabilities is  $3^3 = 27$ . Those 27 ternary functions are enumerated from 0 to nine after which A to Z. Strictly speaking, we do not want all of these capabilities due to the fact there are robust relationships among such operations in Boolean algebra.

Several of them are nontrivial and meaningful. as an instance, capabilities zero, D, and Z are the trivial, consistent-valued functions; characteristic P is identification; feature 5 is the usual ternary inverter (STI); features 2 and eight are the negative threshold inverter (NTI) and effective threshold inverter (PTI), respectively; functions 7 and B are increment cycling inverter (ICI) and decrement cycling inverter, respectively.

It's miles widely conventional that the most vital and fundamental components in ternary good judgment are STI, NTI and PTI The output-enter characteristic curves of such ternary functions were proven in parent.

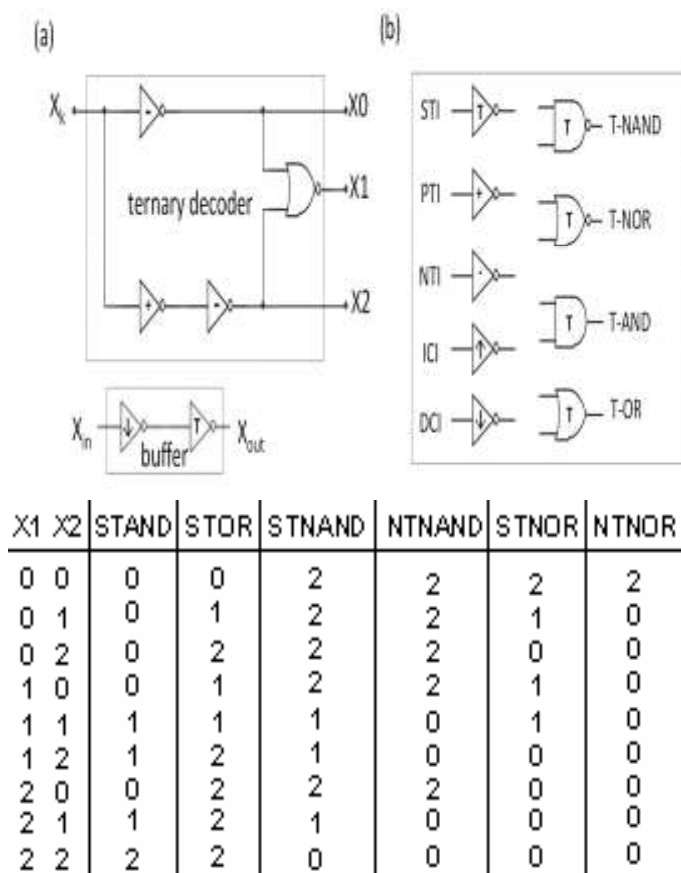


Ternary logic is a type of multi valued logic which adds a third value to the conventional binary logic.

In this paper, ternary logic values denoted by symbols 0, 1 and 2 have voltages levels equal to ground,  $V_{dd}/2$  and  $V_{dd}$ , respectively. A ternary function of  $n$  variables is a function mapped  $\{0, 1, 2\}^n$  to  $\{0, 1, 2\}$ . The basic ternary operations (AND, OR and INVERT) are defined by operators,  $+$  and  $-$  denote AND, OR and arithmetic subtraction operations, respectively.

The most fundamental building blocks in the ternary design of digital systems are ternary inverter, NAND and NOR gates. The ternary gates are designed according to the conventions provided by given equations.

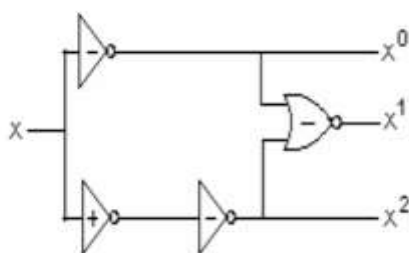
In ternary systems, there are three types of inverters: positive ternary inverter (PTI), negative ternary inverter (NTI) and standard ternary inverter (STI). These inverters are defined by more set of equations where  $x$  and  $XC$  are the input and output of the inverter, respectively



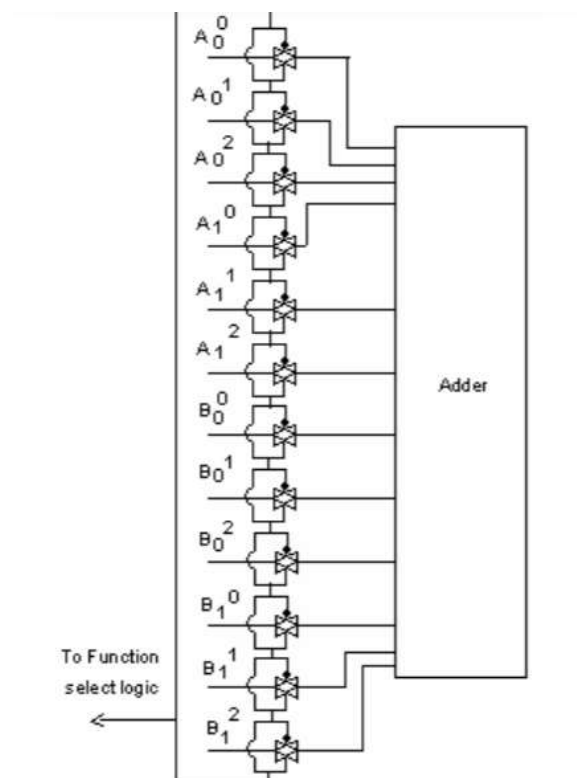
### ALU WORKING

Block diagram & architecture of proposed T-ALU is shown in fig 1 and 2. Its functions are given in table 1. The operating voltages required are +5 & -

5v. Main building blocks of ALU are function selection logic, CMOS transmission gates & separate processing modules like adder, subtractor, comparator etc.



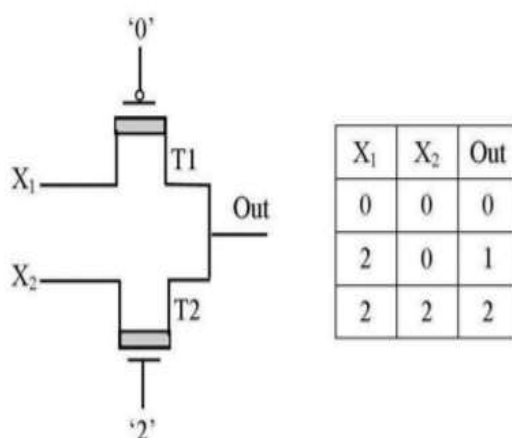
X	X <sup>0</sup>	X <sup>1</sup>	X <sup>2</sup>
0	2	0	0
1	0	2	0
2	0	0	2



### Encoder Design

For the implementation of ternary processing modules, a brand new encoder design is proposed. This layout incorporates only transistors T1 and T2, as proven in figure 4. Those transistors with identical parameters carry out voltage department and bring output same to  $(X_1 + X_2)/2$ , as defined in truth desk of

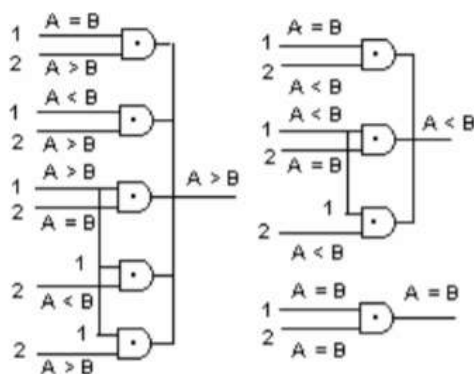
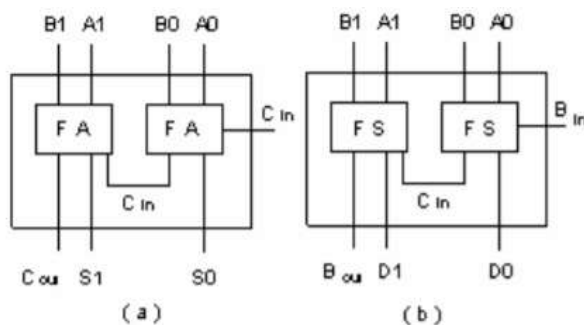
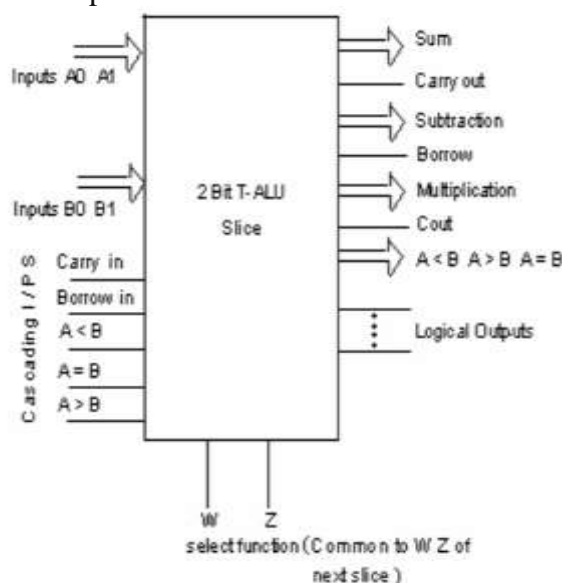
encoder proven in determine four. The proposed layout makes use of skip transistor common sense and thereby eliminates an instantaneous direction from Vdd to ground which leads to less strength dissipation in comparison to the encoder of. Consequently, it results in the low-electricity designs of various TALU modules



### EXPECTED RESULT

Experimental circuits are designed & implemented to verify workings of some modules of proposed ALU. These circuits are build using logic gates specified in section II. Typical experimental results are presented for adder, multiplier, & Ex-OR operations & as seen desired operations

are achieved. Fig 15(a) shows storage oscilloscope waveform for adder module when  $B1=1$   $B0=2$ ,  $A1=0$ ,  $A0=2$ . , ( b ) is output of multiplier module when  $B1=2$ ,  $B0=2$ ,  $A1=2$ ,  $A0=2$  & finally ( C ) shows Ex-OR operation  $B1=1$ ,  $B0=0$ ,  $A1=1$ ,  $A0=0$ .





## PERFORMANCE EVALUATION

The proposed TALU is analysed and simulated the use of HSPICE simulator with Compact SPICE model for 32 nm CNTFETs (Stanford model, 2007). This Stanford model has been defined in Deng and Wong (2007a, 2007b). Similarly, brief simulations outcomes affirm an appropriate capability of the proposed layout. It verifies that consistent with the fee of M0 and M1, FASE executes addition, subtraction and XOR operations.

Transient simulations also are done for exclusive processing modules to measure postpone and electricity performance of the proposed TALU layout as well as to make contrast with present CNTFET-based totally designs.

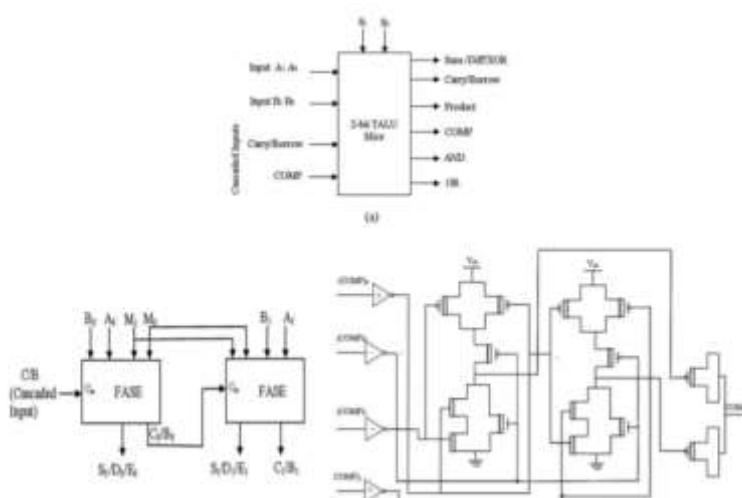
## CONCLUSION

An entire architecture, layout & implementation of two-bit ALU slice is described. The scheme primarily based on stepped forward ternary logic gate is likewise described. It reveals vast ways of reduction in circuit complexity, low static energy consumption & extended velocity of operation. The ALU may be extended to implement extra function with

modification in choice good judgment, decoder and many others. Consequently it may be integrated as processing unit for ternary microprocessors.

The ternary logic functions also can be implemented the usage of ternary PLAs thereby growing packing density, more complicated characteristic implementation and so on, for Development. Novel hardware-green and low-energy CNTFET-based TALU has been proposed in this paper. The proposed TALU provides a hardware optimized answer by using introducing ASE processing module in addition to with the aid of presenting a brand new encoder design for realization of ternary features. Moreover, it achieves a discount in PDP through sixty two% averaged over all operations (addition, multiplication, and comparison) with recognize to existing TALU designs.

In addition, the proposed 2- bit TALU slice may be easily cascaded to shape an n-bit design using  $n/2$  slices. Hence, the proposed TALU can function an efficient processing unit for contemporary ternary microprocessors with CNTFETs in Nano scale technology.



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