Dual-Input Pseudo-CMOS Logic for Digital Applications on Flexible Substrates

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***Abstract*—A new standard cell topology, Dual-Input Pseudo-CMOS (DIPC), for dual-gate Indium-Gallium-Zinc-Oxide (IGZO) thin-film transistor (TFT) technology on flexible substrates is presented. The proposed logic topology is compared with the conventional Pseudo-CMOS in terms of robustness (noise margin), speed performance, power consumption and area usage. This work shows that the back-gate of a TFT can be used as a separate parallel transistor reducing the number of devices in logic gates without compromising the speed and the power. Two 32-bit code generators for RFID transponders with both libraries have been designed and fabricated using n-type only TFTs with a channel length of 5 μm. The proposed topology allowed to reduce the number of TFTs by 24% and the chip consumes only 2.2 μW of power at 4 kHz clock frequency and 1 V of supply voltage. This work also forecasts that the number of TFTs can be reduced strongly by using the proposed DIPC topology for complex designs such as arithmetic logic units and microprocessors.**[1]

I. Introduction

Thin-film transistor (TFT) technologies have some unique characteristics which place them in an important position in the semiconductor industry. First, there is only a limited amount of process steps which do not require as high temperatures as the silicon processes, therefore the manufacturing cost is lower than the silicon devices of the same area, but with a lower intrinsic performance. Second, glass and flexible materials like polyimide can be used as substrate for TFT devices. The thin and flexible nature of the substrate enables bending the circuitry down to 3 mm of radius [1] and various applications such as radio-frequency identification (RFID) tags [2] and on-body health patches for biomedical applications [3]. Finally, large area manufacturing combined with the other properties brought curved LED displays into our daily lives [4].

Among other semiconductors, amorphous Indium-Gallium-Zinc-Oxide (a-IGZO) is the ideal candidate for realizing complex digital thin-film circuits with n-type only transistors having a back-gate terminal. A cross-section of the flexible dual-gate self-aligned (DGSA) TFT technology which is used in this work is depicted in Figure 1. There are two metal gates to control the thin IGZO channel over SiO_2 insulators with a symmetrical thickness of 200 nm on both sides. The dielectric material between source/drain (SD) and gate layers is SiN_x with a thickness of 200 nm. The average on-current (I_{on}) of 174 TFTs with W/L ratio of 10 μm / 5 μm on 6-inch wafer is 5.36 μA where the gate and the back-gate terminals are connected to each other and V_{GS} = V_{DS} = 5 V. The average on-voltage (V_{on}) where the TFTs start conducting drain-to-source current (I_{DS}) is 0.29 V with a standard deviation of 0.18 V.

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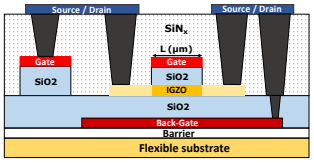


Fig. 1. Dual-gate self-aligned technology stack.

Having a second terminal to control the channel of thin-film transistor has many advantages. By changing the back-gate voltage, V_T of a TFT can be shifted in positive or negative direction as in Figure 2 (left). This feature is used in display applications to compensate V_T variations by tuning the back-gate voltage of individual TFTs [5]. Dual-gate TFTs in this technology are symmetrical devices such that the roles of the front-gate and the back-gate can be interchanged. Figure 2 (right) plots the I_{DS} vs V_{BG} of a TFT with different V_G values.

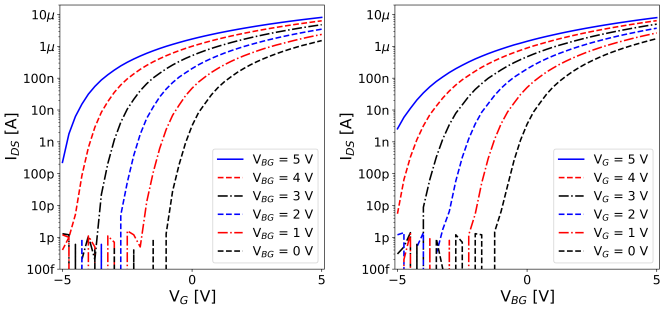


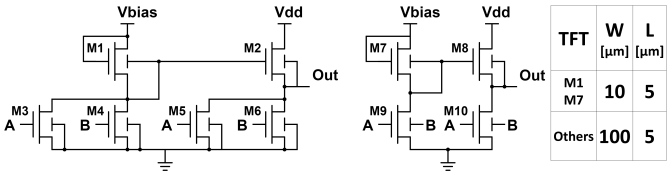
Fig. 2. Measured I_{DS} vs V_G for different V_{BG}'s (left) and I_{DS} vs V_{BG} for different V_G's (right).

Pseudo-CMOS logic is the most common logic topology for unipolar technologies thanks to its robust characteristics [6]. Having two stages helps shifting the voltage transfer curve and provides a rail-to-rail output swing. However, it requires many TFTs per standard cell (2 x number-of-inputs + 2). Therefore it causes a high chip area usage. Chip area and the number of devices are two important factors determining the total yield of

an integrated circuit (IC). In this study, a new logic topology (Dual-Input Pseudo-CMOS) for dual-gate TFT technologies is proposed and compared to the conventional Pseudo-CMOS topology in terms of DC transfer characteristics and performance with a 32-bit RFID transponder chip. The new topology enables to reduce the number of TFTs in a digital IC and therefore the chip area without compromising the robustness, power consumption and performance specifications achieved with the conventional Pseudo-CMOS logic.

II. Dual-Input Pseudo-CMOS Logic and Standard Cell Library

The idea of the proposed Dual-Input Pseudo-CMOS (DIPC) topology is based on replacing two parallel TFTs in the conventional Pseudo-CMOS logic by one dual-gate TFT [6] [7]. Therefore, DIPC topology allows to reduce the number of TFTs only for the gates having OR operation in their function (NOR, Or-And-Invert etc.). The other standard cells (NAND, INV etc.) are the same with conventional Pseudo-CMOS logic. Since only depletion mode n-type transistors are available in this technology, it is not recommended to connect many transistors in series in the pull-down network. Therefore, logic gates such as NAND3 and NAND4 are not included in the standard cell library. Circuit schematics of NOR2 gates for both topologies are shown in Figure 3 while the Table I shows the number of transistors per standard cell in libraries of both logic styles used in this study.



TFT	W [µm]	L [µm]
M1 M7	10	5
Others	100	5

Fig. 3. Conventional Pseudo-CMOS NOR2 gate (left) and proposed Dual-Input Pseudo-CMOS NOR2 gate (right).

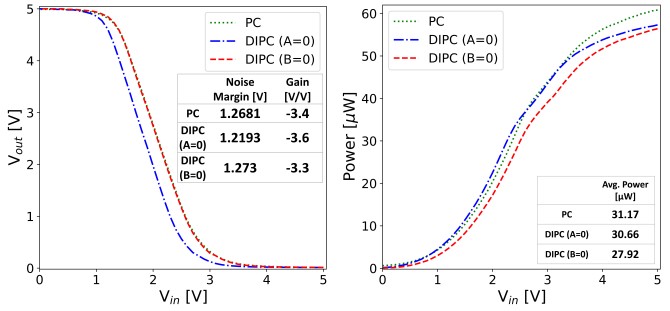


Fig. 4. Measured voltage transfer curves (left) and power consumption during switching (right) of NOR gates in both topologies (V_{BIAS} = 10 V).

Voltage transfer characteristics and the total static power (P_{VDD} + P_{VBIAS}) of NOR gates for both topologies are plotted in Figure 4 where V_{DD} is 5 V and V_{BIAS} is 10 V. It can be observed that the proposed DIPC topology shows very similar DC characteristics with the conventional Pseudo-CMOS topology. The voltage transfer curve of the logic gates can be tuned by changing V_{BIAS} for the same V_{DD} as shown in Figure 5 (left) similar to the conventional Pseudo-CMOS logic. After the fabrication of the circuit, the noise margin of the gates can be tuned to an optimum level as shown in Figure 5 (right). The left y-axis indicates the noise margin while the right y-axis is the trip voltage where the input voltage is equal to the output voltage of the logic gate.

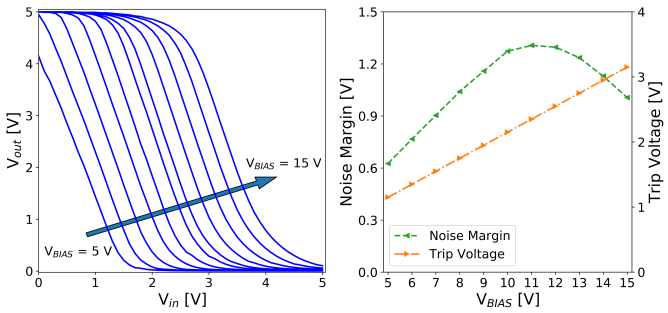


Fig. 5. Impact of V_{BIAS} on DC characteristics of the DIPC NOR2 gate (V_{DD} = 5 V, V_B = 0).

Ring oscillator circuits with 33 cascaded inverters have been designed and measured in order to evaluate the speed performance and power consumption of the inverter cell which is used in both standard cell libraries. It should be noted that the schematic of the inverter is the same with DIPC NOR2 gate where V_B = 0. Figure 6 (left) shows the power consumption per inverter and Figure 6 (right) plots the propagation delay for different supply voltage combinations. It can be observed that the lowest operation voltage for the ring oscillator is when V_{DD} = 0.5 V and V_{BIAS} = 0.75 V.

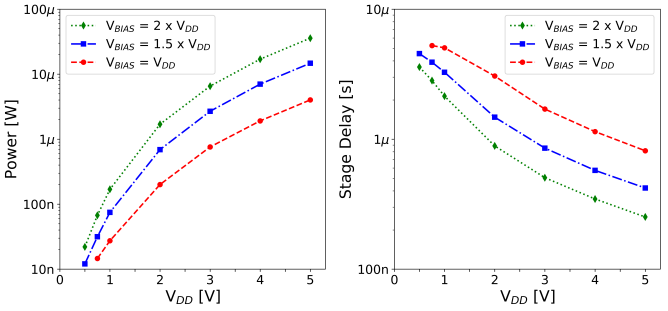


Fig. 6. Power consumption (left) and stage delay (right) of the inverter for different supply voltages based on ring oscillator measurements.

III. 32-Bit Code Generator for RFID Transponder

In order to further evaluate the Dual-Input Pseudo-CMOS topology and compare it with the conventional Pseudo-CMOS logic, two code generator chips compatible with RFID transponder circuits with both standard cell libraries have been designed and fabricated. The chip generates a pre-defined 32-bit code as a serial output followed by another 32-bit of logic zero for each 64 clock cycles applied to the input. It mainly consists of a 6-bit up-counter, a 5-to-1 hard-coded combinatorial core and an output register with a buffer. For the design of the chip, a typical design flow procedure is followed from RTL to GDS level similar to CMOS physical

TABLE I
LIST OF STANDARD CELLS USED IN THE LIBRARIES AND THE CHIPS

	Standard PC		Dual-Input PC		
Cell Name	**Number of TFTs**	**Area (μm^2)**	**Number of TFTs**	**Area (μm^2)**	**Used in the Chip**
INV	4	38400	4	36000	22
INVx3	4	64000	4	60000	2
NAND2	6	76800	6	72000	10
NOR2	6	38400	4	36000	7
NOR3	8	51200	6	42000	3
NOR4	10	64000	6	42000	0
OAI21	8	108800	6	72000	6
OAI22	10	134400	6	72000	3
DFFN	38	236800	26	186000	10
Chip	**680**	**5587200**	**516**	**4518000**	**Total = 63**

implementation flows. However, the Liberty Timing File (.lib) which is used for the synthesis of top-level design is borrowed from a CMOS technology. In this way, the gate-level netlist of both chips are kept the same in order to see the impact of the chosen topology on the circuit performance.

The die micrographs of two 32-bit code generator circuits on a flexible substrate are in Figure 7. Excluding the test pads, the area of the chip with the conventional Pseudo-CMOS is 12.28 mm^2 (W: 4012 μm, H: 3060 μm) and the area of the one with Dual-Input Pseudo-CMOS is 10.57 mm^2 (W: 3596 μm, H: 2940 μm). There is an area reduction of 13.9% with the proposed logic topology. However, it should be noted that the area of the standard cells takes around 45% of the total chip area while the rest is used for row-to-row spacing and the routing between cells. This TFT technology is not optimized for complex digital circuits yet and there are no specific metal layers for routing. The routing needs to be done using the same layers with Source/Drain and Gate of TFTs, so the standard cells cannot be placed close to each other.

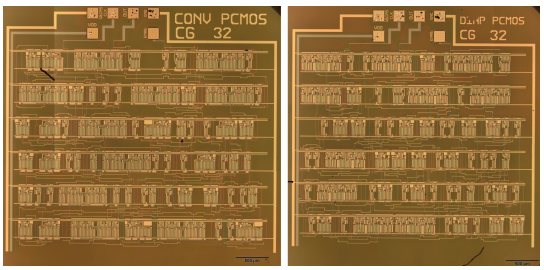


Fig. 7. Die pictures of 32-bit code generators using conventional Pseudo-CMOS logic (left) and Dual-Input Pseudo-CMOS logic (right).

Other parameters to compare libraries are the total area of the standard cells in each chip excluding the area for routing & spacing and the total number of TFTs. The list of the standard cells in both libraries, the number of TFTs used in each cell and the area of the cells are listed in Table I. Using the proposed DIPC topology results in reduction of the total cell area from 5.59 mm^2 to 4.52 mm^2 which is 19% smaller. It should be noted that the height of the cells in conventional Pseudo-CMOS library is 320 μm while it is 300 μm in DIPC library, so the area of some cells in two libraries is different even though their circuit schematics are the same. With the proposed topology, total number of TFTs used in the chip is reduced from 680 to 516 which is a 24% reduction.

Figure 8 plots the measured power consumption vs clock speed for both code generator chips. It should be noted that the contribution of dynamic power to the total power is negligible due to the dominant static current for these unipolar topologies. The measurements are done while V_{BIAS} is equal to V_{DD} until 5 V, then V_{BIAS} is being increased until the chip does not operate correctly while V_{DD} is kept at 5 V. The minimum supply voltage recorded is 1 V with 4 kHz of operation speed and 2.2 μW power consumption. The maximum operation speed recorded is with 108 kHz of clock frequency when V_{DD} is 5 V and V_{BIAS} is 11 V with power consumption of 4.756 mW. It can be observed that two chips with different libraries show very similar characteristics in terms of power consumption and operation speed. The slight differences including power, speed and operating supply range probably stem from the process variations. As these two chips are located far from each other, local V_T and mobility parameters might be different.

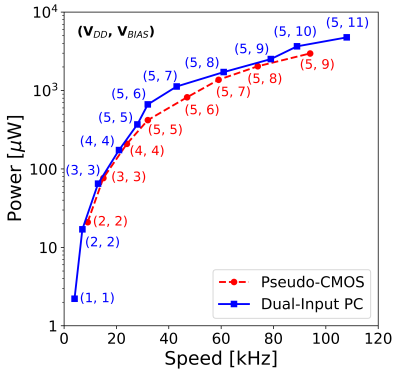


Fig. 8. Power vs speed performance of 32-bit transponder with both logic topologies.

Scope data of 32-bit code generator using Dual-Input Pseudo-CMOS library with the clock frequency of 4 kHz and supply voltages V_{DD} being equal to V_{BIAS} of 1 V is seen in Figure 9. The circuit generates a serial output data of the following 32-bit pre-defined code followed by 32-bit of logic zero: 1001-0011-0100-1100-0110-1111-0111-0010. It can be observed that the output signal does not have a rail-to-rail swing when V_{BIAS} is not larger than V_{DD} as predicted from DC characteristics.

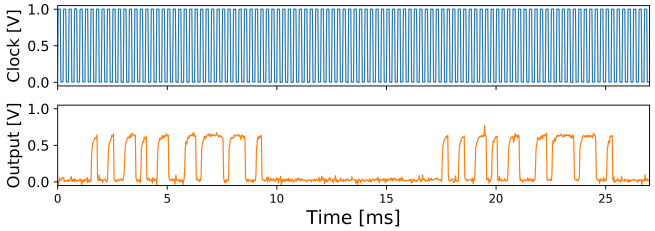


Fig. 9. Scope data from 32-bit code generator with DIPC logic topology at V_{DD} = V_{BIAS} = 1 V.

Following the validation of Dual-Input Pseudo-CMOS logic topology with the measurements of 32-bit RFID transponder chips, potential reduction of the number of required TFTs for simpler and more complex circuits (from 8 bit to 1 kbit code generators, 8-bit custom design ALU and 8-bit custom design CPU) is investigated using the physical implementation flow. Figure 10 shows a linear relationship between the complexity of the circuit (number of used logic gates) and the number of used TFTs. With the proposed DIPC topology, it is possible to reduce the number of TFTs for a complex digital design employing 1186 logic gates, from 9168 to 7052 transistors. This is a gain of more than 2000 devices which is beneficial for the chip size and corresponding yield.

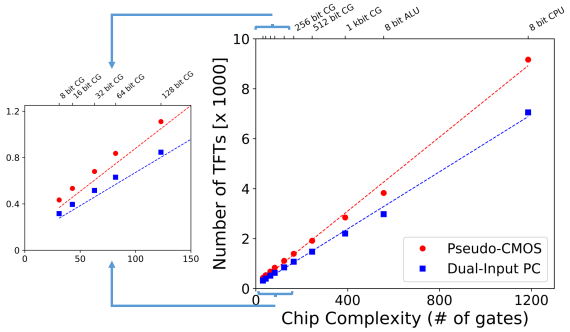


Fig. 10. Number of TFTs needed to realize a variety of digital circuits using both logic topologies.

IV. Conclusions and Discussion

A new logic topology, Dual-Input Pseudo-CMOS, for digital applications with dual-gate TFT technologies is proposed. This logic topology is compared with the conventional Pseudo-CMOS logic in terms of footprint, DC transfer characteristics and performance in more complex digital circuits. It has been shown that a dual-gate TFT can take place of two regular TFTs which are connected parallelly. This technique allows to reduce the number of TFTs in complex digital circuits substantially without compromising the operation speed and power consumption. The fabricated 32-bit code generators for RFID transponders using both logic topologies have been compared with the similar works made on foil in the literature as seen in Table II. This work also predicts a significant reduction in the number of TFTs which are used by more complex digital chips having more than a thousand logic gates. The proof of concept presented in this paper can be improved to further reduce the area and the number of devices of digital TFT circuits with the following improvements: First, as depicted in Figure 1, there is no direct VIA connecting gate and back-gate metals even though they are adjacent to each other. There would be more area reduction if the technology stack allowed back-gate to be used as a routing metal. Second, specific routing metals could be developed in the process technology. Adding routing layers on top of Source/Drain metal layer would allow the Place & Route tool to abut the rows to reduce the area.

TABLE II
Comparison of This Work to State of the Art

	IEEE RFID 2017 [2]	ISSCC 2017 [8]	SID 2020 [9]	**This Work**	
Tech-nology	a-IGZO	a-IGZO	a-IGZO	a-IGZO	a-IGZO
Logic Type	Pseudo-CMOS	Pseudo-CMOS	Pseudo-CMOS	Pseudo-CMOS	Dual-Input PC
L [μm]	10	4	5	5	5
Memory	16-bit	128-bit	64-bit	32-bit	32-bit
Min. Supply	V_{DD}=1V V_{Bias}=2V	V_{DD}=3V V_{Bias}=6V	V_{DD}=0.6V V_{Bias}=0.6V	V_{DD}=2V V_{Bias}=2V	V_{DD}=1V V_{Bias}=1V
Data Rate	148 b/s @1V	105.9 kb/s @3V	35 b/s @0.6V	9 kb/s @2V	4 kb/s @1V
Power	6.8 μW @1V	7.5 mW @3V	140 nW @0.6V	20.9 μW @2V	2.2 μW @1V
Number of TFTs	n/a	1712	409	680	516
Chip Area	80.38 mm^2	50.55 mm^2	12.5 mm^2	12.28 mm^2	10.57 mm^2

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