LIT3RICK: AN UP5K ULTRASOUND PULSE-ECHO DEVICE

A POLYGLOT DOCUMENTATION FILE

Luc Jonveaux[*]
Tinkerer, Milly le Meugon, France
`contact@un0rick.cc`

December 22, 2021

ABSTRACT

Non destructive testing and imaging ultrasound have been around since the ’50s. Many ultrasound open-source projects are emerging, mostly focusing on image processing - while hardware has been left behind. Several teams have produced successful designs to be used on commercial US scanners, but they are not cheap, and are difficult to access.

I couldn’t find designs to play with, that would be affordable or open, so I decided to update the previous one, the un0rick, for a more cost-efficient board designed for makers, researchers and hackers.

This PDF is also a ZIP that contains the sources to the hardware and some data too, don’t hesitate to have a look. Just rename the file from .PDF to .ZIP and you’re ready to go .

***K*eywords** open-source · ultrasound · hardware · ice40 · fpga

1 Overview

This wonderful board has been designed to provide a curious tinkerer with the basis to play with, and understand, ultrasound NDT and imaging bases.

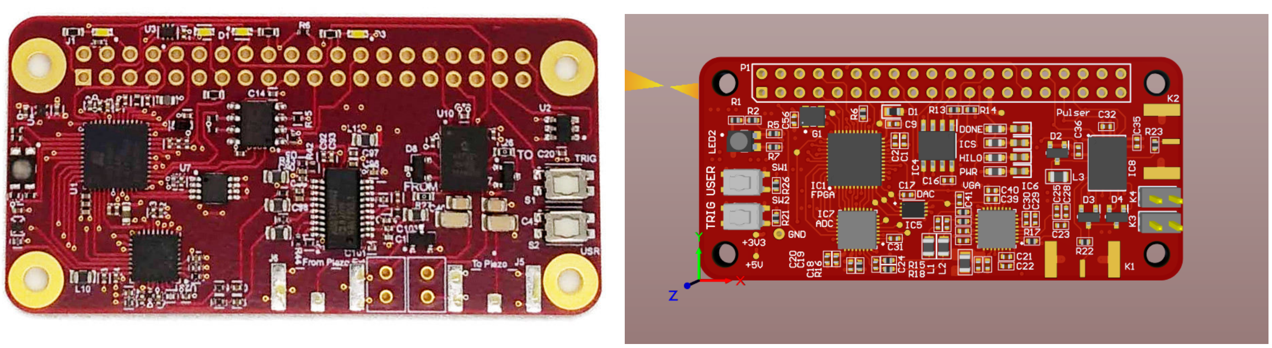

Figure 1: Top side of the lit3rick and its update, the lit3-32 boards.

1.1 Concept

FPGA: a Lattice up5K chip: chosen as the right compromise between a number of IOs, RAM, and fabric speed. It is compatible with Claire Wolf’s Yosys Open SYnthesis Suite.

Memory: FPGA RAM - 1Mb, as well as 8 Mb SPI Flash for FPGA configuration. It gets filled with a AD9629BCPZ-65, 64Msps ADC.

[*]More on the website `http://un0rick.cc`. This paper has its on Zenodo DOI 10.5281/zenodo.3364559

Ultrasound processing: A VGA (AD8331 for the lit3rick, AD8332 for the lit3-32) controled by DAC, with a HV7361GA pulser (bipolar, +- 100V). The VGA allows in the first case an amplification in the +7.5 dB to +55.5 dB range, while the second range of the AD8332 allows to reach 84.5dB.

Extensibility: two SMA plug for the piezos (with capacity to separate the TX and RX paths) as well as a general header for RPi GPIO

User Interfaces: a RGB LED, 2 push button (with software noise debouncing) and jumpers for high voltage selection, connected to the TX/RX and I2C pins of the RPi header. The header i2s IOs are also connected, allowing for exporting signals through this audio bus.

Input Voltage: 5 V from RPi or USB, uses 350mA-450mA at 5V with a raspberry on. The FPGA and logic operate at at 3.3 V. For cost-efficiency, the high voltage generation component was removed from the board.

2 Where to find the latest sources

The latest sources of the hardware as well as software are available at `https://github.com/kelu124/lit3rick/`. However, this PDF also doubles as an archive (you can rename the .pdf as a .zip, and you'll see), and contains, in short: a set of gerbers and BOM, some VHDL/verilog code, a basic FPGA binary ready to be used, and a python library to operate the board from a Raspberry Pi. There may be some other stuff there, but I forgot what I put there.

3 Operation

The FPGA has all the right logic in place to provide you with a full control over the pulse-echo process. At the time of this paper, the verilog had been developed for the lit3rick, but not for the lit3-32 board.

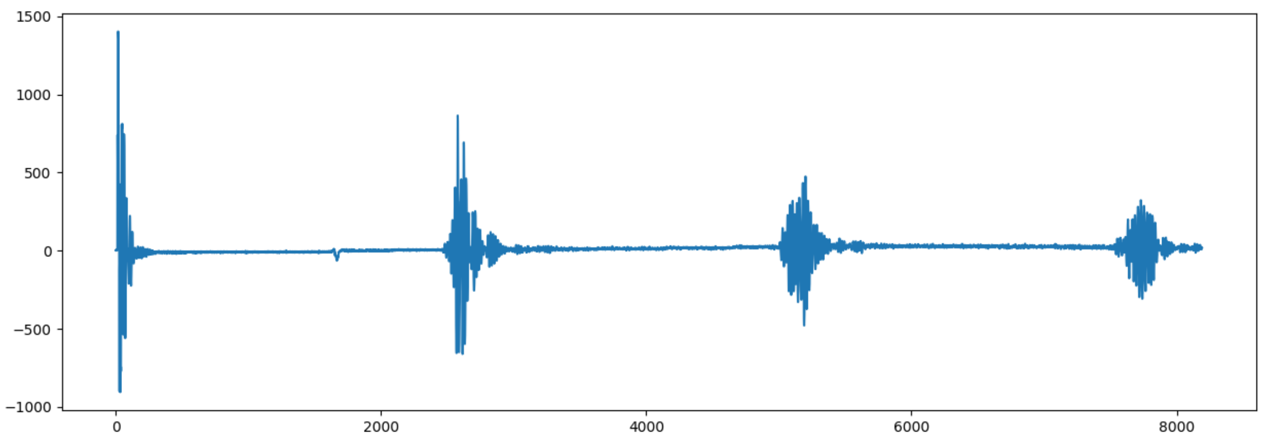

Figure 2: Example of raw signal acquisition on the lit3rick.

We have demonstrated the possibility as well to provide an onboard filtering, enveloppe detection and enveloppe compression, using an A-Law approach.

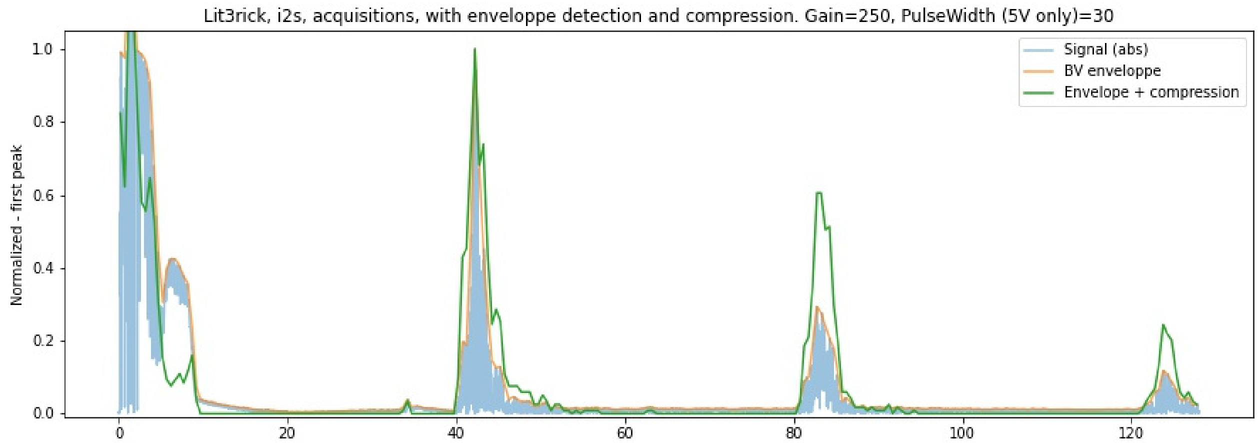

Figure 3: Example of enveloppe detection acquisition.

4 Last details

Certification The lit3rick and lit3-32 boards are also open-hardware certified, respectively under ID FR000006 and ID FR000016.

License This work is based on previous TAPR projects, the un0rick and the echOmods projects. The lit3rick project and its boards are open hardware and software, developed with open-source elements.

5 Links to go further

- Come and chat : join the Slack channel
- The full GitHub Repo with more ongoing works : also a messy braindump with all experiments
- The board's Tindie shop to get it
- The project Hackaday page with more logs
- Check out my previous work on the topic of ultrasound modules [1] and its dataset on Zenodo. More to come!

6 Next steps

Plenty to do on the next steps! Let me know if you'd like to contribute. The current shopping list (non-exhaustive) may include:

- Improving the documentation, and updated the work of its predecessor, the un0rick [3].
- Work on BOM costs and overall hardware design.
- Increase the high voltage source, and have it settable via an on-board, and ideally have a bipolar design.
- Improving the features of the onboard firmware.. and try to develop a VGA output ! So far, we have put a small micropython design up and running.
- Work on the FTDI - so I have only used the RPi, and write something to program the flash from the RPi.

References

[1] Luc Jonveaux 2017. Arduino-like development kit for single-element ultrasound imaging. In *Journal of Open Hardware, 1(1), p.3*. DOI: 10.5334/joh.2

[2] Luc Jonveaux 2018. The pyusbus repository. Website at *https://github.com/kelu124/pyusbus*

[3] Luc Jonveaux 2019. un0rick : open-source fpga board for single element ultrasound imaging On *Zenodo*. DOI: 10.5281/zenodo.3364559

[4] Luc Jonveaux 2021. lit3rick: an up5k ultrasound pulse-echo device On *Zenodo*. DOI: 10.5281/zenodo.5792245

[5] Luc Jonveaux 2021. An open-source max14866 development board On *Zenodo*. DOI: 10.5281/zenodo.5792252

[6] Luc Jonveaux 2021. pyubus: opening usb ultrasound probes On *Zenodo*. DOI: 10.5281/zenodo.5792256